1 INTRODUCTION

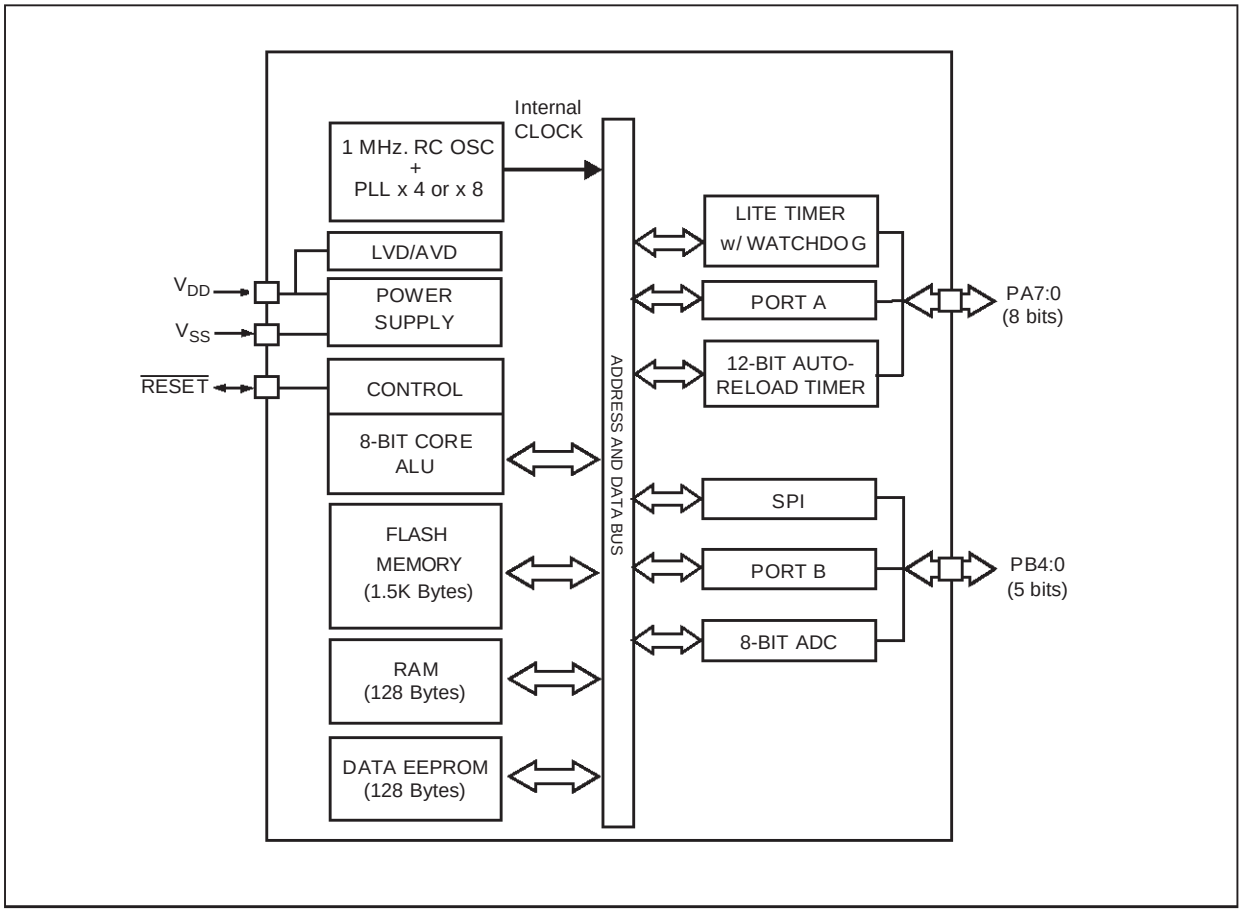
The ST7FLITE0 is a member of the ST7 microcontroller family. All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The ST7FLITE0 features FLASH memory with byte-by-byte In-Circuit Programming (ICP) and In-Application Programming (IAP) capability.

Under software control, the ST7FLITE0 device can be placed in WAIT, SLOW, or HALT mode, reducing power consumption when the application is in idle or standby state.

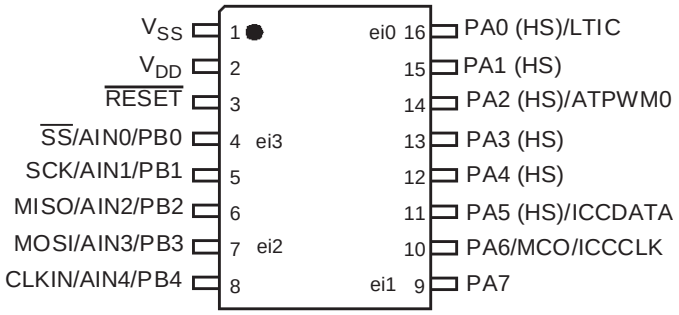
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. General Block Diagram



2 PIN DESCRIPTION

Figure 2. 16-Pin Package Pinout (150mil)



(HS) 20mA high sink capability
ei_x associated external interrupt vector

PIN DESCRIPTION (Cont'd)

Legend / Abbreviations for Table 1**:**

Type: I = input, O = output, S = supply

In/Output level: C= CMOS $0.15V_{DD}/0.85V_{DD}$ with input trigger

C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog

– Output: OD = open drain [2], PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°	Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
					Input				Output			
			Input	Output	float	wpu	int	ana	OD	PP		
1	V_{SS}	S									Ground	
2	V_{DD}	S									Main power supply	
3	$\overline{RESET}$	I/O	C_T			X			X		Top priority non maskable interrupt (active low)	
4	PB0/AIN0/$\overline{SS}$	I/O	C_T		**X**	ei3			X	X	**Port B0**	ADC Analog Input 0 or SPI Slave Select (active low)
5	PB1/AIN1/SCK	I/O	C_T		**X**	X			X	X	**Port B1**	ADC Analog Input 1 or SPI Serial Clock
6	PB2/AIN2/MISO	I/O	C_T		**X**	X			X	X	**Port B2**	ADC Analog Input 2 or SPI Master In/ Slave Out Data
7	PB3/AIN3/MOSI	I/O	C_T		**X**	ei2			X	X	**Port B3**	ADC Analog Input 3 or SPI Master Out / Slave In Data
8	PB4/AIN4/CLKIN	I/O	C_T		**X**	X			X	X	**Port B4**	ADC Analog Input 4 or External clock input
9	PA7	I/O	C_T		**X**	ei1			X	X	**Port A7**	
10	PA6 /MCO/ICCCLK	I/O	C_T		**X**	X			X	X	**Port A6**	Main Clock Output/In Circuit Communication Clock
11	PA5/ ICCDATA	I/O	C_T	HS	**X**	X			X	X	**Port A5**	In Circuit Communication Data
12	PA4	I/O	C_T	HS	**X**	X			X	X	**Port A4**	
13	PA3	I/O	C_T	HS	**X**	X			X	X	**Port A3**	
14	PA2/ATPWM0	I/O	C_T	HS	**X**	X			X	X	**Port A2**	Auto-Reload Timer PWM0
15	PA1	I/O	C_T	HS	**X**	X			X	X	**Port A1**	
16	PA0/LTIC	I/O	C_T	HS	**X**	ei0			X	X	**Port A0**	Lite Timer Input Capture

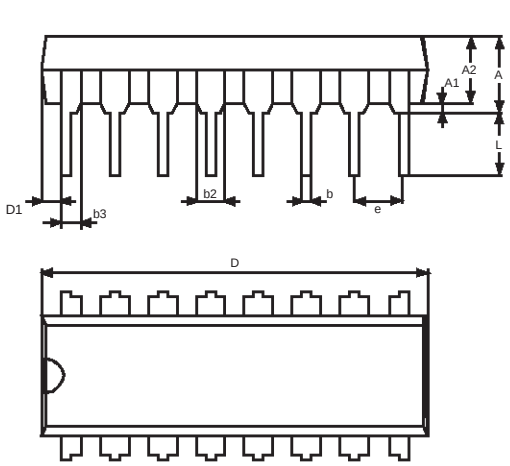
Note:

In the interrupt input column, "ei_x" defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

3 PACKAGE CHARACTERISTICS

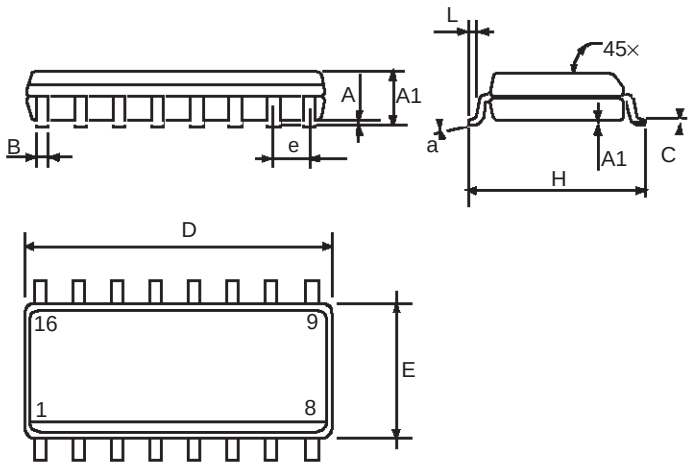
3.1 PACKAGE MECHANICAL DATA

Figure 3. 16-Pin Plastic Dual In-Line Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
b3	0.76	0.99	1.14	0.030	0.039	0.045
c	0.20	0.25	0.36	0.008	0.010	0.014
D	18.67	19.18	19.69	0.735	0.755	0.775
D1	0.13			0.005		
e		2.54			0.100	
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150
eB			10.92			0.430
	Number of Pins					
N	16					

Figure 4. 16-Pin Plastic Small Outline Package, 150-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	9.80		10.00	0.386		0.394
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
α	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
	Number of Pins					
N	16					

0016020

Notes:

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