Table 1. Device summary

Root Part Number	Package	Packaging
STA8090FG	TFBGA99 5x 6mm	Tape and Reel

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1 Overview

STA8090FG is one of the part number of Teseo III STA8090x series.

STA8090FG is a highly integrated single-chip standalone GNSS receiver designed for positioning system applications.

STA8090FG embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including the US GPS, European Galileo, Russia's GLONASS, Chinese BeiDou and Japan's QZSS.

The STA8090FG ability of tracking simultaneously the signals from multiple satellites regardless of their constellation, makes this chip capable of delivering exceptional accuracy in urban canyons and in the environments where buildings and other obstructions make satellite visibility challenging.

STA8090FG embeds innovative power management with switching regulator for power consumption optimization.

The extended voltage supply ranges from 1.6 V to 4.3 V, the 1.8 V and 3.3 V I/O compliance support makes the STA8090FG the suitable solution for different user applications.

The STA8090FG combines a high performance ARM946 microprocessor with I/O capabilities and enhanced peripherals. It supports USB2.0 standard at full speed (12 Mbps) with on-chip PHY.

The chip embeds backup logic with real time clock.

STA8090FG can host customer code on top of STMicroelectronics GNSS library.

Customers can develop on TeseoIII their application code by using a software development kit based on different real time operating systems.

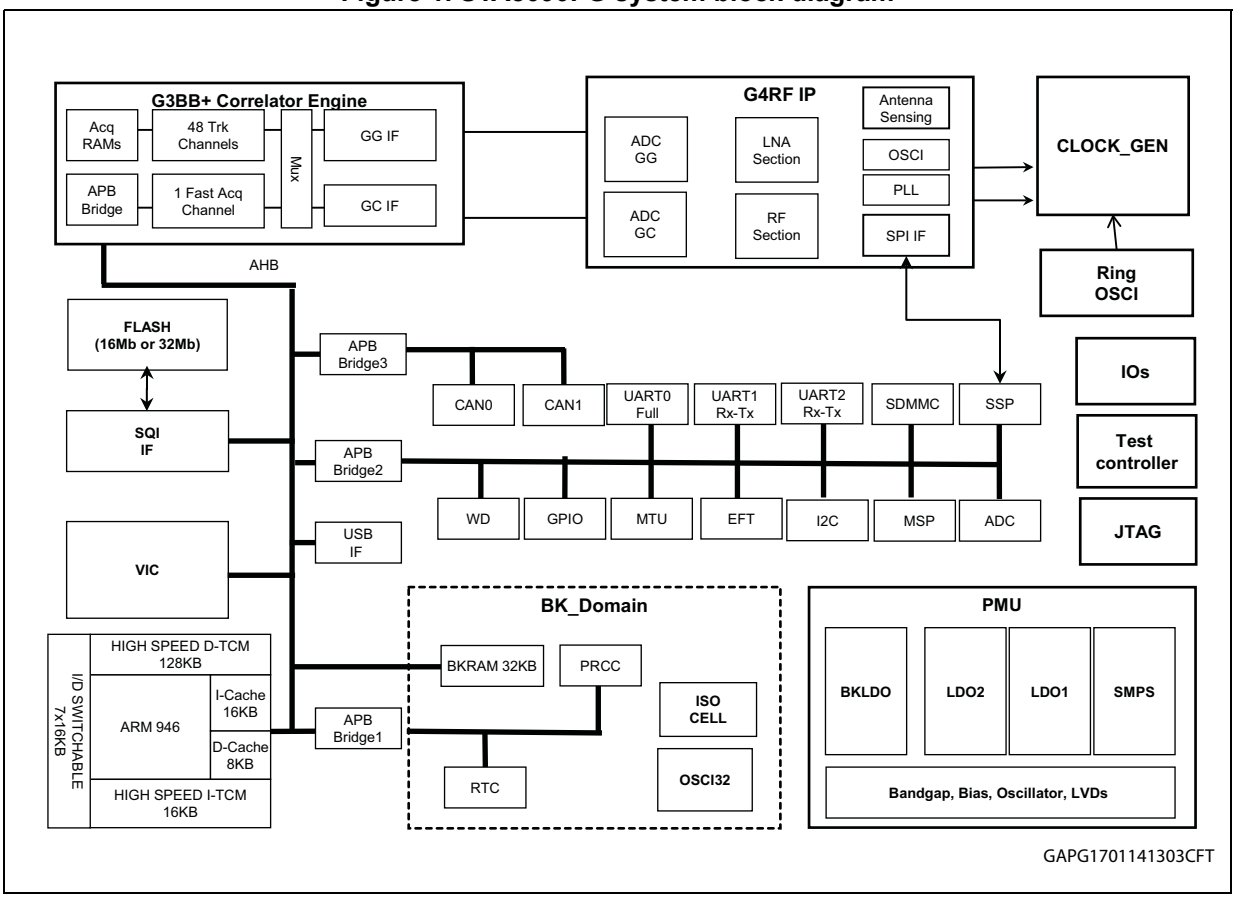
STA8090FGBD can be offered also bundled with STMicroelectronics dead reckoning firmware called TESEO-DRAW; TESEO-DRAW firmware is a multi-sensors data fusion hub for Teseo family IC's.

The STA8090FG, using STMicroelectronics CMOSRF Technology, is housed in a TFBGA99 (5 x 6 x 1.2 mm) package with stacked 16 Mbit or 32 Mbit Flash memory.

2 Pin description

2.1 Block diagram

Figure 1. STA8090FG system block diagram



2.2 TFBGA99 pin configuration

Table 2. TFBGA99 connection diagram (with CAN)

	1	2	3	4	5	6	7	8	9
A	VINM	VINM	SPI_CLK	SPI_CSN	VINL1	VOL1	GND	VINB	VOB
B	VLX	VLX	SPI_DI	UART0_ TX	UART0_ CTS	UART2_ RX	GPIO1	GPIO0	GND
C	GND	GND	SPI_DO	VDDIO_ R1	UART2_ TX	UART0_ RTS	VDD_SQI	VDD_ ADC	Reserved
D	VOM	GND	TMS	UART0_ DSR	UART0_ DTR	GND	ADC_IN2	GND	RTC_XTO
E	VDD_ANA	TDO	TRSTn	UART0_ DCD	VDDD	UART0_ RX	ADC_IN1	WAKEUP0	RTC_XTI
F	GND	TDI	VDDD	VDDD	GND	GND	WAKEUP1	STDBYn	RSTn
G	USB_DP	TCK	VDDD	GND	GND	GND	STDBY_ OUT	PMU_ CFG	XTAL_ OUT
H	USB_DM	GPIO10	MMC_D3	MMC_ CLK	TP_IF_N	GND	GND	VCC_PLL	XTAL_IN
J	CAN0_TX	GPIO11	MMC_D2	MMC_ CMD	TP_IF_P	GND	GND	ANT_ SENSE2	VCC_ CHAIN
K	CAN0_RX	VDDIO_ R2	GPIO2	MMC_D1	GND_LNA	GND_LNA	GND_LNA	GND	ANT_ SENSE1
L	GND	I2C_SD	I2C_CLK	MMC_D0	VCC_RF	LNA_IN	VOL2	VINL2	GND

Table 3. TFBGA99 connection diagram (no CAN)

	1	2	3	4	5	6	7	8	9
A	VINM	VINM	SPI_CLK	SPI_CSN	VINL1	VOL1	GND	VINB	VOB
B	VLX	VLX	SPI_DI	UART0_ TX	UART0_ CTS	UART2_ RX	GPIO1	GPIO0	GND
C	GND	GND	SPI_DO	VDDIO_ R1	UART2_ TX	UART0_ RTS	VDD_SQI	VDD_ ADC	Reserved
D	VOM	GND	TMS	UART0_ DSR	UART0_ DTR	GND	ADC_IN2	GND	RTC_XTO
E	VDD_ANA	TDO	TRSTn	UART0_ DCD	VDDD	UART0_ RX	ADC_IN1	WAKEUP0	RTC_XTI
F	GND	TDI	VDDD	VDDD	GND	GND	WAKEUP1	STDBYn	RSTn
G	USB_DP	TCK	VDDD	GND	GND	GND	STDBY_ OUT	PMU_ CFG	XTAL_ OUT
H	USB_DM	GPIO10	MMC_D3	MMC_ CLK	TP_IF_N	GND	GND	VCC_PLL	XTAL_IN
J	UART0_ TX	GPIO11	MMC_D2	MMC_ CMD	TP_IF_P	GND	GND	ANT_ SENSE2	VCC_ CHAIN
K	UART0_ RX	VDDIO_ R2	GPIO2	MMC_D1	GND	GND	GND	GND_LNA	ANT_ SENSE1
L	GND	I2C_SD	I2C_CLK	MMC_D0	VCC_RF	LNA_IN	VOL2	VINL2	GND

2.3 Power supply pins

Table 4. Power supply pins

Symbol	I/O voltage	I/O	Description	STA8090FG
VCC_CHAIN	1.2 V	PWR	Analog supply voltage for RF chain (1.2V)	J9
VCC_PLL	1.2 V	PWR	Analog supply voltage for PLL RF (1.2V)	H8
VCC_RF	1.2 V	PWR	Analog supply voltage for RF (1.2V)	L5
VDD_ADC	1.8 V	PWR	Digital supply voltage for ADC (1.8V)	C8
VDD_SQI	1.8 V	PWR	Digital supply voltage for SQI	C7
VDDD	1.1 V	PWR	Digital supply voltage	E5, F3, F4, G3
VDDIO_R1	1.8 V or 3.3 V	PWR	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	C4
VDDIO_R2	3.3V	PWR	Digital supply voltage for I/O ring 2 (3.3 V)	K2
VINB	1.6 V - 4.3 V	PWR	Backup LDO input supply voltage (1.6 V to 4.3 V)	A8
VINL1	1.6 V - 4.3 V	PWR	LDO1 input supply voltage (1.6 V to 4.3 V)	A5
VINL2	1.6 V - 4.3 V	PWR	LDO2 input supply voltage (1.6 V to 4.3 V)	L8

Table 4. Power supply pins (continued)

Symbol	I/O voltage	I/O	Description	STA8090FG
VINM	1.6 V - 4.3 V	PWR	SMPS coil input supply (1.6 V to 4.3 V)	A1, A2
VDD_ANA	1.6 V - 4.3 V	PWR	SMPS input supply (1.6 V to 4.3 V)	E1
VLX	0 V - 4.3 V	PWR	SMPS coil output	B1, B2
VOB	1.0V	PWR	LDO backup output voltage (1.0 V)	A9
VOL1	1.1 V or 1.8 V	PWR	LDO1 output voltage: PMU_CFG = high -> 1.1 V (it can be also configured to 1.2 V) PMU_CFG = low -> 1.8 V	A6
VOL2	1.2 V	PWR	LDO2 output voltage (1.2 V)	L7
VOM	1.1 V or 1.8 V	PWR	SMPS output voltage PMU_CFG = high -> 1.8 V PMU_CFG = low -> 1.1 V (it can be also configured to 1.2 V)	D1
GND	GND	GND	Ground	A7, B9, C1, C2, D2, D6, D8, F1, F5, F6, G4, G5, G6, H6, H7, J6, J7, K8, L1, L9
GND_LNA	GND	GND	Ground	K5, K6, K7

2.4 Main function pins

Table 5. Main function pins

Symbol	I/O voltage	I/O	Description	STA8090FG
ADC_IN1	1.4 V – 0 V typ range	I	ADC Analog input [1]	E7
ADC_IN2	1.4 V – 0 V typ range	I	ADC Analog input [2]	D7
PMU_CFG	1.0 V	I	Power management unit config pin High -> VOL1 = 1.1 V, VOM = 1.8 V Low -> VOL1 = 1.8 V, VOM = 1.1 V	G8
RSTn	1.0 V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	F9
RTC_XTI	1.0 V (max)	I	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	E9
RTC_XTO	1.0 V (max)	O	Output of the oscillator amplifier circuit.	D9
STDBY_OUT	1.0 V	O	When low, indicates the chip is in Standby mode	G7
STDBYn	1.0 V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	F8

Table 5. Main function pins (continued)

Symbol	I/O voltage	I/O	Description	STA8090FG
WAKEUP0	1.0 V	I	WAKEUP from STANDBY mode	E8
WAKEUP1	1.0 V	I	WAKEUP from STANDBY mode	F7

2.5 Test/emulated dedicated pins

Table 6. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Description	STA8090FG
TCK	VDDIO_R2	I	JTAG Test Clock	G2
TDI	VDDIO_R2	I	JTAG Test Data In	F2
TDO	VDDIO_R2	O	JTAG Test Data Out	E2
TMS	VDDIO_R2	I	JTAG Test Mode Select	D3
TRSTn	VDDIO_R2	I	JTAG Test Circuit Reset	E3
TP_IF_N	1.2 V	O	Diff.Test Point for IF – Negative	H5
TP_IF_P	1.2 V	O	Diff.Test Point for IF – Positive	J5

2.6 Communication interface pins

Table 7. Communication interface pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
CAN0_RX(1)	VDDIO_R2	I	AF0 (default)	CAN0_RX(1)	CAN0 receive data input	K1
		I	AF1	UART0_RX	UART0 Rx data	
		I	AF2	Tsense	External temperature capture port	
		I/O	AF3	I2C_SD	I2C serial data	
CAN0_TX(1)	VDDIO_R2	O	AF0 (default)	CAN0_TX(1)	CAN0 transmit data output	J1
		O	AF1	UART0_TX	UART0 Tx data	
		I/O	AF2	GPIO7	General purpose I/O #7	
		O	AF3	I2C_CLK	I2C clock	
I2C_CLK	VDDIO_R2	O	AF0 (default)	I2C_CLK	I2C clock	L3
		I/O	AF1	GPIO8	General purpose I/O #8	
		O	AF2	CAN1_TX(1)	CAN1 transmit data output	
		O	AF3	SPI_CLK	SPI clock	

Table 7. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
I2C_SD	VDDIO_R2	I/O	AF0 (default)	I2C_SD	I2C serial data	L2
		I/O	AF1	GPIO9	General purpose I/O #9	
		I	AF2	CAN1_RX(1)	CAN1 receive data input	
		O	AF3	SPI_CSN	SPI chip select active low	
SPI_CLK	VDDIO_R1	O	AF0 (default)	SPI_CLK	SPI clock	A3
		I/O	AF1	GPIO25	General purpose I/O #25	
		O	AF2	SQI_CLK	SQI Flash clock	
		O	AF3	MMC_CLK	Multimedia Clock line	
SPI_CSN	VDDIO_R1	O	AF0 (default)	SPI_CSN	SPI chip select active low / IO_Power Sel Ring 1	A4
		I/O	AF1	GPIO24	General purpose I/O #24	
		O	AF2	SQI_CEN	SQI Flash chip enable	
		I/O	AF3	MMC_CMD	Multimedia card command line	
SPI_DI	VDDIO_R1	I	AF0 (default)	SPI_DI	SPI serial data input / BOOT2	B3
		I/O	AF1	Tsense	External temperature capture port	
		I/O	AF2	SQI_SIO1/SO	SQI Flash data IO 1 / ser. output	
		I/O	AF3	MMC_D0	Multimedia card data 0	
SPI_DO	VDDIO_R1	O	AF0 (default)	SPI_DO	SPI serial data output	C3
		I/O	AF1	GPIO27	General purpose I/O #27	
		I/O	AF2	SQI_SIO0/SI	SQI Flash data IO 0 / ser. input	
		I/O	AF3	MMC_D1	Multimedia card data 1	
UART0_CTS	VDDIO_R1	I	AF0 (default)	UART0_CTS	UART0 clear to send	B5
		I/O	AF1	GPIO15	General purpose I/O #15	
		O	AF2	i2s_out_sclk	MSP serial clock output	
		O	AF3	Clock GNSS	GNSS clock out	
UART0_DCD	VDDIO_R1	I	AF0 (default)	UART0_DCD	UART0 data carrier detect	E4
		I/O	AF1	GPIO17	General purpose I/O #17	
		O	AF2	i2s_out_sdata	MSP serial data output	
		O	AF3	Clock GNSS	GNSS clock out	

Table 7. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
UART0_DSR	VDDIO_R1	I	AF0 (default)	UART0_DSR	UART0 data set ready	D4
		I/O	AF1	GPIO16	General purpose I/O #16	
		O	AF2	i2s_out_lrclk	MSP left/right clock output	
		O	AF3	Sign GC	GLONASS and BeiDou 3-bit coding output (Sign)	
UART0_DTR	VDDIO_R1	O	AF0 (default)	UART0_DTR	UART0 data terminal read	D5
		I/O	AF1	GPIO18	General purpose I/O #18	
		I	AF2	Timer_ICAPA	Extended function timer - input capture A	
		O	AF3	Mag_1 GG	GPS and Galileo 3-bit coding Output (MAG1)	
UART0_RTS	VDDIO_R1	O	AF0 (default)	UART0_RTS	UART0 request to send	C6
		I/O	AF1	GPIO14	General purpose I/O #14	
		O	AF2	TCXO_OUT	TCXO out clock	
		O	AF3	Sign GG	GPS and Galileo 3-bit coding output (Sign)	
UART0_RX	VDDIO_R1	I	AF0 (default)	UART0_RX	UART0 Rx data	E6
		O	AF1	SPI_DO	SPI serial data output	
		I/O	AF2	SQI_SIO2	SQI Flash data IO 2	
		I	AF3	Timer_ICAPA	Extended Function Timer - Input Capture A	
UART0_TX	VDDIO_R1	O	AF0 (default)	UART0_TX	UART0 Tx data / BOOT1	B4
		I	AF1	SPI_DI	Serial data input	
		I/O	AF2	SQI_SIO3	SQI Flash data IO 3	
		O	AF3	Timer_OCMPA	Extended Function Timer – Output Compare A	
UART2_RX	VDDIO_R1	I	AF0 (default)	UART2_RX	UART 2 Rx data	B6
		I/O	AF1	GPIO28	General purpose I/O #28	
		I/O	AF2	I2C_SD	I2C serial data	
		I/O	AF3	MMC_D2	Multimedia card data 2	

Table 7. Communication interface pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
UART2_TX	VDDIO_R1	O	AF0 (default)	UART2_TX	UART 2 Tx data / BOOT0	C5
		I/O	AF1	GPIO29	General purpose I/O #29	
		O	AF2	I2C_CLK	I2C clock	
		I/O	AF3	MMC_D3	Multimedia card data 2	
USB_DM	VDDIO_R2	USB	AF0	USB_DM	USB D- signal	H1
		I	AF1 (default)	UART1_RX	UART1 Rx data	
		I	AF2	CAN1_RX(1)	CAN1 receive data input	
		I/O	AF3	I2C_SD	I2C serial data	
USB_DP	VDDIO_R2	USB	AF0	USB_DP	USB D+ signal	G1
		O	AF1 (default)	UART1_TX	UART1 Tx data	
		O	AF2	CAN1_TX(1)	CAN1 transmit data output	
		O	AF3	I2C_CLK	I2C clock	

1. Only for STA8090FGB and STA8090FGBD.

2.7 Multimedia card pins

Table 8. Multimedia card pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
MMC_CLK	VDDIO_R2	O	AF0 (default)	MMC_CLK	Multimedia Clock line	H4
		O	AF1	i2s_out_lrclk	MSP left/right clock output	
		I	AF2	Timer_ICAPA	Extended Function Timer - Input Capture A	
		I/O	AF3	GPIO4	General purpose I/O #4	
MMC_CMD	VDDIO_R2	I/O	AF0 (default)	MMC_CMD	Multimedia card command line	J4
		O	AF1	i2s_out_sdata	MSP serial data output	
		O	AF2	CAN0_TX(1)	CAN0 transmit data output	
		I/O	AF3	GPIO5	General purpose I/O #5	

Table 8. Multimedia card pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
MMC_D0	VDDIO_R2	I/O	AF0 (default)	MMC_D0	Multimedia card data 0	L4
		O	AF1	i2s_out_sclk	MSP serial clock output	
		I/O	AF2	I2C_SD	I2C serial data	
		I/O	AF3	GPIO20	General purpose I/O #20	
MMC_D1	VDDIO_R2	I/O	AF0 (default)	MMC_D1	Multimedia card data 1	K4
		I	AF1	i2s_in_sdata	MSP serial data input	
		O	AF2	Sign GC	GLONASS and BeiDou 3-bit coding output (Sign)	
		I/O	AF3	GPIO21	General purpose I/O #21	
MMC_D2	VDDIO_R2	I/O	AF0 (default)	MMC_D2	Multimedia card data 2	J3
		I/O	AF1	Reserved	Reserved	
		I	AF2	CAN0_RX(1)	CAN0 receive data input	
		I/O	AF3	Tsense	External temperature capture port	
MMC_D3	VDDIO_R2	I/O	AF0 (default)	MMC_D3	Multimedia card data 2	H3
		I/O	AF1	Reserved	Reserved	
		O	AF2	Sign GG	GPS 3-bit coding output (Sign)	
		I/O	AF3	GPIO23	General purpose I/O #23	

1. Only for STA8090FGB.

2.8 General purpose pins

Table 9. General purpose pins

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
GPIO0	VDDIO_R1	I/O	AF0 (default)	GPIO0	General purpose I/O #0	B8
		I	AF1	PPS_IN	Pulse per second input	
		O	AF2	Timer_OCMPB	Extended Function Timer – Output Compare B	
		O	AF3	Mag_0 GC	GLONASS and BeiDou 3-bit coding Output (MAG0)	

Table 9. General purpose pins (continued)

Symbol	I/O voltage	I/O	Alternative function	Function	Description	STA8090FG
GPIO1	VDDIO_R1	I/O	AF0 (default)	GPIO1	General purpose I/O #1 / BOOT3	B7
		I	AF1	i2s_in_sdata	MSP serial data input	
		O	AF2	PPS_OUT	Pulse per second output	
		I/O	AF3	Tsense	External temperature capture port	
GPIO2	VDDIO_R2	I/O	AF0 (default)	GPIO2	General purpose I/O #2	K3
		I/O	AF1	Reserved	Reserved	
		I	AF2	Timer_ICAPB	Extended Function Timer – Input Capture B	
		O	AF3	Mag_1 GC	GLONASS and BeiDou 3-bit coding Output (MAG1)	
GPIO10	VDDIO_R2	I/O	AF0 (default), AF1	GPIO10	General purpose I/O #10	H2
		I	AF2	Timer_ICAPA	Extended Function Timer – Input Capture A	
		O	AF3	Timer_OCMPB	Extended Function Timer – Output Compare B	
GPIO11	VDDIO_R2	I/O	AF0 (default), AF1	GPIO11	General purpose I/O #11	J2
		O	AF2	Timer_OCMPA	Extended Function Timer – Output Compare A	
		I	AF3	Timer_ICAPB	Extended Function Timer – Input Capture B	

2.9 RF Front-end pins

Table 10. RF Front-end pins

Symbol	I/O voltage	I/O	Description	STA8090FG
ANT_SENSE1	3.3 V	I	Antenna sensing input 1	K9
ANT_SENSE2	3.3 V	I	Antenna sensing input 2	J8
LNA_IN	1.2 V	I	Low Noise Amplifier Input	L6
XTAL_IN	1.2 V	I	Input Side of Crystal Oscillator or TCXO Input	H9
XTAL_OUT	1.2 V	O	Output Side of Crystal Oscillator	G9

3 General description

3.1 RF front end

The RF front-end is able to down-convert both the GPS-Galileo signal from 1575.42 MHz to 4.092 MHz (4 Fo, being F0 = 1.023 MHz), the GLONASS signal from 1601.718 MHz to 8.57 MHz and the BeiDou signal from 1561.098 MHz to 10.23 MHz.

It embeds high performance LNA minimizing external component count and two LDOs to supply the internal core facilitating requirements for external power supply. A three bits ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 64 Fo sampling clock for the baseband and 192 Fo clock for MCU subsystem.

3.2 GPS/Galileo/GLONASS/BeiDou Base Band (G3BB+) processor

STA8090FG integrates G3BB+ proprietary IP, which is the ST last generation high-sensitivity Baseband processor fully compliant with GPS, Galileo, GLONASS and BeiDou systems.

The baseband receives, from the embedded RF Front-End, two separate IF signals coded in sign-magnitude digital format on 3 bits and the related clocks. The Galileo/GPS (GALGPS) and GLONASS/BeiDou (GNSCOM) signals at the base band inputs are centered on 4.092 MHz, 8.57 MHz and 10.23 MHz.

The baseband processes the two IF signals performing data codification, sample rate conversion and final frequency conversion to zero IF before acquisition and tracking correlations.

The baseband processor has the capability of acquiring and tracking the Galileo, GPS, GLONASS and BeiDou signals in a simultaneous or single way, or a combination of three, being GLONASS and BeiDou mutually exclusive. The number of tracking channels to be used is programmable; the unused tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format or in a ST binary format. The library includes support of ST self-trained assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with autonomous and server-based ephemeris prediction and extension.

3.3 MCU Subsystem

The implemented sub-system includes an AHB Lite bus matrix.

An ARM946 core is embedded in the sub-system and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be

configured by the ARM946 (see *Table 11: TCM Configuration*). ITCM can be configured as Ni x 16 KB; DTCM can be configured as 128 + Nd x 16 KB, where Ni + Nd = 8, Ni ≥ 1.

Table 11. TCM Configuration

TCMcfg [2]	TCMcfg [1]	TCMcfg [0]	ITCM	DTCM
0	0	0	16 KB	240 KB
0	0	1	32 KB	224 KB
0	1	0	48 KB	208 KB
0	1	1	64 KB	192 KB
1	0	0	80 KB	176 KB
1	0	1	96 KB	160 KB
1	1	0	112 KB	144 KB
1	1	1	128 KB	128 KB

3.3.1 AHB slaves

- G3 APB port that allows to interface with the G3BB acquisition memory and control registers.
- 512 Kbytes ROM
- Vectored Interrupt Controller (VIC).
- SQI flash memory controller
- 3 x ARM946 APB peripheral bus (APB1, APB2, APB3).

Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 64 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ.

The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

FS USB device controller

Full speed USB device with transceiver.
It is an AHB slave. When active it requires a 48 MHz clock XTAL_IN.

3.4 APB peripherals

3.4.1 CAN

The 2 CAN[(a)] cores perform communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

CAN consists of the CAN core, message RAM, message handler, control registers and module. For communication on a CAN network, individual message objects are configured. The message objects and identifier masks for acceptance filtering of received messages are stored in the message RAM. All functions concerning the handling of messages are implemented in the message handler. These functions include acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN can be accessed directly by the CPU through the module interface. These registers are used to control/configure the CAN core and the message handler and to access the message RAM.

CAN features

- Supports CAN protocol version 2.0 part A and B
- 32 messages objects
- Each message object has its own identifier mask
- Maskable interrupt
- Disabled automatic re-transmission mode for time triggered CAN applications
- Programmable loop-back mode for self-test operation
- Two 16-bit module interfaces to the AMBA APB bus from ARM

3.4.2 SSP

The SSP is a master interface for synchronous serial communication with peripheral devices that have Motorola SPI.

The SSP performs serial-to-parallel conversion on data received from a peripheral device on SPI_DI pin, and parallel-to-serial conversion on data written by CPU for transmission on SPI_DO pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 32 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO.

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SSPCLK from the on-chip clock. One combined interrupt is delivered, which is asserted from several internal maskable events.

a. STA8090FGB and STA8090FGBD only (see *Figure 5: Ordering information scheme*).

SSP features

The SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep
- transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location
- deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode

3.4.3 UART

The UARTx (x = 0|1|2) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

UART features

The UARTx (x = 0|1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to UARTCLK / 16 (1.5 Mbps with UARTCLK at 24 MHz), or up to UARTCLK / 8 (3.0 Mbps with UARTCLK at 24 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8 bits of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Support of the modem control functions CTS, RTS, plus DCD, DSR, RTS, DTS and RI (UART0 only)
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

3.4.4 Flash

The STA8090FG integrates 16 Mbits or 32 Mbits of Flash Memory. This eliminates the need of the external Flash simplifying the routing associated to integrate a GPS receiver into a customer board.

3.4.5 SDMMC

STA8090FG features an SD/MMC host.

3.4.6 MTU

The 2 Multi Timer Units provide access to eight interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in each MTU, allowing eight counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

3.4.7 WDT

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (WDOGINT), depending on a programmed value.

The watchdog monitors the interrupt and asserts a reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. You can enable or disable the watchdog unit as required.

Note: Watchdog is stalled when the ARM processor is in Debug mode.

3.4.8 GPIO

The GPIO block provides twenty-one (21) programmable inputs or outputs. Each input or output can be controlled in two modes:

- software mode through an APB bus interface
- alternate mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

3.4.9 ADC

10 bit SAR ADC operating at 1.8 V analog supply. It can convert up to 2 single ended channels with analog input multiplexer at 500KSPS

3.4.10 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 32 Kbyte SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed

alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer+fractional part) to the 47-bit counter. Once set by the MCU this bits is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.4.11 MSP

The STA8090FG provides one MSP transmitter block.

- Element (data) size from 8 to 32 bits, LSB or MSB first
- Programmable frequency shift clock for data transfer
- Direct interface to:
  - Industry-standard codecs and serially connected A/D and D/A devices
  - IIS compliant devices
  - SPI compliant devices
- Transmit first-in, first-out memory buffers (FIFOs), 32 bits wide, 8 locations deep

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C.

4.3 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{ddio} = 1.8 V, V_{dd} = 1.20 V. They are given only as design guidelines and are not tested.

4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 12 lists the absolute maximum rating for STA8090FG.

Table 12. Voltage characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{CC_CHAIN}	Analog supply voltage for RF chain (1.2 V)	-0.3	1.32	V
V_{CC_PLL}	Analog supply voltage for PLL RF (1.2 V)	-0.3	1.32	V
V_{CC_RF}	Analog supply voltage for RF (1.2 V)	-0.3	1.32	V
V_{DD_ADC}	Digital supply voltage for ADC (1.8 V)	-0.3	1.98	V
V_{DD_SQI}	Digital supply voltage for SQI	-0.3	1.95	V
V_{DDD}	Power supply pins for the core logic.	-0.3	1.32	V
V_{DDIO_R1}	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	-0.3	3.63	V
V_{DDIO_R2}	Digital supply voltage for I/O ring 2 (3.3 V)	-0.3	3.63	V
V_{INB}	Backup LDO input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
V_{INL1}	LDO1 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V

Table 12. Voltage characteristics (continued)

Symbol	Parameter	Min.	Max.	Unit
V_{INL2}	LDO2 input supply voltage (1.6 V to 4.3 V)	-0.3	4.8	V
V_{INM}	SMPS coil input supply (1.6 V to 4.3 V)	-0.3	4.8	V
V_{DD_ANA}	SMPS input supply (1.6 V to 4.3 V)	-0.3	4.8	V
$V_{ESD\text{-}HBM}$	Electrostatic discharge, human body model(1).	-2	2	kV
$V_{ESD\text{-}CDM}$	Electrostatic discharge, charge device model(2).	-250	250	V

1. Balls sustaining only ±500 V are: A1, A2, A5, A6, A7, A8, A9, B1, B2, B9, C1, C2, D1, D2, D9, E1, E9, F1, L7 and L8.
2. Ball L6 (LNA_IN) sustains only ±150 V.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13. Thermal characteristics

Symbol	Parameter	Min.	Max.	Unit
T_{oper}	Operative temperature range	-40	85	°C
T_j	Operative junction temperature	-40	125	°C
T_{st}	Storage temperature	-55	150	°C
$R_{j\text{-}amb}$	Thermal resistance junction to ambient(1)		41	°C/W

1. According to JEDEC specification on a 2 layers board.

Table 14. Frequency limits

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{CLK}	Operating ARM9 CPU frequency	V_{DDD} = 1.2 V; T_C = 85 °C(1)	—	—	196	MHz
F_{AHB}	AHB frequency		—	—	49	MHz

1. Not tested in production.

Table 15. Power consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
P_{RF}	RFIP power (total V_{INL2})	G2 = GPS/Galileo; T_{amb} = 25 °C; V_{INL2} = 1.8 V	—	25		mW
		G2 + GLONASS; T_{amb} = 25 °C; V_{INL2} = 1.8 V	—	35		mW
		G2 + COMPASS; Beidou2 T_{amb} = 25 °C; V_{INL2} = 1.8 V	—	35		mW
P_{MVR}(1)	Switchable area power; (total V_{INL1})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INL1} = 1.8 V; UART active; other peripherals inactive	—	90		mW
P_{LPVR}(1)	Always ON area power (total V_{INB})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INB} = 3.3 V	—	1		mW
P_{IO}(1)	IO rings power (total V_{DDIO_R1} + V_{DDIO_R2})	f_{ARM} = 196 MHz; f_{AHB} = 49 MHz; T_{amb} = 25 °C; V_{INL1} = 1.8 V; UART active; other peripherals inactive	—	4		mW
$I_{DStandby}$	Standby mode supply current	RTC running = 32.768 KHz; T_{amb} = 25 °C; V_{INB} = 1.8 V	—	29	—	µA
$I_{DDeepStandby}$	Deep standby mode supply current(2)		—	7	—	µA

1. Not tested in production.
2. STDBY_OUT pin not supported in deep standby.

4.6 Recommended DC operating conditions

Table 16 lists the functional recommended operating DC parameters for STA8090FG.

Table 16. Recommended DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC_CHAIN}	Analog supply voltage for RF chain (1.2 V)	1.08	1.20	1.32	V
V_{CC_PLL}	Analog supply voltage for PLL RF (1.2 V)	1.08	1.20	1.32	V
V_{CC_RF}	Analog supply voltage for RF (1.2 V)	1.08	1.20	1.32	V
V_{DD_ADC}	Digital supply voltage for ADC (1.8 V)	1.71	1.80	1.89	V
V_{DD_SQI}	Flash power supply.	1.71	1.80	1.89	V

Table 16. Recommended DC operating conditions (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDD}	Power supply pins for the core logic.	1.00	1.10	1.32	V
V_{DDIO_R1}	Digital supply voltage for I/O ring 1 (1.8 V)	1.71	1.80	1.89	V
	Digital supply voltage for I/O ring 1 (3.3 V)	3.00	3.30	3.60	V
V_{DDIO_R2}	Digital supply voltage for I/O ring 2 (3.3 V)	3.00	3.30	3.60	V
V_{INB}	Backup LDO input supply voltage (1.6 V to 4.3 V)	1.60		4.30	V
V_{INL1}	LDO1 input supply voltage to generate 1.1 V and 1.2 V	1.60		4.30	V
	LDO1 input supply voltage to generate 1.8 V	2.10		4.30	V
V_{INL2}	LDO2 input supply voltage to generate 1.2 V	1.60		4.30	V
V_{INM}	SMPS coil input supply voltage to generate 1.1 V and 1.2 V	1.60		4.30	V
	SMPS coil input supply voltage to generate 1.8 V	2.10		4.30	V
V_{DD_ANA}	SMPS input supply (1.6 V to 4.3 V)	1.60		4.30	V
T_C	Operating temperature range	-40		85	°C

4.7 DC characteristics

Table 17 specifies the SMPS voltage regulator characteristics.

Table 17. SMPS DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OM}	Output voltage (1.2 V)	1.6 V ≤ V_{INM} ≤ 4.3 V; I_{OM} ≤ 100 mA	1.08	1.20	1.32	V
	Output voltage (1.1 V)	1.6 V ≤ V_{INM} ≤ 4.3 V; I_{OM} ≤ 100 mA	1.0	1.10	1.21	V
	Output voltage (1.8 V)	2.1 V ≤ V_{INM} ≤ 4.3 V; I_{OM} ≤ 100 mA	1.71	1.80	1.89	V
I_{OM}	Output current		0	—	100	mA

Table 18 specifies the LDO1 voltage regulator characteristics.

Table 18. LDO1 DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL1}	Output voltage (1.2V)	1.6 V ≤ V_{INL1} ≤ 4.3 V; I_{OL1} ≤ 70 mA	1.08	1.20	1.32	V
	Output voltage (1.1V)	1.6 V ≤ V_{INL1} ≤ 4.3 V; I_{OL1} ≤ 70 mA	1	1.10	1.21	V
	Output voltage (1.8V)	2.1 V ≤ V_{INL1} ≤ 4.3 V; I_{OL1} ≤ 70 mA	1.71	1.80	1.89	V
I_{OL1}	Output current		0	—	70	mA

Table 19 specifies the LDO2 voltage regulator characteristics.

Table 19. LDO2 DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL2}	Output voltage	1.6 V ≤ V_{INL2} ≤ 4.3 V; I_{OL2} ≤ 30 mA	1.08	1.20	1.32	V
I_{OL2}	Output current		0	—	30	mA

Table 20 specifies the low voltage detection thresholds

Table 20. Low voltage detection thresholds

Parameter		Min.	Typ.	Max.	Unit
Input LVD always on and main VRs(1)	Upper voltage threshold	—	1.680	—	V
	Lower voltage threshold	—	1.650	—	V
Output LVD always on VR(1)	Upper voltage threshold	—	0.995	—	V
	Lower voltage threshold	—	0.935	—	V
Output LVD main VR(1)	Upper voltage threshold @ $V_{OL1/M}$ = 1.2 V	—	1.142	—	V
	Lower voltage threshold @ $V_{OL1/M}$ = 1.2 V	—	1.076	—	V
	Upper voltage threshold @ $V_{OL1/M}$ = 1.1 V	—	1.048	—	V
	Lower voltage threshold @ $V_{OL1/M}$ = 1.1 V	—	0.986	—	V
Output LVD main VR(1)	Upper voltage threshold @ $V_{OL1/M}$ = 1.8 V	—	1.645	—	V
	Lower voltage threshold @ $V_{OL1/M}$ = 1.8 V	—	1.626	—	V

1. Not tested in production.

Table 21 lists the DC characteristics for all the IO digital buffers expect for the following input buffers: STBYn (F8), STDBY_OUT (G7), WAKEUP0 (E8), WAKEUP1 (F7), PMU_CFG (G8) and RSTn (F9).

Table 21. I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}(1)	Logical input low level voltage	V_{DDIO} = 1.8 V	-0.3	—	0.3 * V_{DDIO}	V
		V_{DDIO} = 3.3V	-0.3	—	0.8	V
V_{IH}(1)	Logical input high level voltage	V_{DDIO} = 1.8 V	0.7 * V_{DDIO}	—	V_{DDIO} + 0.3	V
		V_{DDIO} = 3.3V	2.0	—	V_{DDIO} + 0.3	V
V_{HYST}(2)	Schmitt-trigger hysteresis	–	50	—		mV
V_{OL}	Low level output voltage	V_{DDIO} = 1.8 V		—	0.4	V
		V_{DDIO} = 3.3V		—	0.4	V
V_{OH}	High level output voltage	V_{DDIO} = 1.8 V	V_{DDIO} - 0.4	—		V
		V_{DDIO} = 3.3V	V_{DDIO} - 0.4	—		V

1. Excludes oscillator inputs RTC_XTI and XTAL_IN. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.

Table 22 lists the DC characteristics for the 1.0 V IO digital buffers input buffers: STBYn (F8), STDBY_OUT (G7), WAKEUP0 (E8), WAKEUP1 (F7), PMU_CFG (G8) and RSTn (F9).

Table 22. 1.0 V I/O buffers DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logical input low level voltage	V_{OB} = 1.0 V	-0.3	—	0.35 * V_{OB}	V
V_{IH}	Logical input high level voltage	V_{OB} = 1.0 V	0.65 * V_{OB}	—	V_{OB} + 0.3	V
V_{OL}	Low level output voltage	V_{OB} = 1.0 V		—	0.2	V
V_{OH}	High level output voltage	V_{OB} = 1.0 V	V_{OB} - 0.2	—		V

4.8 AC characteristics

4.8.1 RF electrical specifications

Table 23. RFACHAIN – GALGPS filter and VGA

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
S11(1)	Input return loss	GPS band	—	-8		dB
f_{IF}	IF frequency	PLL in default condition with 26Mhz as reference	—	4.045		MHz
NF	Noise figure	NF overall chain with AGC set at 0 dB	—	2(1)		dB
C_G	Conversion gain from RF input to ADC input	VGA at max gain	—	119		dB
		VGA at min gain	—	69		dB

Table 23. RFACHAIN – GALGPS filter and VGA (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
IP_{1dB}	RF-IF-VGA input compression point	VGA min	—	-80		dBm
IRR	Image rejection ratio		—	20		dB
BW_{GPS}	-3dB IF bandwidth	GPS mode	—	2.4		MHz
BW_{GAL}		Galileo mode	—	4.8		MHz
ATT	Alias frequency rejection	F = 60 MHz (fs = 65.474 MHz)	—	30		dB
T_{gGPS}	IF filter group delay variation	GPS mode	—		200(1)	ns
T_{gGAL}		Galileo mode	—		30(1)	ns

1. Not tested in production.

Table 24. RFCHAIN – GLONASS/BeiDou filter and VGA

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$S11^{(1)}$	Input return loss	GLONASS band		-10		dB
		BeiDou band		-7		
$f_{IFGNS/BDU}$	IF frequency for GLONASS	PLL in default condition with 26 Mhz as reference	—	8.519		MHz
	IF frequency for BeiDou		—	10.277		
NF	Noise figure	NF overall chain with AGC set at 0 dB	—	$2^{(1)}$		dB
C_G	Conversion gain from RF input to ADC input	VGA at max gain	—	118		dB
		VGA at min gain	—	68		dB
IP_{1dB}	RF-IF-VGA input compression point	VGA min	—	-80		dBm
IRR	Image rejection ratio		—	25		dB
$BW_{GNS/BDU}$	-3dB IF bandwidth		—	10		MHz
ATT	Alias frequency rejection	F = 53 MHz (fs = 65.474 MHz)	—	30		dB
$T_{gGNS/BDU}$	IF filter group delay variation		—		$20^{(1)}$	ns

1. Not tested in production.

Table 25. Synthesizer

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{TCXO_XTAL}	Input frequency for xtal amplifier $^{(1)}$	10		52	MHz
R_{DIV}	Reference divider range	1		63	
N_{DIV}	Loop divider range	56		2047	
F_{LO}	LO operating frequency		3142.656		MHz

1. That amplifier can be used as a TCXO input buffer.

4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator/buffer for RTC circuit.
- an OSCI oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF[(b)], as shown on *Figure 2*.

OSCI32 is disabled by default and must be enabled by setting bit28-OSCI_EN of PRCC_BACKUP_REG0 to have 32.768KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The recommended oscillator specifications are shown in *Table 26*:

Table 26. Crystal recommended specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SXTAL}	Crystal frequency(1)	—	32.768	—	kHz
LM_{SXTAL}	Motion inductance(1)	—	5	—	kH
CM_{SXTAL}	Motional capacitance(1)	—	5.0	—	fF
CO_{SXTAL}	Shunt capacitance(1)	—	1.3	—	pF
ESR	Resonance resistance(1)	—	—	80	kΩ
CL	External load capacitance(1)	—	18	—	pF

1. Not tested in production.

The oscillator amplifier specifications are shown in the following table:

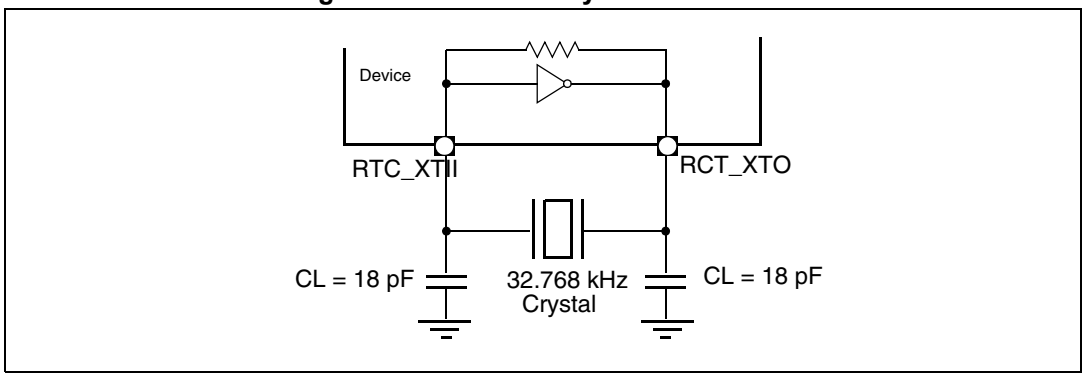
Table 27. Oscillator amplifier specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_S	Startup time(1)	—	0.3	0.6	s
DL	Drive level(1)	—	—	<0.1	µW
RLC	Required load capacitance(1)	—	12.5	—	pF
GM	Startup transconductance	22.5	33.6	—	µA/V

1. Not tested in production.

b. Using crystal with recommended characteristics as per *Table 26*.

Figure 2. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI_EN = 0b in PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 28. Characteristics of external slow clock input

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JIT} (cc)	Cycle-to-cycle jitter	-70	—	70	ps
T_{JIT} (per)	Period jitter	-70	—	70	ps
	Variation	-500	—	500	ppm
T_{DUTY}	Duty cycle	45	—	55	%

4.8.3 OSCI oscillator specifications

The supported values of the embedded BOOT ROM are 16.368 MHz, 24.00 MHz, 26.00 MHz and 48.00 MHz.

The default values supported by the GNSS binary image is 26 MHz and 48 MHz, to enable USB peripheral the 48 MHz is mandatory.

4.8.4 ADC specifications

This section gives the AC specification of the 10 bit Successive Approximation Register ADC embedded in STA8090FG device. It is controlled by the ARM9 MCU through a wrapper and an APB bridge as depicted in *Figure 3* and it has a maximum conversion rate of 1MSPS with 8 muxed analog input channels capability. An internal voltage reference is used and analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins.

Figure 3. SARADC connections

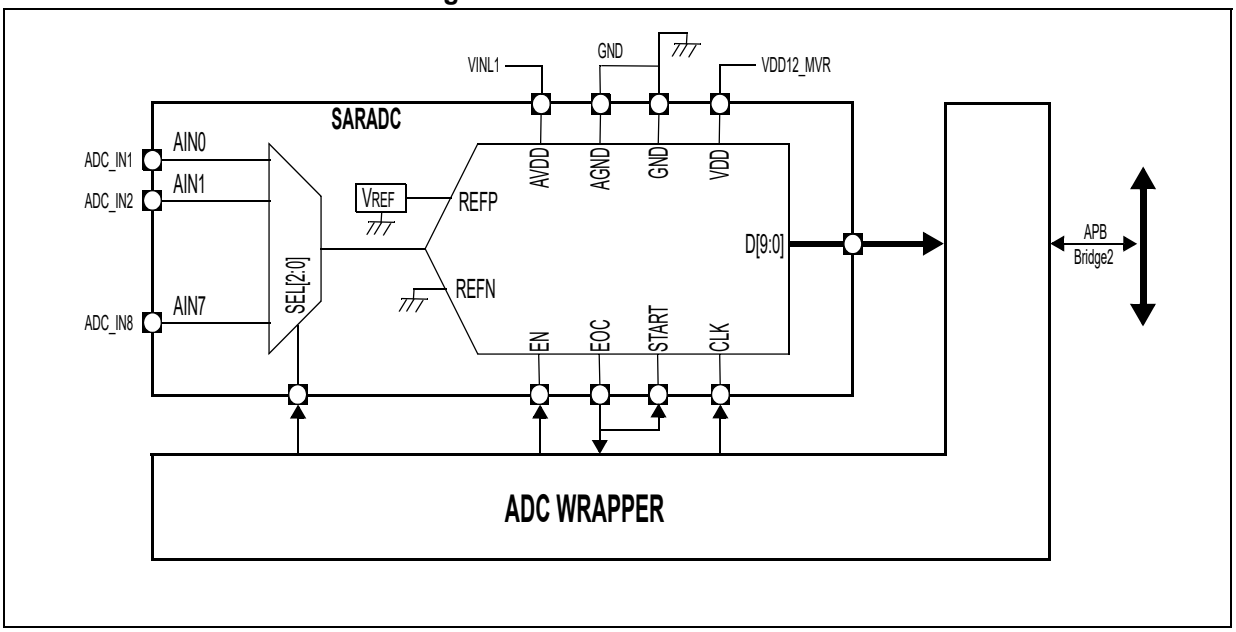


Table 29. SARADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ADCIN}	ADC_IN input range	V_{GND}-0.3	—	V_{INL1}+0.3	V
V_{ADCCR}	Conversion range	V_{GND}	—	V_{REF}	V
V_{REF}	Voltage reference	1.35	1.4	1.45	V
C_{IN}	Input capacitance(1)	5.5	7.0	8.5	pF
R_{IN}	Input mux resistance (total equivalent sampling resistance)(2)	1.5	2.0	2.5	kΩ
F_{CLK}	Clock frequency	2.5		15	MHz
δ_{CLK}	Clock duty cycle	45	50	55	%
T_{SUP}	Start up time(1)(3)	—	—	20	µs
T_C	Conversion time	—	14		cycles
T_S	Sampling time	—	3		cycles
INL	Performance			< +/- 2	LSB
DNL				< +/- 2	LSB

1. Not tested in production.
2. Pad input capacitance included.
3. From EN=1.

4.8.5 Flash specifications

This section gives the AC specification of the embedded Flash in STA8090FG device.

Table 30. Flash specifications

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_C	Serial clock frequency	QPI mode - 4 read instructions	—		78	MHz
t_{SE}	Sector erase cycle time	Size = 16 Mb	—	60	200	ms
		Size = 32 Mb	—	35	200	ms
t_{BE32}	Block erase (32 KB) cycle time	Size = 16 Mb	—	0.25	1	s
	Block erase (32 KB) cycle time	Size = 32 Mb	—	0.2	1	s
t_{BE}	Block erase (64 KB) cycle time	Size = 16 Mb	—	0.5	2	s
	Block erase (64 KB) cycle time	Size = 32 Mb	—	0.35	2	s
t_{CE}	Chip erase time	Size = 16 Mb	—	12.5	25	s
		Size = 32 Mb	—	25	50	s
t_{PP}	Page program cycle time	Size = 16 Mb	—	0.008 + (n x 0.004)	3	ms
		Size = 32 Mb	—	0.008 + (n x 0.004)	3	ms

5 Package and packing information

5.1 ECOPACK packages

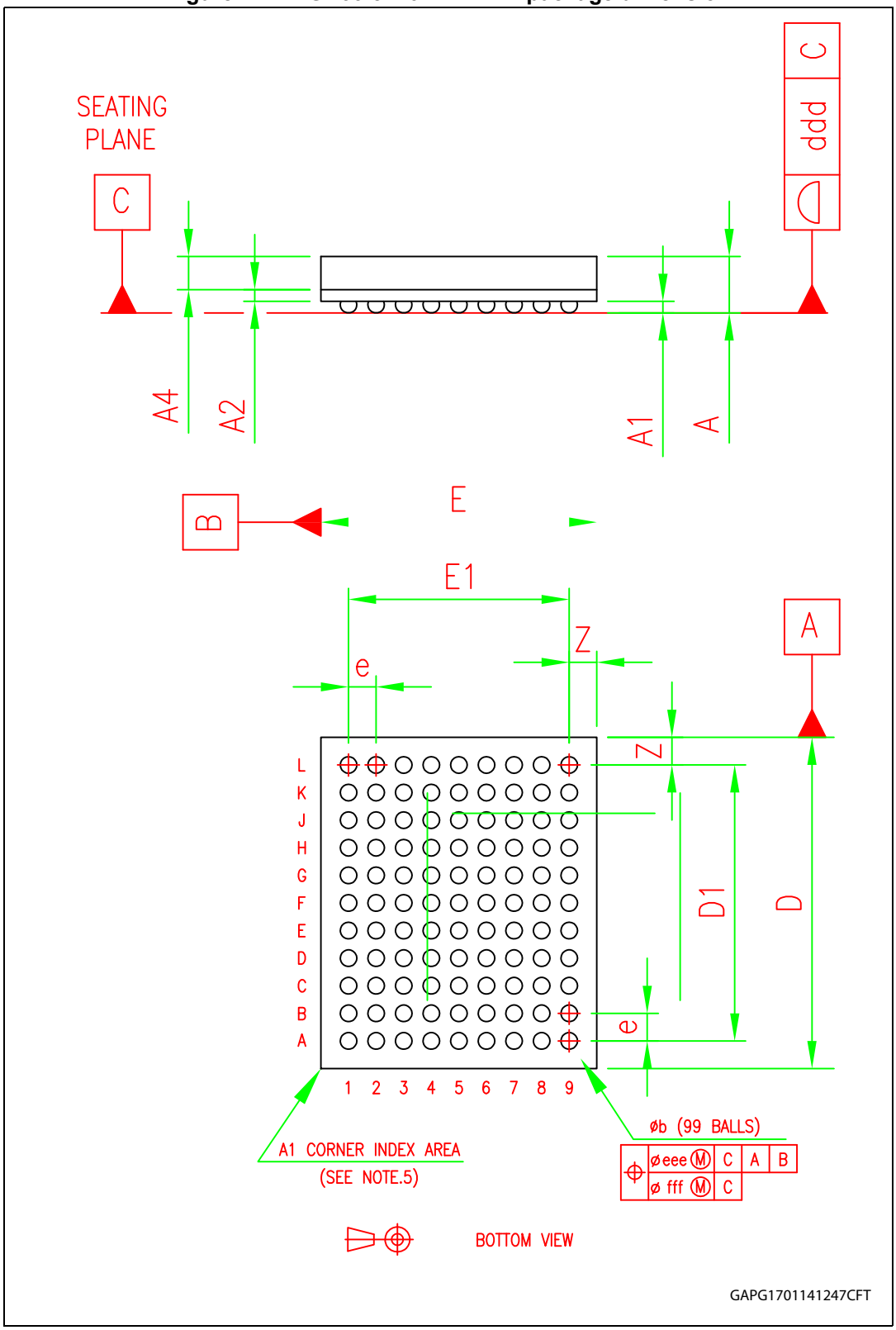
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.2 TFBGA99 5 x 6 x 1.2 mm package information

Table 31. TFBGA99 package dimensions

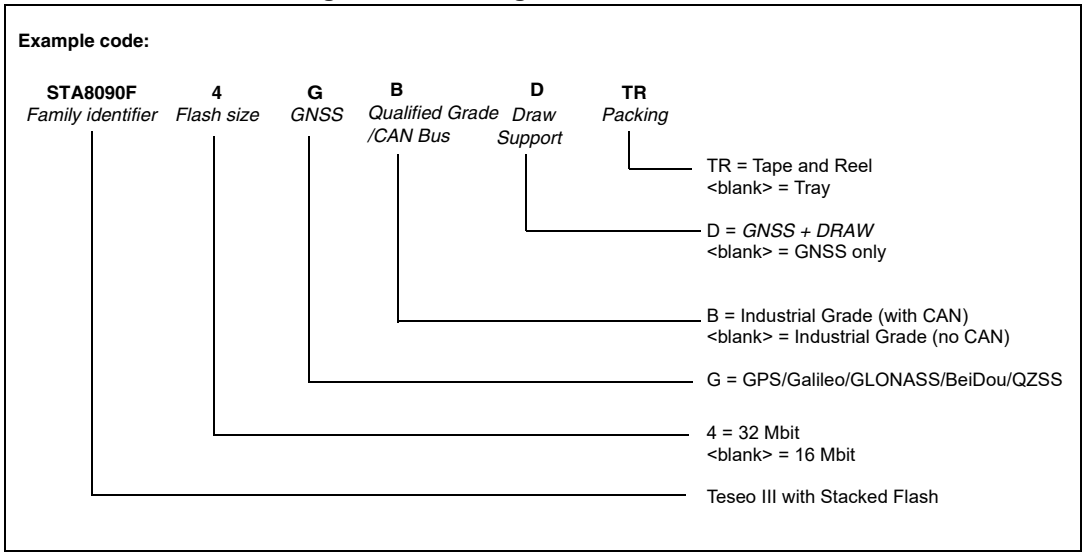
Symbol	Min.	Typ.	Max
A			1.20
A1	0.15		
A2		0.28	
A4			0.60
b	0.25	0.30	0.35
D	5.85	6.00	6.15
D1		5.00	
E	4.85	5.00	5.15
E1		4.00	
e		0.50	
F		0.50	
ddd			0.08
eee			0.15
fff			0.05

Figure 4. TFBGA99 5 x 6 x 1.2 mm package dimension



6 Ordering information

Figure 5. Ordering information scheme



7 Revision history

Table 32. Document revision history

Date	Revision	Changes
21-Nov-2014	1	Initial release.
04-Dec-2014	2	*Table 6: Test/emulated dedicated pins* – TDI, TMS: updated description *Table 7: Communication interface pins* – SPI_DI: updated description *Table 9: General purpose pins* – GPIO1: updated description *Table 20: Low voltage detection thresholds* – Input LVD always on and main VRs: removed minimum and maximun values
05-Nov-2015	3	Updated *Features* and *Description* Updated *Chapter 1: Overview* Updated *Figure 1: STA8090FG system block diagram* *Table 4: Power supply pins*: – VOL1 VOM, VDDD: updated description Updated *Section 3.4.3: UART* and *Section 3.4.4: Flash* Added *Section 3.4.5: SDMMC* and *Section 3.4.11: MSP* *Table 12: Voltage characteristics*: – $V_{ESD\text{-}HBM}$, $V_{ESD\text{-}CDM}$: updated values *Table 15: Power consumption*: – P_{RF}: updated typical value for GPS/Galileo – P_{MVR}, P_{LPVR}, P_{IO}: added note – I_{DSLEEP}: updated value *Table 16: Recommended DC operating conditions*: – V_{INL1}, V_{INL2}, V_{INM}: updated parameter *Table 17: SMPS DC characteristics*: – V_{OM}: set min and max values as TBD, removed condition for Output voltage at 1.0 V *Table 18: LDO1 DC characteristics*: – V_{OL1}: set min and max values as TBD, removed condition for Output voltage at 1.0 V *Table 19: LDO2 DC characteristics*: – V_{OL2}: set min and max values as TBD *Table 20: Low voltage detection thresholds*: – Output LVD main VR: removed condition for Output voltage at 1.0 V *Table 23: RFACHAIN – GALGPS filter and VGA*: – S11: Added note – C_G: updated values *Table 24: RFCHAIN – GLONASS/BeiDou filter and VGA*: – S11: Added note – C_G: updated values *Table 27: Oscillator amplifier specifications*: – T_S: updated minimum value Updated *Section 4.8.3: OSCI oscillator specifications*, *Section 4.8.5: Flash specifications* and *Chapter 6: Ordering information*

Table 32. Document revision history (continued)

Date	Revision	Changes
22-Mar-2017	4	Added STA8090FGBD option for DRAW support. Updated *Section 1: Overview* *Table 15: Power consumption* – Updated Min., Typ. and Max. values *Table 17: SMPS DC characteristics* – Updated Min., Typ. and Max. values *Table 18: LDO1 DC characteristics* – Updated Min., Typ. and Max. values *Table 19: LDO2 DC characteristics* – Updated Min., Typ. and Max. values Updated *Figure 5: Ordering information scheme*
29-May-2017	5	Updated: *Table 15: Power consumption*: removed I_{DSLEEP} and added $I_{DStandby}$ and $I_{DDeepStandby}$ parameters.
05-Jun-2020	6	Minor text changes.

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