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9/2020—Rev. D to Rev. E

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Updated Outline Dimensions ... 31
Changes to Ordering Guide ... 31

1/2018—Rev. C to Rev. D

Changed CP-32-7 to CP-32-2 ... Throughout
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Updated Outline Dimensions ... 31
Changes to Ordering Guide ... 31

3/2017—Rev. B to Rev. C

Changed CP-32-2 to CP-32-7 ... Throughout
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10/2013—Rev. A to Rev. B

Changed Thermal Impedance from 28°C/W to 42°C/W (Throughout) ... 9
Added Endnote 1 to Table 4 ... 9
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5/2010—Rev. 0 to Rev. A

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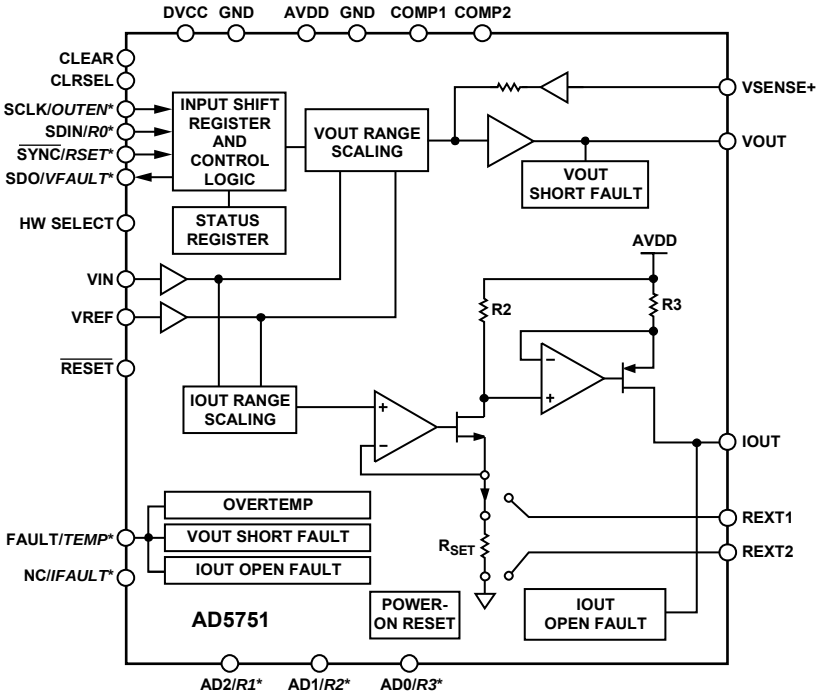
10/2009—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



*DENOTES SHARED PIN. SOFTWARE MODE DENOTED BY REGULAR TEXT, HARDWARE MODE DENOTED BY *ITALIC* TEXT. FOR EXAMPLE, FOR FAULT/*TEMP* PIN, IN SOFTWARE MODE, THIS PIN TAKES ON FAULT FUNCTION. IN HARDWARE MODE, THIS PIN TAKES ON *TEMP* FUNCTION.

Figure 1. Functional Block Diagram

SPECIFICATIONS

AV_{DD} = 12 V (± 10%) to 55 V (maximum), DV_{CC} = 2.7 V to 5.5 V, GND = 0 V. IOUT: R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE RANGE					Output unloaded
		0 to 4.096		V	
Input Leakage Current	−1		+1	µA	
REFERENCE INPUT					
Reference Input Voltage		4.096		V	External reference must be exactly as stated; otherwise, accuracy errors show up as error in output
Input Leakage Current	−1		+1	µA	
VOLTAGE OUTPUT					
Output Voltage Ranges	0		5	V	
	0		10	V	AVDD must have minimum 1.3 V headroom or >11.3 V
	0		40	V	
Output Voltage Overranges[2]	0		6	V	Programmable overranges; see Detailed Description of Features section
	0		12	V	
	0		44	V	
Accuracy					
Total Unadjusted Error (TUE)					
B Version[3]	−0.1		+0.1	% FSR	
	−0.05	±0.02	+0.05	% FSR	T_A = 25°C
A Version[3]	−0.3		+0.3	% FSR	
	−0.1	±0.05	+0.1	% FSR	T_A = 25°C
Relative Accuracy (INL)	−0.02	±0.005	+0.02	% FSR	
Dead Band on Output, RTI	−14	8	+14	mV	Referred to 4.096 V input range
Offset Error	−5		+5	mV	0 V to 10 V range
	−4	±0.5	+4	mV	T_A = 25°C, 0 V to 10 V range
	−3		+3	mV	0 V to 5 V range
	−2.2	±0.3	+2.2	mV	T_A = 25°C, 0 V to 5 V range
	−20		+20	mV	0 V to 40 V range
	−17	±0.5	+17	mV	T_A = 25°C, 0 V to 40 V range
Gain Error	−0.05		+0.05	% FSR	0 V to 5 V, 0 V to 10 V range
	−0.04	±0.015	+0.04	% FSR	T_A = 25°C
	−0.09		+0.09	% FSR	0 V to 40 V range
	−0.05	±0.02	+0.05	% FSR	T_A = 25°C
Gain Error TC[4]		±0.5		ppm FSR/°C	All ranges
Full-Scale Error	−0.05		+0.05	% FSR	0 V to 5 V, 0 V to 10 V range
	−0.04	±0.015	+0.04	% FSR	T_A = 25°C
	−0.09		+0.09	% FSR	0 V to 40 V range
	−0.05	±0.02	+0.05	% FSR	T_A = 25°C
Full-Scale Error TC[4]		±1.5		ppm FSR/°C	All ranges
OUTPUT CHARACTERISTICS[4]					
Headroom			1.3	V	Output unloaded
Short-Circuit Current		15		mA	
Load					
	1			kΩ	For specified performance, 0 V to 5 V and 0 V to 10 V ranges
	5			kΩ	For specified performance, 0 V to 40 V range

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Capacitive Load Stability					T_A = 25°C
R_{LOAD} = ∞			1	nF	
R_{LOAD} = 1 kΩ			1	nF	
R_{LOAD} = ∞			2	µF	External compensation capacitor required; see Driving Large Capacitive Loads section
DC Output Impedance		0.12		Ω	
Settling Time					
0 V to 5 V Range, ¼ to ¾ Step		7		µs	Specified with 2 kΩ || 220 pF, ±0.05%
0 V to 5 V Range, 40 mV Input Step		4.5		µs	Specified with 2 kΩ || 220 pF, ±0.05%
0 V to 40 V Range, ¼ to ¾ Step		15.8		µs	Specified with 5 kΩ || 220 pF, ±0.05%
Slew Rate		2		V/µs	Specified with 1 kΩ || 220 pF
Output Noise		3.5		µV rms	0.1 Hz to 10 Hz bandwidth
		45.5		µV rms	100 kHz bandwidth; specified with 2 kΩ || 220 pF
Output Noise Spectral Density		165		nV/√Hz	Measured at 10 kHz; specified with 2 kΩ || 220 pF
AC PSRR		65		dB	200 mV, 50 Hz/60 Hz sine wave superimposed on power supply voltage
DC PSRR		10		µV/V	
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	3.92		20	mA	
Output Current Overranges[2]	0		24.5	mA	See Detailed Description of Features section
	0		20.4	mA	See Detailed Description of Features section
	3.92		20.4	mA	See Detailed Description of Features section
ACCURACY (INTERNAL R_{SET})					
Total Unadjusted Error (TUE)					
B Version[3]	−0.2		+0.2	% FSR	
	−0.08	±0.03	+0.08	% FSR	T_A = 25°C
A Version[3]	−0.5		+0.5	% FSR	
	−0.3	±0.15	+0.3	% FSR	T_A = 25°C
Relative Accuracy (INL)	−0.02	±0.01	+0.02	% FSR	
Offset Error	−16		+16	µa	
	−10	+5	+10	µa	T_A = 25°C
Offset Error TC[4]		±3		ppm FSR/°C	
Dead Band on Output, RTI		8	+14	mV	Referred to 4.096 V input range
Gain Error	−0.2		+0.2	% FSR	
	−0.125	±0.02	+0.125	% FSR	T_A = 25°C
Gain TC[4]		±10		ppm FSR/°C	
Full-Scale Error	−0.2		+0.2	% FSR	
	−0.125	±0.02	+0.125	% FSR	T_A = 25°C
Full-Scale TC[4]		±4		ppm FSR/°C	
ACCURACY (EXTERNAL R_{SET})					
Total Unadjusted Error (TUE)					
B Version[3]	−0.1		+0.1	% FSR	
	−0.08	±0.03	+0.08	% FSR	T_A = 25°C
A Version[3]	−0.3		+0.3	% FSR	
	−0.1	±0.02	+0.1	% FSR	T_A = 25°C
Relative Accuracy (INL)	−0.02	±0.01	+0.02	% FSR	
Offset Error	−14		+14	µA	
	−11	+5	+11		T_A = 25°C
Offset Error TC[4]		±2		ppm FSR/°C	
Dead Band on Output, RTI		8	+14	mV	Referred to 4.096 V input range
Gain Error	−0.08		+0.08	% FSR	
	−0.07	±0.02	+0.07	% FSR	T_A = 25°C

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Gain TC[4]		±1		ppm FSR/°C	
Full-Scale Error	−0.1		+0.1	% FSR	
	−0.07	±0.02	+0.07	% FSR	T_A = 25°C
Full-Scale TC[4]		±2		ppm FSR/°C	
OUTPUT CHARACTERISTICS[4]					
Current Loop Compliance Voltage	0		AV_{DD} − 2.75	V	
Resistive Load					Chosen such that compliance is not exceeded
Inductive Load	See test conditions/comments column			H	Needs appropriate capacitor at higher inductance values; see Driving Inductive Loads section
Settling Time					
4 mA to 20 mA, Full-Scale Step		8.5		µs	250 Ω load
120 µA Step, 4 mA to 20 mA Range		1.2		µs	250 Ω load
DC PSRR			1	µA/V	
Output Impedance		130		MΩ	
DIGITAL INPUTS[4]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		5		pF	Per pin
DIGITAL OUTPUTS[4]					
FAULT, IFAULT, TEMP, VFAULT					
V_{OL}, Output Low Voltage			0.4	V	10 kΩ pull-up resistor to DVCC
		0.6		V	At 2.5 mA
V_{OH}, Output High Voltage	3.6			V	10 kΩ pull-up resistor to DVCC
SDO					
V_{OL}, Output Low Voltage	0.5	0.5		V	Sinking 200 µA
V_{OH}, Output High Voltage	DVCC − 0.5	DVCC − 0.5		V	Sourcing 200 µA
High Impedance Output Capacitance		3		pF	
High Impedance Leakage Current	−1		+1	µA	
POWER REQUIREMENTS					
AV_{DD}	10.8		55	V	
DV_{CC}					
Input Voltage	2.7		5.5	V	
AI_{DD}		4.4	5.6	mA	Output unloaded, output disabled
		5.2	6.2	mA	Current output enabled
		5.2	6.2	mA	Voltage output enabled
DI_{CC}		0.3	1	mA	V_{IH} = DVCC, V_{IL} = GND
Power Dissipation		108		mW	AVDD = 24 V, outputs unloaded

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Overranges are nominal; gain and offset are not trimmed as per nominal ranges.
[3] Specification includes gain and offset errors, over temperature, and drift after 1000 hours, T_A = 125°C.
[4] Guaranteed by characterization, but not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 12 V (± 10%) to 55 V (maximum), DV_{CC} = 2.7 V to 5.5 V, GND = 0 V. VOUT: R_{LOAD} = 2 kΩ (5 kΩ for 0 V to 40 V range), C_L = 200 pF, IOUT: R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	5	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	10	ns min	16th SCLK falling edge to $\overline{SYNC}$ rising edge (on 24th SCLK falling edge if using PEC)
t_6	5	ns min	Minimum $\overline{SYNC}$ high time (write mode)
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9, t_{10}	1.5	µs max	CLEAR pulse low/high activation time
t_{11}	5	ns min	Minimum $\overline{SYNC}$ high time (read mode)
t_{12}	40	ns max	SCLK rising edge to SDO valid (SDO C_L = 15 pF)
t_{13}	10	ns min	$\overline{RESET}$ pulse low time

[1] Guaranteed by characterization, but not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.

Timing Diagrams

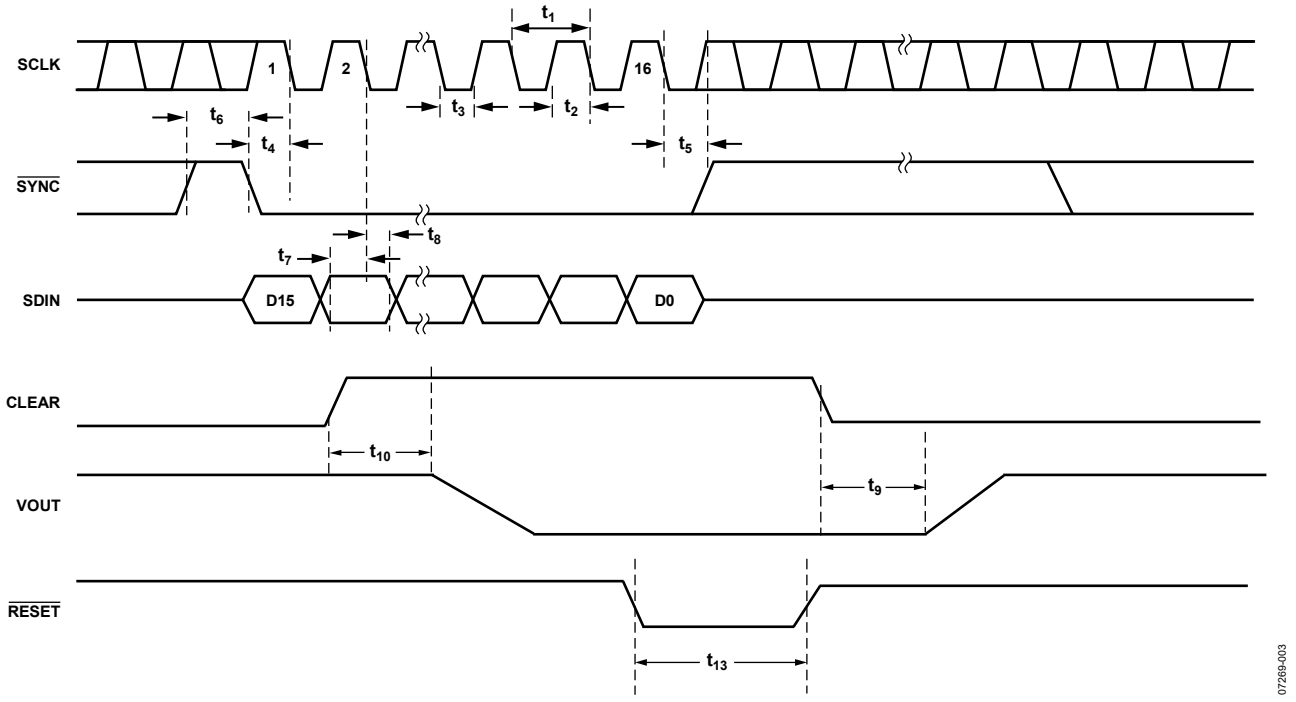


Figure 2. Write Mode Timing Diagram

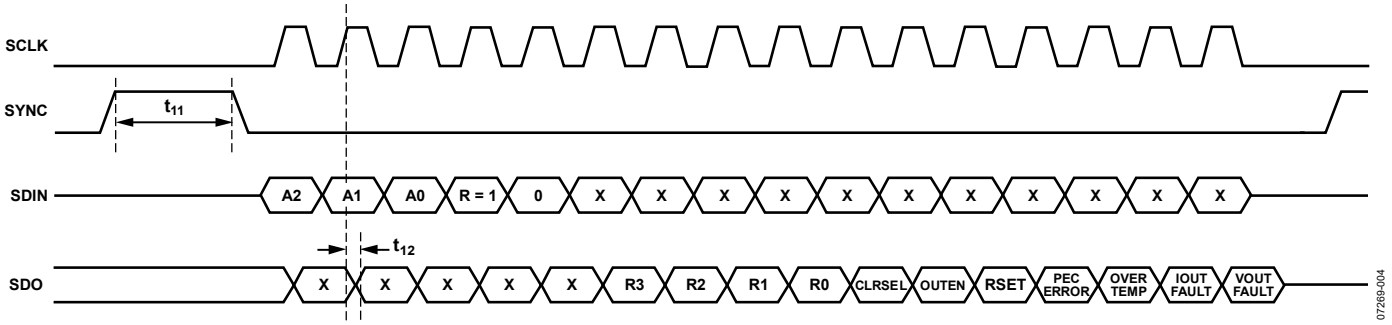


Figure 3. Readback Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AVDD to GND	−0.3 V to +58 V
DVCC to GND	−0.3 V to +7 V
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V, or 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V, or 7 V (whichever is less)
VREF to GND	−0.3 V to +7 V
VSENSE+ to GND	−0.3 V to AV_{DD}
VIN to GND	−0.3 V to +7 V
VOUT, IOUT to GND	−0.3 V to AV_{DD}
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
32-Lead LFCSP Package	
θ_{JA} Thermal Impedance[1]	42°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] Simulated data based on a JEDEC 2s2p test board with thermal vias.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

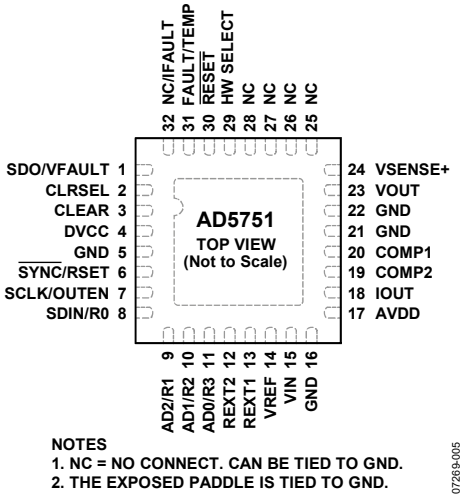


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SDO/VFAULT	Serial Data Output (SDO). In software mode, this pin is used to clock data from the input shift register in readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. This pin is a CMOS output. Short-Circuit Fault Alert (VFAULT). In hardware mode, this pin acts as a short-circuit fault alert pin and is asserted low when a short-circuit error is detected. This pin is an open-drain output and must be connected to a pull-up resistor.
2	CLRSEL	In hardware or software mode, this pin selects the clear value, either zero-scale or midscale code. In software mode, this pin is implemented as a logic OR with the internal CLRSEL bit.
3	CLEAR	Active High Input. Asserting this pin sets the output current/voltage to zero-scale code or midscale code of range selected (user-selectable). CLEAR is a logic OR with the internal clear bit. See the Asynchronous Clear (CLEAR) section for more details. In software mode, during power-up, the CLEAR pin level determines the power-on condition of the voltage channel, which can be active 0 V or tristate.
4	DVCC	Digital Power Supply.
5	GND	Ground Connection.
6	$\overline{\text{SYNC}}$/RSET	Positive Edge-Sensitive Latch ($\overline{\text{SYNC}}$). In software mode, a rising edge parallel loads the input shift register data into the AD5751, also updating the output. Resistor Select (RSET). In hardware mode, this pin selects whether the internal or the external current sense resistor is used. If RSET = 0, the external sense resistor is chosen. If RSET = 1, the internal sense resistor is chosen.
7	SCLK/OUTEN	Serial Clock Input (SCLK). In software mode, data is clocked into the input shift register on the falling edge of SCLK. This pin operates at clock speeds up to 50 MHz. Output Enable (OUTEN). In hardware mode, this pin acts as an output enable pin.
8	SDIN/R0	Serial Data Input (SDIN). In software mode, data must be valid on the falling edge of SCLK. Range Decode Bit (R0). In hardware mode, this pin, in conjunction with R1, R2, and R3, selects the output current/voltage range setting on the part.
9	AD2/R1	Device Addressing Bit (AD2). In software mode, this pin, in conjunction with AD0 and AD1, allows up to eight devices to be addressed on one bus. Range Decode Bit (R1). In hardware mode, this pin, in conjunction with R0, R2, and R3, selects the output current/voltage range setting on the part.

Pin No.	Mnemonic	Description
10	AD1/R2	Device Addressing Bit (AD1). In software mode, this pin, in conjunction with AD0 and AD2, allows up to eight devices to be addressed on one bus. Range Decode Bit (R2). In hardware mode, this pin, in conjunction with R0, R1, and R3, selects the output current/voltage range setting on the part.
11	AD0/R3	Device Addressing Bit (AD0). In software mode, this pin, in conjunction with AD1 and AD2, allows up to eight devices to be addressed on one bus. Range Decode Bit (R3). In hardware mode, this pin, in conjunction with R0, R1, and R2, selects the output current/voltage range setting on the part.
12, 13	REXT2, REXT1	A 15 kΩ external current setting resistor can be connected between the REXT1 and REXT2 pins to improve the IOUT temperature drift performance.
14	VREF	Buffered Reference Input.
15	VIN	Buffered Analog Input (0 V to 4.096 V).
16	GND	Ground Connection.
17	AVDD	Positive Analog Supply.
18	IOUT	Current Output.
19, 20	COMP2, COMP1	Optional Compensation Capacitor Connections for the Voltage Output Buffer. These are used to drive higher capacitive loads on the output. These pins also reduce overshoot on the output. Care should be taken when choosing the value of the capacitor connected between the COMP1 and COMP2 pins because it has a direct influence on the settling time of the output. See the Driving Large Capacitive Loads section for further details.
21	GND	Ground Connection.
22	GND	Ground Connection.
23	VOUT	Buffered Analog Output Voltage.
24	VSENSE+	Sense Connection for the Positive Voltage Output Load Connection.
25, 26, 27, 28	NC	No Connect. Can be tied to GND.
29	HW SELECT	This part is used to configure the part to hardware or software mode. HW SELECT = 0 selects software control. HW SELECT = 1 selects hardware control.
30	$\overline{\text{RESET}}$	In software mode, this pin resets the part to its power-on state. Active low. In hardware mode, there is no reset. If using the part in hardware mode, the $\overline{\text{RESET}}$ pin should be tied high.
31	FAULT/TEMP	Fault Alert (FAULT). In software mode, this pin acts as a general fault alert pin. It is asserted low when an open-circuit, short-circuit, overtemperature error, or PEC interface error is detected. This pin is an open-drain output and must be connected to a pull-up resistor. Overtemperature Fault (TEMP). In hardware mode, this pin acts as an overtemperature fault pin. It is asserted low when an overtemperature error is detected. This pin is an open-drain output and must be connected to a pull-up resistor.
32	NC/IFAULT	No Connect (NC). In software mode, this pin is a no connect. Instead, tie this pin to GND. Open-Circuit Fault Alert (IFAULT). In hardware mode, this pin acts as an open-circuit fault alert pin. It is asserted low when an open-circuit error is detected. This pin is an open-drain output and must be connected to a pull-up resistor.
33 (EPAD)	Exposed paddle	The exposed paddle is tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

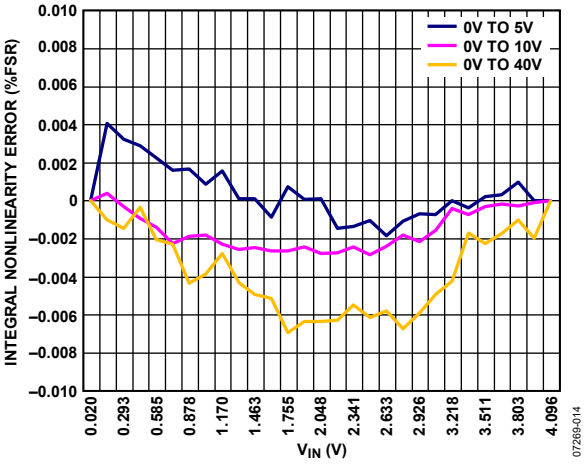


Figure 5. Integral Nonlinearity Error vs. V_{IN}

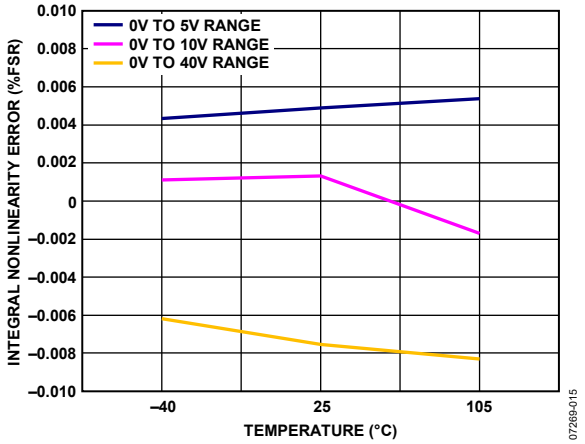


Figure 6. Integral Nonlinearity Error vs. Temperature

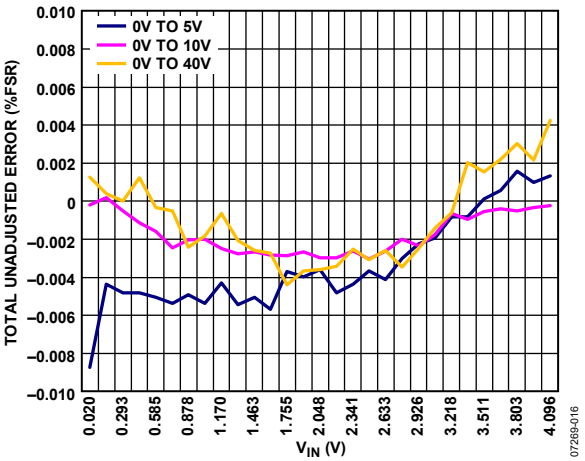


Figure 7. Total Unadjusted Error vs. V_{IN}

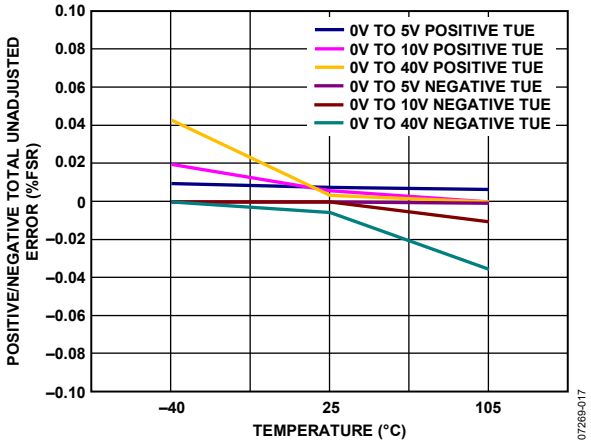


Figure 8. Total Unadjusted Error vs. Temperature

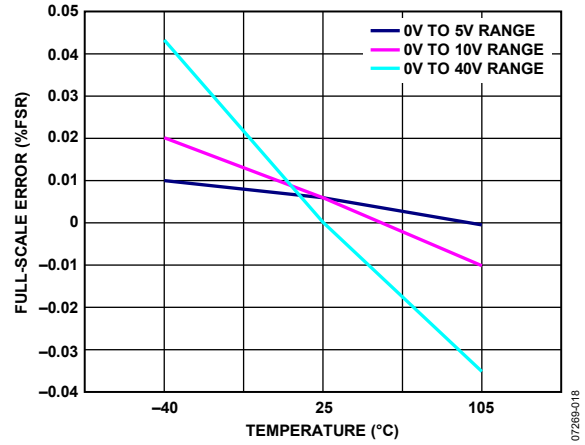


Figure 9. Full-Scale Error vs. Temperature

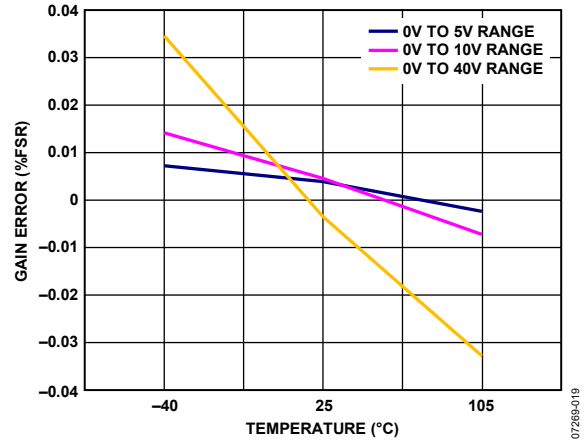


Figure 10. Gain Error vs. Temperature

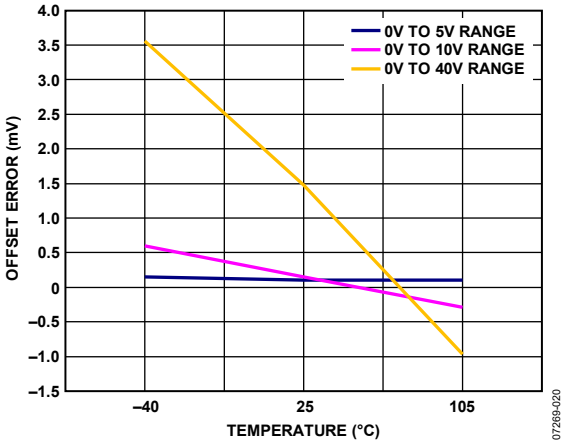


Figure 11. Offset Error vs. Temperature

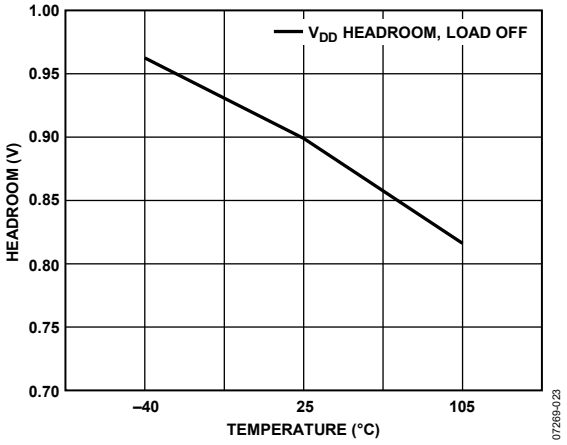


Figure 14. AVDD Headroom, 0 V to 10 V Range, Output Set to 10 V, Load Off

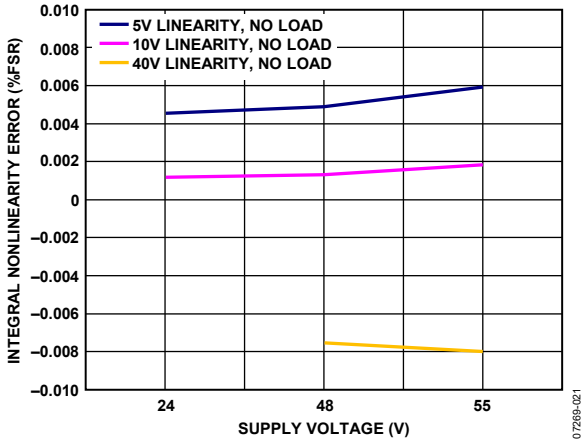


Figure 12. INL Error vs. Supply Voltage

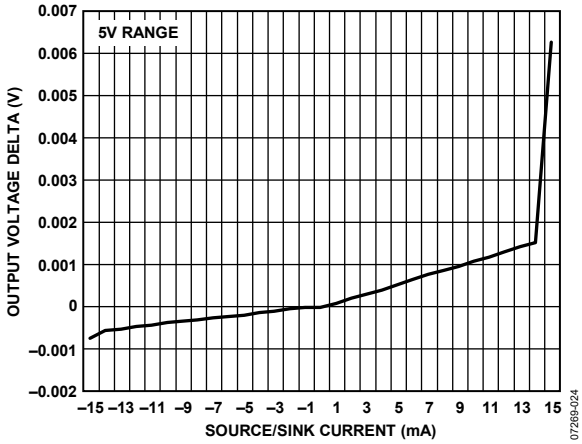


Figure 15. Source and Sink Capability of Output Amplifier

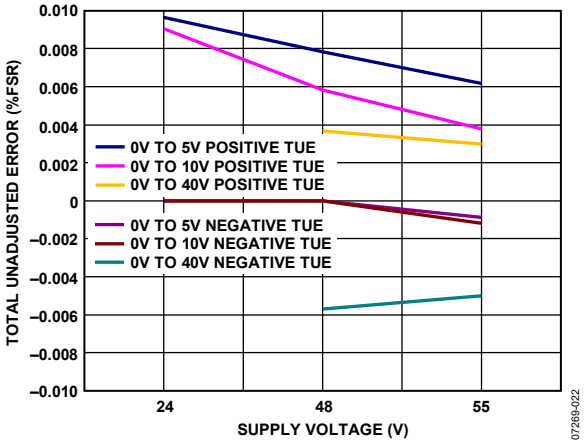


Figure 13. Total Unadjusted Error vs. Supply Voltage

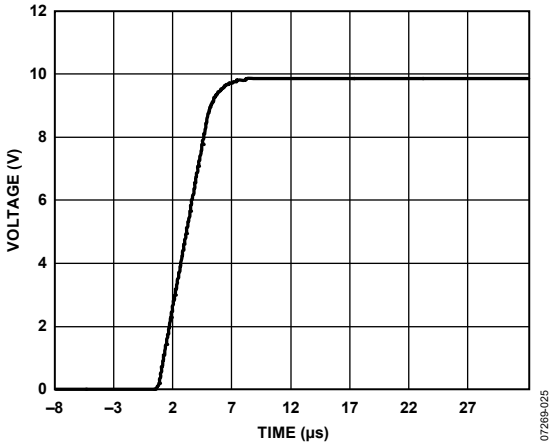


Figure 16. Full-Scale Positive Step, 10 V Range

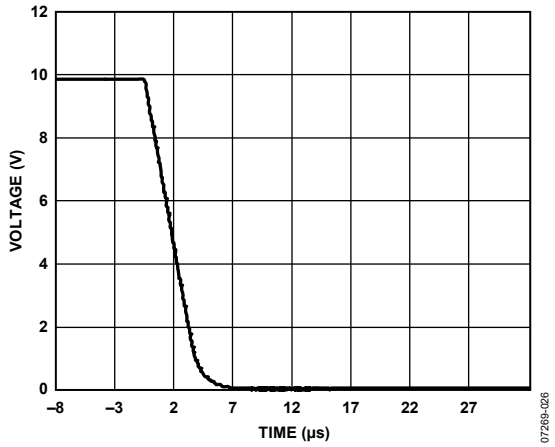


Figure 17. Full-Scale Negative Step, 10 V Range

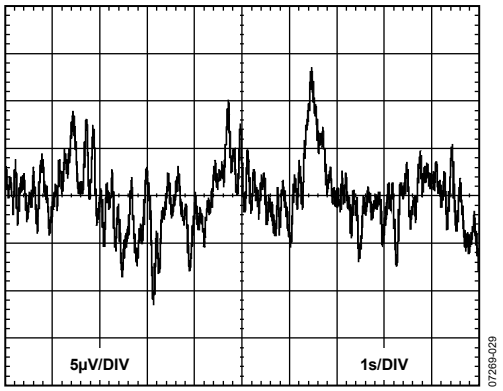


Figure 20. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

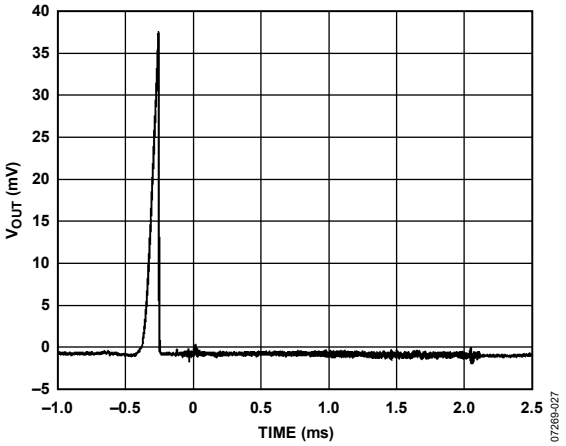


Figure 18. V_{OUT} vs. Time on Power-Up, Load = 2 kΩ || 200 pF

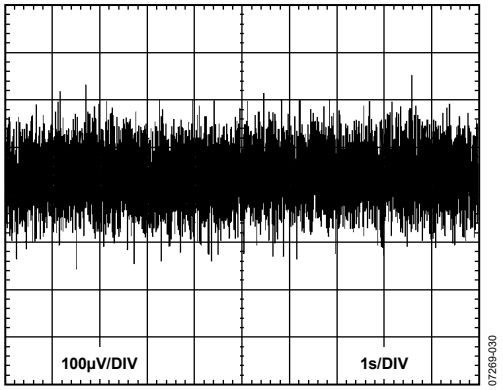


Figure 21. Peak-to-Peak Noise (100 kHz Bandwidth)

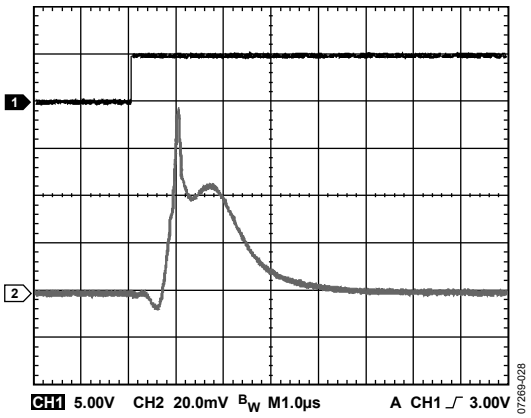


Figure 19. V_{OUT} Enable Glitch, Load = 2 kΩ || 1 nF

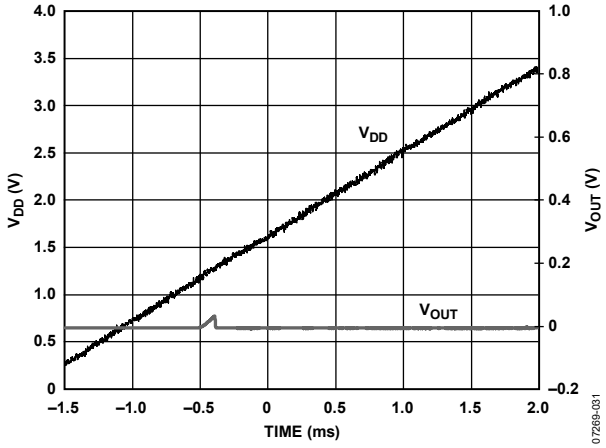


Figure 22. V_{DD} and V_{OUT} vs. Time on Power-Up

CURRENT OUTPUT

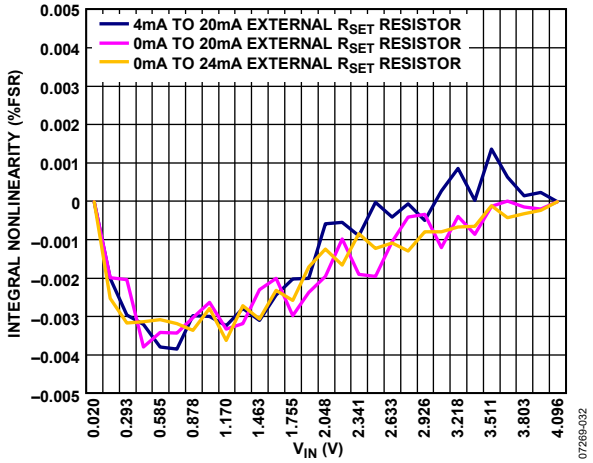


Figure 23. Integral Nonlinearity Error vs. V_{IN}, External R_{SET} Resistor

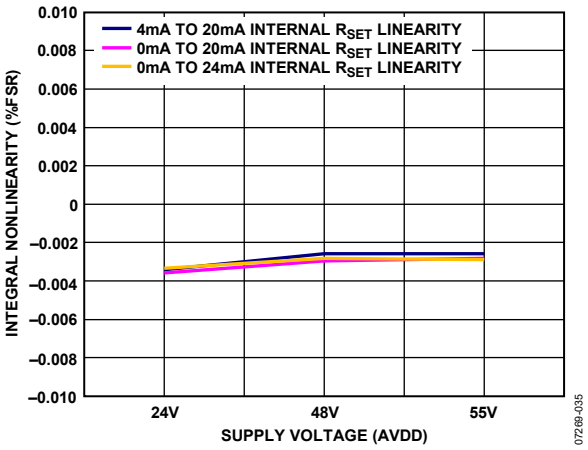


Figure 26. Integral Nonlinearity Current Mode, Internal R_{SET} Sense Resistor

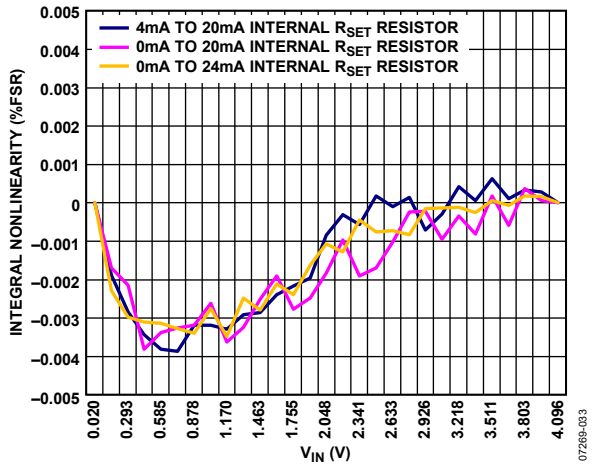


Figure 24. Integral Nonlinearity Error vs. V_{IN}, Internal R_{SET} Resistor

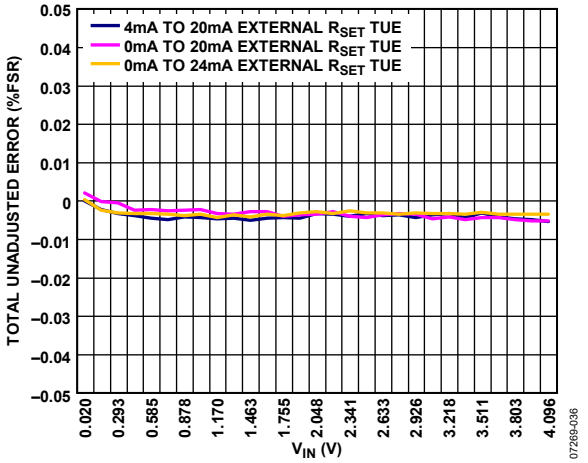


Figure 27. Total Unadjusted Error vs. V_{IN}, External R_{SET} Resistor

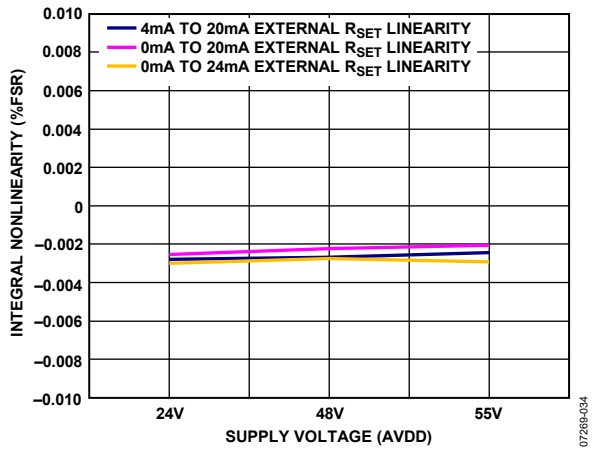


Figure 25. Integral Nonlinearity Current Mode, External R_{SET} Sense Resistor

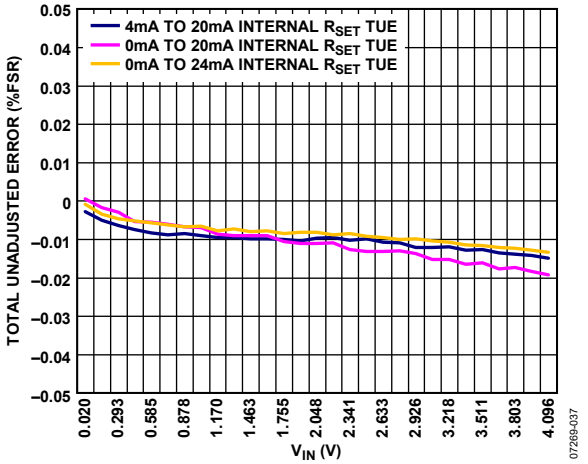


Figure 28. Total Unadjusted Error vs. V_{IN}, Internal R_{SET} Resistor

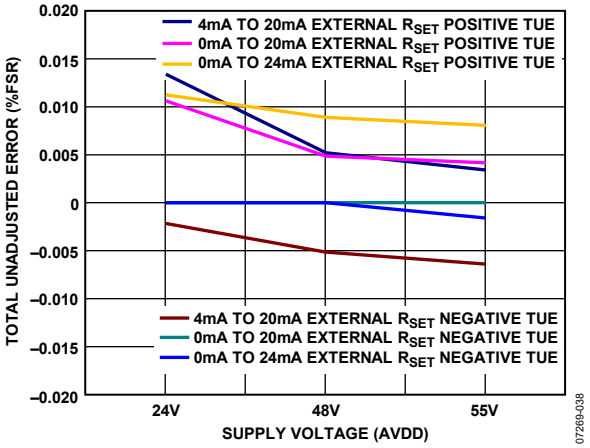


Figure 29. Total Unadjusted Error Current Mode, External R_{SET} Sense Resistor

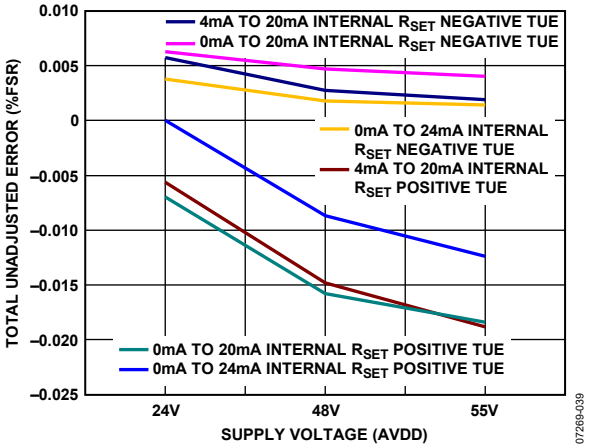


Figure 30. Total Unadjusted Error Current Mode, Internal R_{SET} Sense Resistor

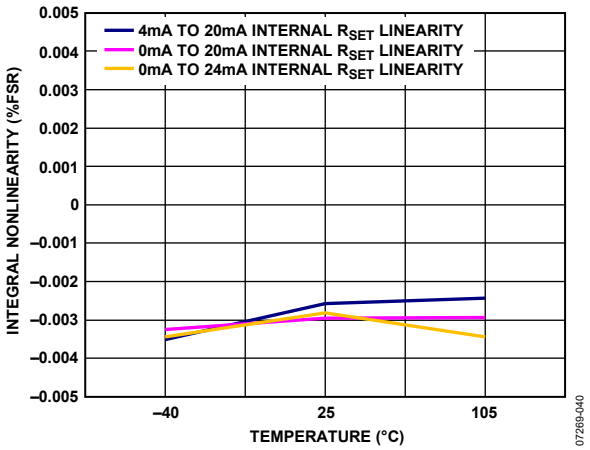


Figure 31. Integral Nonlinearity Error vs. Temperature, Internal R_{SET} Sense Resistor

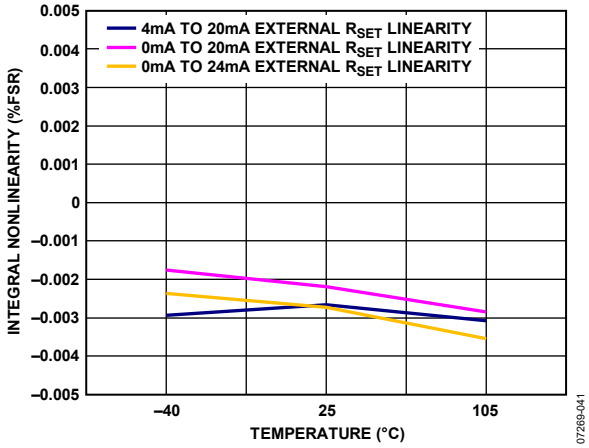


Figure 32. Integral Nonlinearity Error vs. Temperature, External R_{SET} Sense Resistor

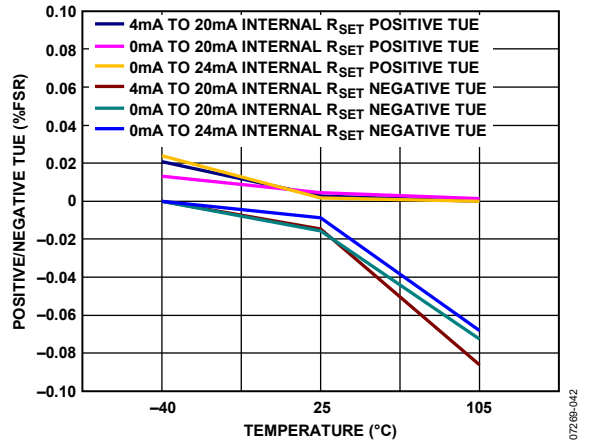


Figure 33. Total Unadjusted Error vs. Temperature, Internal R_{SET} Sense Resistor

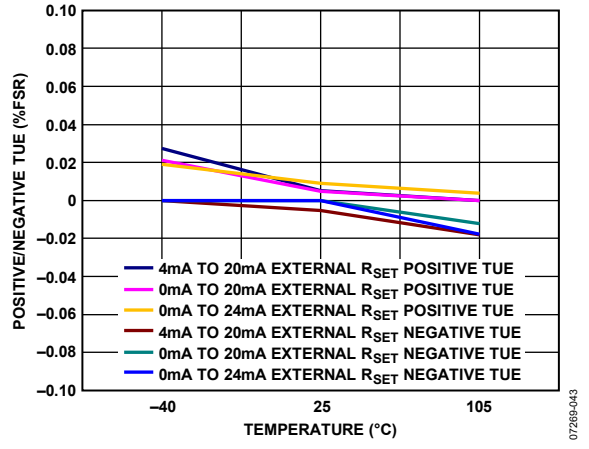


Figure 34. Total Unadjusted Error vs. Temperature, External R_{SET} Sense Resistor

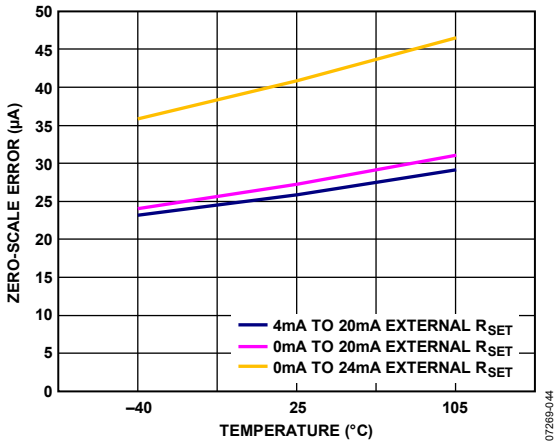


Figure 35. Zero-Scale Error vs. Temperature, External R_{SET} Sense Resistor

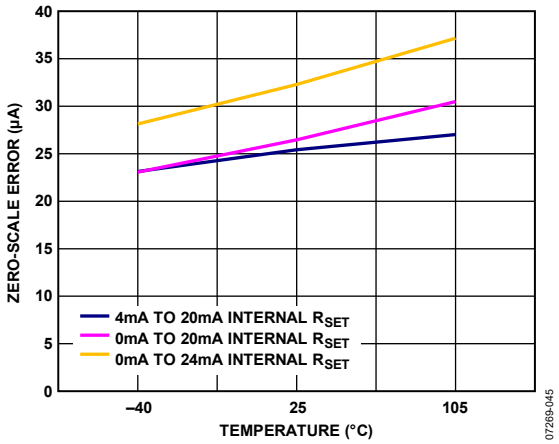


Figure 36. Zero-Scale Error vs. Temperature, Internal R_{SET} Sense Resistor

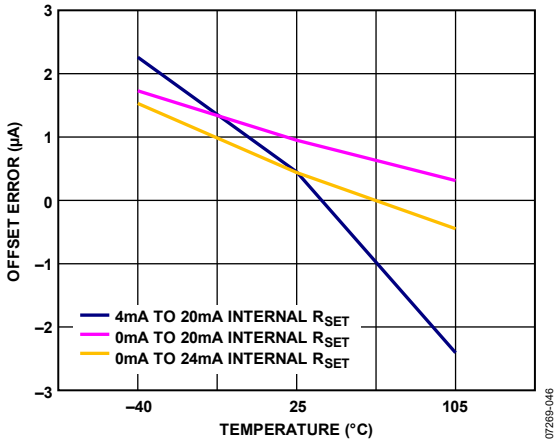


Figure 37. Offset Error vs. Temperature, Internal R_{SET} Sense Resistor

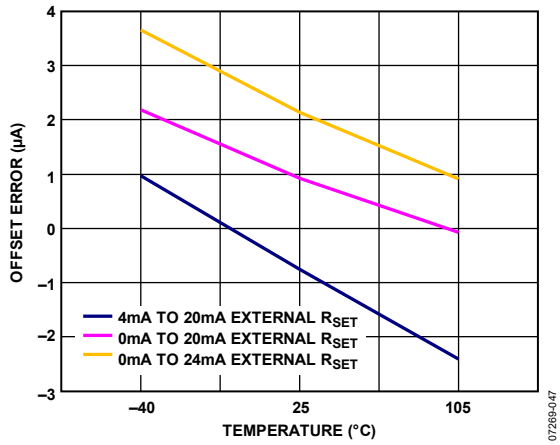


Figure 38. Offset Error vs. Temperature, External R_{SET} Sense Resistor

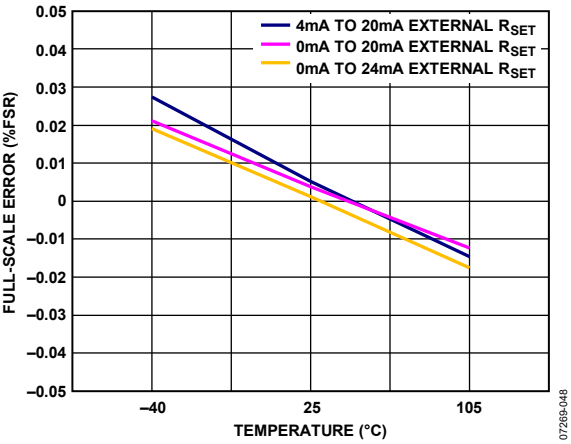


Figure 39. Full-Scale Error vs. Temperature, External R_{SET} Sense Resistor

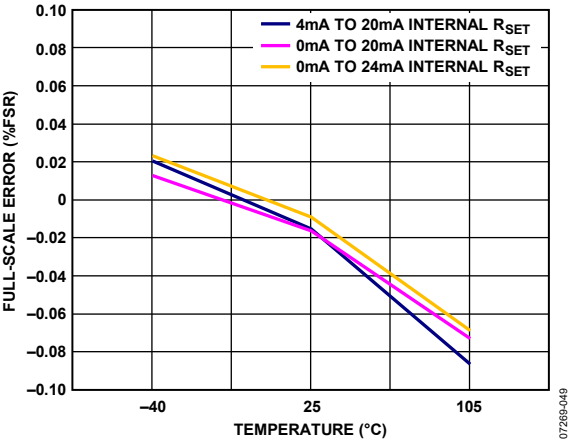


Figure 40. Full-Scale Error vs. Temperature, Internal R_{SET} Sense Resistor

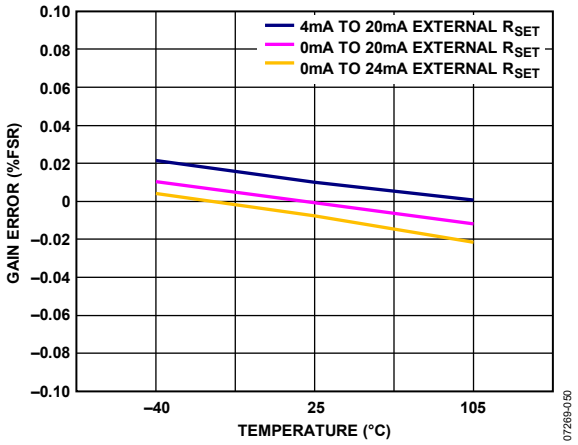


Figure 41. Gain Error vs. Temperature, External R_{SET} Sense Resistor

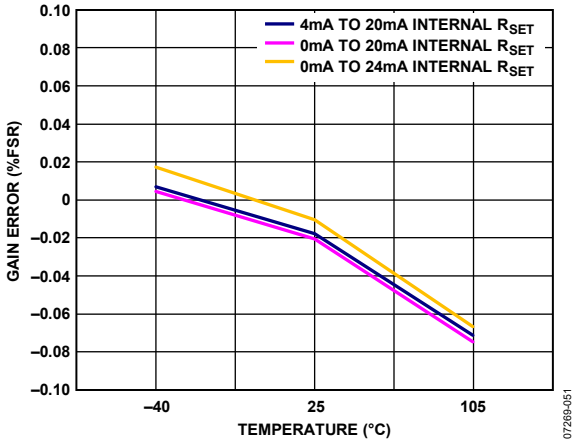


Figure 42. Gain Error vs. Temperature, Internal R_{SET} Sense Resistor

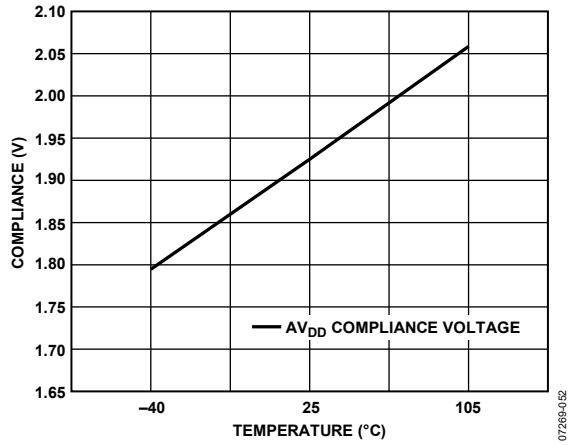


Figure 43. Output Compliance vs. Temperature
Tested When I_{OUT} = 10.8 mA, 0 mA to 24 mA Range Selected

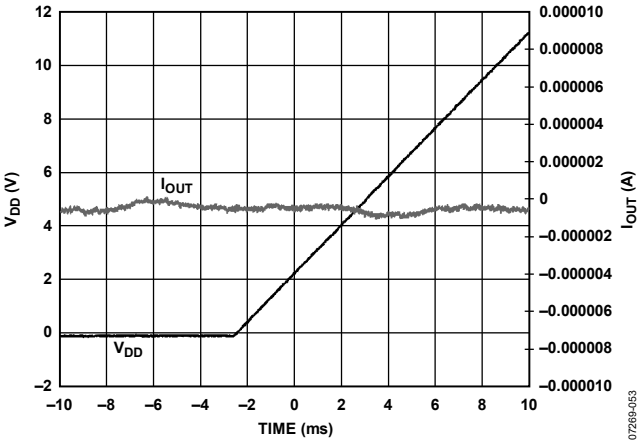


Figure 44. Output Current vs. Time on V_{DD} Power-Up

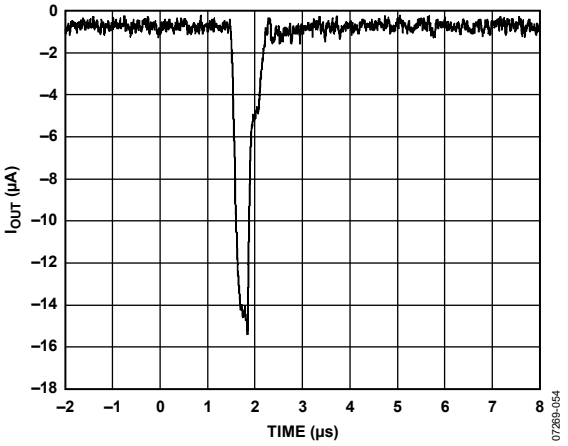


Figure 45. Output Current vs. Time on Output Enable, 0 mA to 20 mA Range

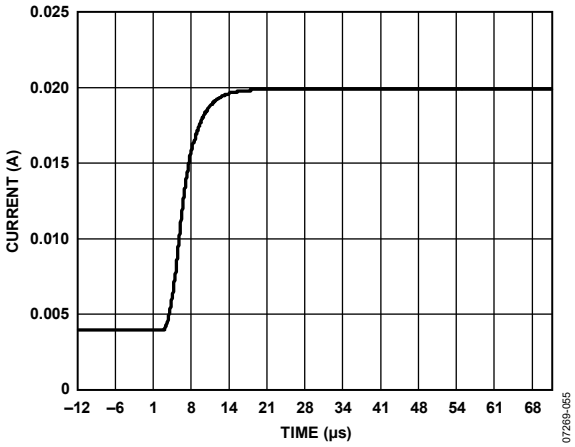


Figure 46. 4 mA to 20 mA Output Current Step

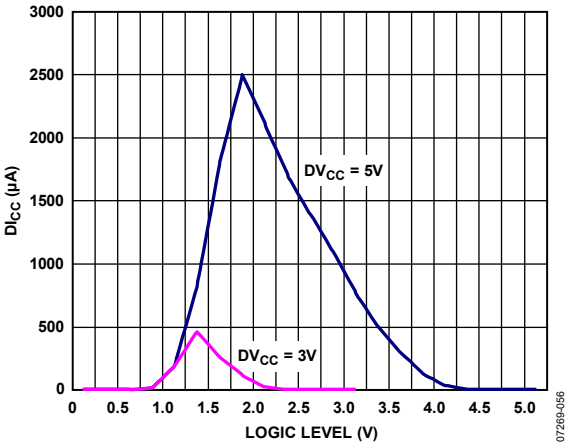


Figure 47. DI_{CC} vs. Logic Input Voltage

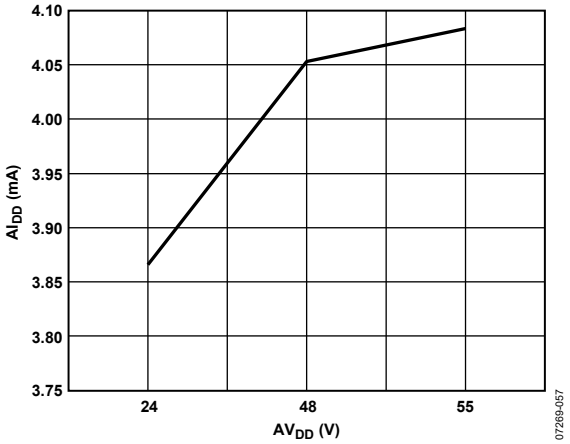


Figure 48. AI_{DD} vs. AV_{DD}, V_{OUT} = 0 V

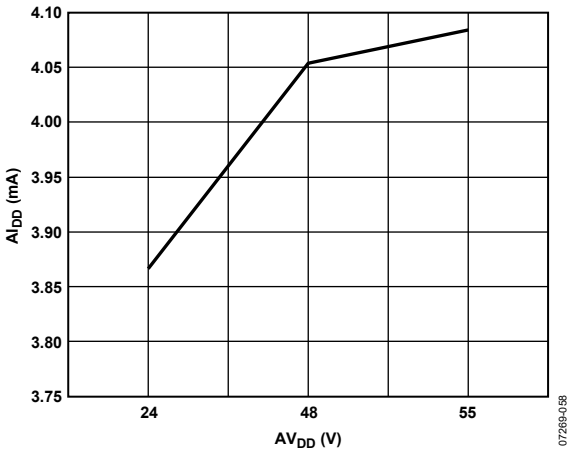


Figure 49. AI_{DD} vs. AV_{DD}, I_{OUT} = 0 mA

TERMINOLOGY

Total Unadjusted Error (TUE)
TUE is a measure of the output error taking all the various errors into account: INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed as a percentage of full-scale range (% FSR).

Relative Accuracy or Integral Nonlinearity (INL)
INL is a measure of the maximum deviation, in % FSR, from a straight line passing through the endpoints of the output driver transfer function. A typical INL vs. input voltage plot is shown in Figure 5.

Full-Scale Error
Full-scale error is the deviation of the actual full-scale analog output from the ideal full-scale output. Full-scale error is expressed as a percentage of full-scale range (% FSR).

Full-Scale TC
Full-scale TC is a measure of the change in the full-scale error with a change in temperature. It is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the output. It is the deviation in slope of the output transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature is shown in Figure 10.

Gain Error TC
Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/°C.

Zero-Scale Error
Zero-scale error is the deviation of the actual zero-scale analog output from the ideal zero-scale output. Zero-scale error is expressed in millivolts (mV).

Zero-Scale TC
Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Offset Error
Offset error is a measurement of the difference between the actual VOUT and the ideal VOUT expressed in millivolts (mV) in the linear region of the transfer function. It can be negative or positive.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a half-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/µs.

Current Loop Voltage Compliance
Current loop voltage compliance is the maximum voltage at the IOUT pin for which the output current is equal to the programmed value.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5751 is powered on. It is specified as the area of the glitch in nV-sec.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output is affected by changes in the power supply voltage.

THEORY OF OPERATION

The AD5751 is a single-channel, low cost, precision, voltage/current output driver with hardware or software programmable output ranges. The software ranges are configured via an SPI-/MICROWIRE-compatible serial interface. The hardware ranges are programmed using the range pins (R0 to R3). The analog input to the AD5751 is provided from a low voltage, single-supply DAC (0 V to 4.096 V), which is internally conditioned to provide the desired output current/voltage range.

The output current range is programmable across three ranges: 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA. The voltage output is provided from a separate pin that can be configured to provide 0 V to 5 V, 0 V to 10 V, and 0 V to 40 V output ranges. An overrange of 20% is available on the 5 V and 10 V output voltage ranges, and of 10% on the 0 V to 40 V range. The VOUT and IOUT pins can be connected together. An overrange of 2% is available on the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current ranges. The current and voltage outputs are available on separate pins. Only one output can be enabled at one time. The output range is selected by programming the R3 to R0 bits in the control register (see Table 7 and Table 8).

Figure 50 and Figure 51 show a typical configuration of AD5751 in software mode and in hardware mode, respectively, in an output module system. The HW SELECT pin chooses whether the part is configured in software or hardware mode. The analog input to the AD5751 is provided from a low voltage, single-supply DAC such as the AD506x or AD566x, which can provide an output range of 0 V to 4.096 V. The supply and reference for the DAC, as well as the reference for the AD5751, can be supplied from a reference such as the ADR392. The AD5751 can operate with a single supply up to 55 V.

SOFTWARE MODE

In current mode, software-selectable output ranges include 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA.

In voltage mode, software-selectable output ranges include 0 V to 5 V, 0 V to 10 V, 0 V to 40 V.

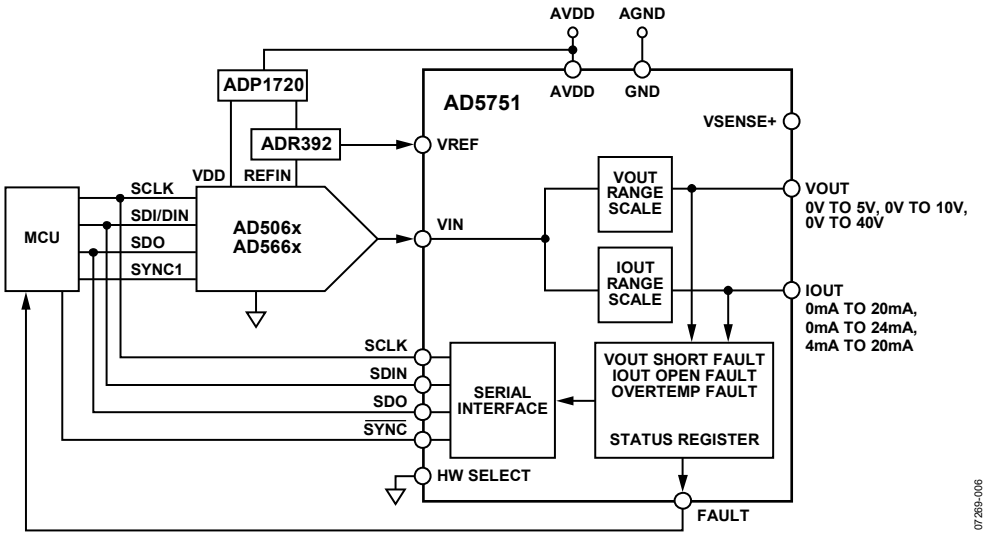


Figure 50. Typical System Configuration in Software Mode (Pull-Up Resistors Not Shown for Open-Drain Outputs)

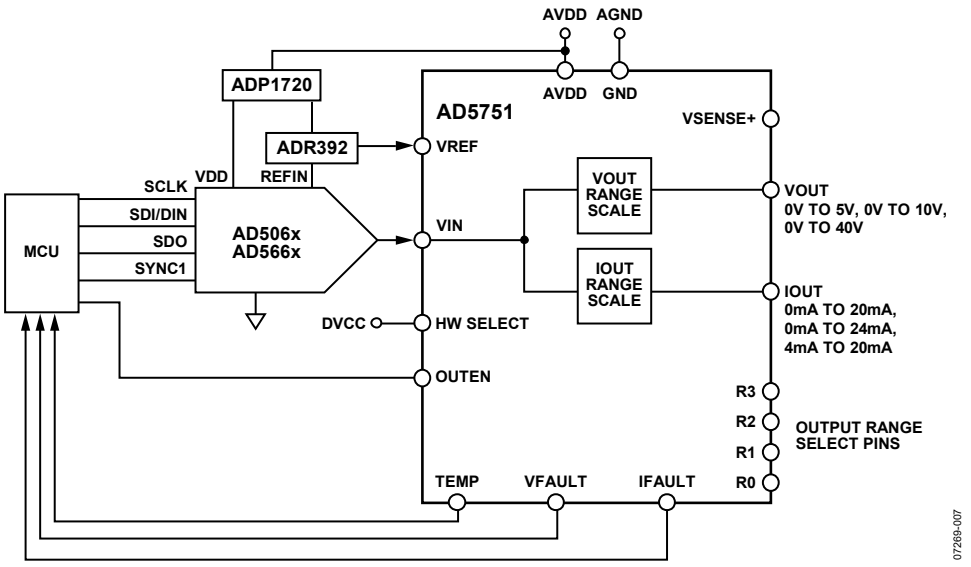


Figure 51. Typical System Configuration in Hardware Mode Using Internal DAC Reference (Pull-Up Resistors Not Shown for Open-Drain Outputs)

Table 6. Suggested Parts for Use with the AD5751

DAC	Reference	Power	Resolution/Accuracy	Description
AD5660	Internal	ADP1720[1]	16-bit/12-bit	Mid end system, single channel, internal reference
AD5664R	Internal	N/A	16-bit/12-bit	Mid end system, quad channel, internal reference
AD5668	Internal	N/A	16-bit/12-bit	Mid end system, octal channel, internal reference
AD5060	ADR434	ADP1720	16-bit/16-bit	High end system, single channel, external reference
AD5064/AD5066	ADR434	N/A	16-bit/16-bit	High end system, quad channel, external reference
AD5662	ADR392[2]	ADR392[2]	16-bit/12-bit	Mid end system, single channel, external reference
AD5664	ADR392[2]	N/A	16-bit/12-bit	Mid end system, quad channel, external reference

[1] ADP1720 input range up to 28 V.
[2] ADR392 input range up to 15 V.

CURRRENT OUTPUT ARCHITECTURE

The voltage input from the analog input VIN core (0 V to 4.096 V) is either converted to a current (see Figure 52), which is then mirrored to the supply rail so that the application simply sees a current source output with respect to an internal reference voltage, or it is buffered and scaled to output a software-selectable unipolar voltage range (see Figure 53). The reference is used to provide internal offsets for range and gain scaling. The selectable output range is programmable through the digital interface (software mode) or via the range pins (R0 to R3) (hardware mode).

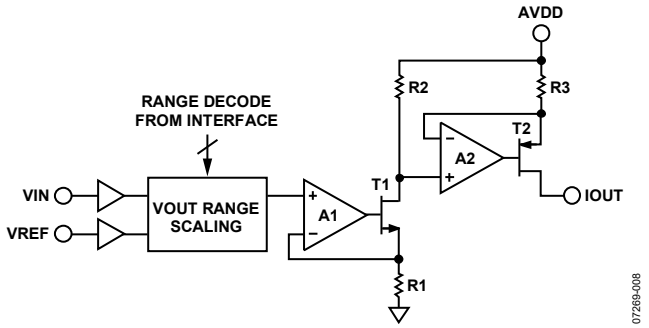


Figure 52. Current Output Configuration

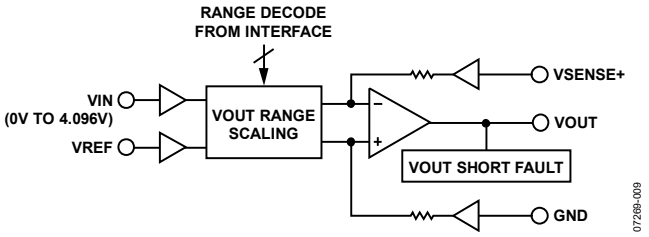


Figure 53. Voltage Output

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, connect a 0.01 µF capacitor between IOUT and GND. This ensures stability with loads beyond 50 mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling.

Voltage Output Amplifier

The voltage output amplifier is capable of driving a load of 1 kΩ (for 0 V to 5 V and 0 V to 10 V ranges) and a load of 5 kΩ (for 0 V to 40 V range) and capacitive loads up to 2 µF (with an external compensation capacitor on the COMP1 and COMP2 pins). The source and sink capabilities of the output amplifier can be seen in Figure 15. The slew rate is 2 V/µs.

Internal to the device, there is a 2.5 MΩ resistor connected between VOUT and VSENSE+. If a fault condition occurs, these resistors act to protect the AD5751 by ensuring that the amplifier loop is closed so that the part does not enter into an open-loop condition.

The current and voltage are output on separate pins and cannot be output simultaneously. This allows the user to tie both the current and voltage output pins together and configure the end system as a single-channel output.

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 1 µF with the addition of a nonpolarized compensation capacitor between the COMP1 and COMP2 pins.

Without the compensation capacitor, up to 20 nF capacitive loads can be driven. Care should be taken to choose an appropriate value for the C_{COMP} capacitor. This capacitor, while allowing the AD5751 to drive higher capacitive loads and reduce overshoot, increases the settling time of the part and therefore affects the bandwidth of the system. Considered values of this capacitor should be in the range of 0 nF to 4 nF depending on the trade-off required between settling time, overshoot, and bandwidth.

POWER-ON STATE OF THE AD5751

On power-up, the AD5751 senses whether hardware or software mode is loaded and sets the power-up conditions accordingly.

In software SPI mode, the power-up state of the output is dependent on the state of the CLEAR pin. If the CLEAR pin is pulled high, the part powers up, driving an active 0 V on the output. If the CLEAR pin is pulled low, the part powers up with the voltage output channel in tristate mode. In both cases, the current output channel powers up in the tristate condition (0 mA). This allows the voltage and current outputs to be connected together if desired.

To put the part into normal operation, the user must set the OUTEN bit in the control register to enable the output and, in the same write, set the output range configuration using the R3 to R0 range bits. If the CLEAR pin is still high (active) during this write, the part automatically clears to its normal clear state as defined by the programmed range and by the CLRSEL pin or the CLRSEL bit (see the Asynchronous Clear (CLEAR) section for more details). The CLEAR pin must be taken low to operate the part in normal mode.

The CLEAR pin is typically driven directly from a microcontroller. In cases where the power supply for the AD5751 supply is independent of the microcontroller power supply, the user can connect a weak pull-up resistor to DVCC or a pull-down resistor to ground to ensure that the correct power-up condition is achieved independent of the microcontroller. A 10 kΩ pull-up/
pull-down resistor on the CLEAR pin should be sufficient for most applications.

If hardware mode is selected, the part powers up to the conditions defined by the R3 to R0 range bits and the status of the OUTEN or CLEAR pin. It is recommended to keep the output disabled when powering up the part in hardware mode.

DEFAULT REGISTERS AT POWER-ON

The AD5751 power-on-reset circuit ensures that all registers are loaded with zero code.

In software SPI mode, the part powers up with all outputs disabled (OUTEN bit = 0). The user must set the OUTEN bit in the control register to enable the output and, in the same write, set the output range configuration using the R3 to R0 bits.

If hardware mode is selected, the part powers up to the conditions defined by the R3 to R0 bits and the status of the OUTEN pin. It is recommended to keep the output disabled when powering up the part in hardware mode.

RESET FUNCTION

In software mode, the part can be reset using the $\overline{\text{RESET}}$ pin (active low) or the reset bit (reset = 1). A reset disables both the current and voltage outputs to their power-on condition. The user must write to the OUTEN bit to enable the output and, in the same write, set the output range configuration. The $\overline{\text{RESET}}$ pin is a level sensitive input; the part stays in reset mode as long as the $\overline{\text{RESET}}$ pin is low. The reset bit clears to 0 following a reset command to the control register.

In hardware mode, there is no reset. If using the part in hardware mode, the $\overline{\text{RESET}}$ pin should be tied high.

OUTEN

In software mode, the output can be enabled or disabled using the OUTEN bit in the control register. When the output is disabled, both the current and voltage channels go into tristate. The user must set the OUTEN bit to enable the output and simultaneously set the output range configuration.

In hardware mode, the output can be enabled or disabled using the OUTEN pin. When the output is disabled, both the current and voltage channels go into tristate. The user must write to the OUTEN pin to enable the output. It is recommended that the output be disabled when changing the ranges.

SOFTWARE CONTROL

Software control is enabled by connecting the HW SELECT pin to ground. In software mode, the AD5751 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 50 MHz. It is compatible with SPI, QSPI™, MICROWIRE, and DSP standards.

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device MSB first as a 16-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK. The input shift register consists of 16 control bits, as shown in Table 7. The timing diagram for this write operation is shown in Figure 2. The first three bits of the input shift register are used to set the hardware address of the AD5751 device on the printed circuit board (PCB). Up to eight devices can be addressed per board.

Bit D11, Bit D1, and Bit D0 must always be set to 0 during any write sequence.

Table 7. Input Shift Register Contents for a Write Operation—Control Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A2	A1	A0	R/$\overline{\text{W}}$	0	R3	R2	R1	R0	CLRSEL	OUTEN	Clear	RSET	Reset	0	0

Table 8. Input Shift Register Descriptions for Control Register

Bit	Description			
A2, A1, A0	Used in association with the AD2, AD1, and AD0 external pins to determine which part is being addressed by the system controller.			
	A2	**A1**	**A0**	**Function**
	0	0	0	Addresses part with Pin AD2 = 0, Pin AD1 = 0, Pin AD0 = 0.
	0	0	1	Addresses part with Pin AD2 = 0, Pin AD1 = 0, Pin AD0 = 1.
	0	1	0	Addresses part with Pin AD2 = 0, Pin AD1 = 1, Pin AD0 = 0.
	0	1	1	Addresses part with Pin AD2 = 0, Pin AD1 = 1, Pin AD0 = 1.
	1	0	0	Addresses part with Pin AD2 = 1, Pin AD1 = 0, Pin AD0 = 0.
	1	0	1	Addresses part with Pin AD2 = 1, Pin AD1 = 0, Pin AD0 = 1.
	1	1	0	Addresses part with Pin AD2 = 1, Pin AD1 = 1, Pin AD0 = 0.
	1	1	1	Addresses part with Pin AD2 = 1, Pin AD1 = 1, Pin AD0 = 1.
R/$\overline{\text{W}}$	Indicates a read from or a write to the addressed register.			

Bit	Description					
R3, R2, R1, R0	Selects the output configuration in conjunction with RSET.					
	RSET	**R3**	**R2**	**R1**	**R0**	**Output Configuration**
	0	0	0	0	0	4 mA to 20 mA (external 15 kΩ current sense resistor).
	0	0	0	0	1	0 mA to 20 mA (external 15 kΩ current sense resistor).
	0	0	0	1	0	0 mA to 24 mA (external 15 kΩ current sense resistor).
	0	0	0	1	1	Unused command. Do not program.
	0	0	1	0	0	Unused command. Do not program.
	0	0	1	0	1	0 V to 5 V.
	0	0	1	1	0	0 V to 10 V.
	0	0	1	1	1	Unused command. Do not program.
	0	1	0	0	0	Unused command. Do not program.
	0	1	0	0	1	0 V to 6.0 V (20% overrange).
	0	1	0	1	0	0 V to 12.0 V (20% overrange).
	0	1	0	1	1	Unused command. Do not program.
	0	1	1	0	0	Unused command. Do not program.
	0	1	1	0	1	Unused command. Do not program.
	0	1	1	1	0	0 V to 40 V.
	0	1	1	1	1	0 V to 44 V.
	1	0	0	0	0	4 mA to 20 mA (internal current sense resistor).
	1	0	0	0	1	0 mA to 20 mA (internal current sense resistor).
	1	0	0	1	0	0 mA to 24 mA (internal current sense resistor).
	1	0	0	1	1	Unused command. Do not program.
	1	0	1	0	0	Unused command. Do not program.
	1	0	1	0	1	0 V to 5 V.
	1	0	1	1	0	0 V to 10 V.
	1	0	1	1	1	Unused command. Do not program.
	1	1	0	0	0	Unused command. Do not program.
	1	1	0	0	1	0 V to 6.0 V (20% overrange).
	1	1	0	1	0	0 V to 12.0 V (20% overrange).
	1	1	0	1	1	Unused command. Do not program.
	1	1	1	0	0	Unused command. Do not program.
	1	1	1	0	1	3.92 mA to 20.4 mA (internal current sense resistor).
	1	1	1	1	0	0 mA to 20.4 mA (internal current sense resistor).
	1	1	1	1	1	0 mA to 24.5 mA (internal current sense resistor).
CLRSEL	Sets clear mode to zero scale or midscale. See the Asynchronous Clear (CLEAR) section.					
	CLRSEL	**Function**				
	0	Clear to 0 V.				
	1	Clear to midscale in unipolar mode; clear to zero scale in bipolar mode.				
OUTEN	Output enable bit. This bit must be set to 1 to enable the outputs.					
Clear	Software clear bit; active high.					
RSET	Select internal/external current sense resistor.					
	RSET	**Function**				
	1	Select internal current sense resistor; used with R3 to R0 bits to select range.				
	0	Select external current sense resistor; used with R3 to R0 bits to select range.				
Reset	Resets the part to its power-on state.					

Readback Operation

Readback mode is activated by selecting the correct device address (A2, A1, A0) and then setting the R/$\overline{W}$ bit to 1. By default, the SDO pin is disabled. After having addressed the AD5751 for a read operation, setting R/$\overline{W}$ to 1 enables the SDO pin and SDO data is clocked out on the 5th rising edge of SCLK. After the data has been clocked out on SDO, a rising edge on $\overline{SYNC}$ disables (tristate) the SDO pin again. Status register data (see Table 9) and control register data are both available during the same read cycle.

The status bits comprise four read-only bits. They are used to notify the user of specific fault conditions that occur, such as an open circuit or short circuit on the output, overtemperature error, or an interface error. If any of these fault conditions occur, a hardware FAULT is also asserted low, which can be used as a hardware interrupt to the controller.

See the Detailed Description of Features section for a full explanation of fault conditions.

HARDWARE CONTROL

Hardware control is enabled by connecting the HW SELECT pin to DVCC. In this mode, the R3, R2, R1, and R0 pins, in conjunction with the RSET pin, are used to configure the output range, as per Table 8.

In hardware mode, there is no status register. The fault conditions (open circuit, short circuit, and overtemperature) are available on Pin IFAULT, Pin VFAULT, and Pin TEMP. If any one of these fault conditions is set, a low is asserted on the specific fault pin. IFAULT, VFAULT, and TEMP are open-drain outputs and, therefore, can be connected together to allow the user to generate one interrupt to the system controller to communicate a fault. If hardwired in this way, it is not possible to isolate which fault occurred in the system.

TRANSFER FUNCTION

The AD5751 consists of an internal signal conditioning block that maps the analog input voltage to a programmed output range. The available analog input range is 0 V to 4.096 V.

For all ranges, both current and voltage, the AD5751 implements a straight linear mapping function, where 0 V maps to the lower end of the selected range and 4.096 V maps to the upper end of the selected range.

Table 9. Input Shift Register Contents for a Read Operation—Status Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A2	A1	A0	1	0	R3	R2	R1	R0	CLRSEL	OUTEN	RSET	PEC error	OVER TEMP	IOUT fault	VOUT fault

Table 10. Status Bit Options

Bit	Description
PEC Error	This bit is set if there is an interface error detected by CRC-8 error checking. See the Detailed Description of Features section.
OVER TEMP	This bit is set if the AD5751 core temperature exceeds approximately 150°C.
IOUT Fault	This bit is set if there is an open circuit on the IOUT pin.
VOUT Fault	This bit is set if there is a short circuit on the VOUT pin.

DETAILED DESCRIPTION OF FEATURES

OUTPUT FAULT ALERT—SOFTWARE MODE

In software mode, the AD5751 is equipped with one FAULT pin; this is an open-drain output allowing several AD5751 devices to be connected together to one pull-up resistor for global fault detection. In software mode, the FAULT pin is forced active low by any one of the following fault scenarios:

- The voltage at IOUT attempts to rise above the compliance range due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with window limits because this requires an actual output error before the fault output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the fault output activates slightly before the compliance limit is reached. Because the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain, and an output error does not occur before the fault output becomes active.
- A short is detected on the voltage output pin (VOUT). The short-circuit current is limited to 15 mA.
- An interface error is detected due to the packet error checking failure (PEC). See the Packet Error Checking section.
- The core temperature of the AD5751 exceeds approximately 150°C.

OUTPUT FAULT ALERT—HARDWARE MODE

In hardware mode, the AD5751 is equipped with three fault pins: VFAULT, IFAULT, and TEMP. These are open-drain outputs allowing several AD5751 devices to be connected together to one pull-up resistor for global fault detection. In hardware control mode, these fault pins are forced active by any one of the following fault scenarios:

- An open-circuit is detected. The voltage at IOUT attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with window limits because this requires an actual output error before the fault output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the fault output activates slightly before the compliance limit is reached. Because the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain, and an output error does not occur before the fault output becomes active. If this fault is detected, the IFAULT pin is forced low.
- A short is detected on the voltage output pin. The short-circuit current is limited to 15 mA. If this fault is detected, the VFAULT pin is forced low.
- The core temperature of the AD5751 exceeds approximately 150°C. If this fault is detected, the TEMP pin is forced low.

VOLTAGE OUTPUT SHORT-CIRCUIT PROTECTION

Under normal operation the voltage output sinks and sources up to 12 mA and maintains specified operation. The maximum current that the voltage output delivers is 15 mA; this is the short-circuit current.

ASYNCHRONOUS CLEAR (CLEAR)

CLEAR is an active high clear that allows the voltage output to be cleared to either zero-scale code or midscale code, and is user-selectable via the CLRSEL pin or the CLRSEL bit of the input shift register, as described in Table 8. (The clear select feature is a logical OR function of the CLRSEL pin and the CLRSEL bit). The current loop output clears to the bottom of its programmed range. When the CLEAR signal is returned low, the output returns to its programmed value or to a new programmed value. A clear operation can also be performed via the clear command in the control register.

Table 11. CLRSEL Options

	Output Clear Value	
CLRSEL	Unipolar Output Voltage Range	Unipolar Current Output Range
0	0 V	Zero-scale; for example: 4 mA on the 4 mA to 20 mA range 0 mA on the 0 mA to 20 mA
1	Midscale	Midscale; for example: 12 mA on the 4 mA to 20 mA range 10 mA on the 0 mA to 20 mA range

EXTERNAL CURRENT SETTING RESISTOR

Referring to Figure 1, R_{SET} is an internal sense resistor and is part of the voltage-to-current conversion circuitry. The nominal value of the internal current sense resistor is 15 kΩ. To allow for overrange capability in current mode, the user can also select the internal current sense resistor to be 14.7 kΩ, giving a nominal 2% overrange capability. This feature is available in the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current ranges.

The stability of the output current value over temperature is dependent on the stability of the value of R_{SET}. As a method of improving the stability of the output current over temperature, an external low drift resistor can be connected to the REXT1 and REXT2 pins of the AD5751, which can be used instead of the internal resistor. The external resistor is selected via the input shift register. If the external resistor option is not used, the REXT1 and REXT2 pins should be left floating.

PROGRAMMABLE OVERRANGE MODES

The AD5751 contains an overrange mode for most of the available ranges. The overranges are selected by configuring the R3, R1, R1, and R0 bits (or pins) accordingly.

In voltage mode, depending on selected range, the overranges are 10% or 20%, providing programmable output ranges of 0 V to 6 V, 0 V to 12 V, and 0 V to 44 V. The 0 V to 4.096 V analog input remains the same.

In current mode, the overranges are typically 2%. In current mode, the overrange capability is only available on three ranges, 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA. For these ranges, the analog input also remains the same (0 V to 4.096 V).

PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5751 offers the option of error checking based on an 8-bit (CRC-8) cyclic redundancy check. The device controlling the AD5751 should generate an 8-bit frame check sequence using the following polynomial:

$$C(x) = x_8 + x_2 + x_1 + 1$$

This is added to the end of the data-word, and 24 data bits are sent to the AD5751 before taking $\overline{\text{SYNC}}$ high. If the AD5751 receives a 24-bit data frame, it performs the error check when $\overline{\text{SYNC}}$ goes high. If the check is valid, then the data is written to the selected register. If the error check fails, the FAULT pin goes low and Bit D3 of the status register is set. After reading this register, this error flag is cleared automatically and the FAULT pin goes high again.

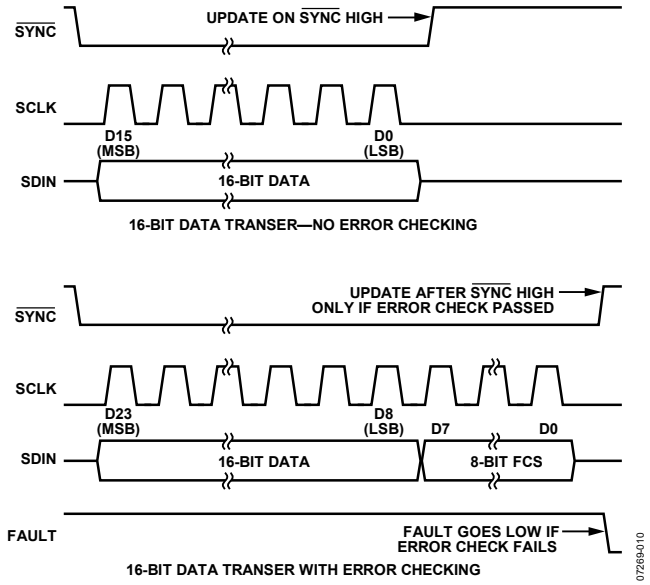


Figure 54. PEC Error Checking Timing

APPLICATIONS INFORMATION

TRANSIENT VOLTAGE PROTECTION

The AD5751 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5751 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as shown in Figure 55. The constraint on the resistor value is that during normal operation the output level at IOUT must remain within its voltage compliance limit of AV_{DD} – 2.75 V and the two protection diodes and resistor must have appropriate power ratings. Further protection can be added with transient voltage suppressors if needed.

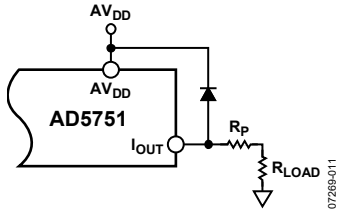


Figure 55. Output Transient Voltage Protection

THERMAL CONSIDERATIONS

It is important to understand the effects of power dissipation on the package and how it affects junction temperature. The internal junction temperature should not exceed 125°C. The AD5751 is packaged in a 32-lead, 5 mm × 5 mm LFCSP package. The thermal impedance, θ_{JA}, is 42°C/W. It is important that the devices not be operated under conditions that cause the junction temperature to exceed its limit. Worst-case conditions occur when the AD5751 are operated from the maximum AV_{DD} (55 V) and driving the maximum current (24 mA) directly to ground. The quiescent current of the AD5751 should also be taken into account, nominally ~4 mA. The following calculations estimate maximum power dissipation under these worst-case conditions, and determine maximum ambient temperature based on this. These figures assume that proper layout and grounding techniques are followed to minimize power dissipation, as outlined in the Layout Guidelines section.

Table 12. Thermal and Supply Considerations

Considerations	32-Lead LFCSP Package
Maximum allowed power dissipation when operating at an ambient temperature of 85°C	$\frac{T_{JMAX} - T_A}{\theta_{JA}} = \frac{125 - 85}{42} = 0.95\ \text{W}$
Maximum allowed ambient temperature when operating from a supply of 55 V and driving 24 mA directly to ground (include 4 mA for internal AD5751 current)	$T_{JMAX} - (P_D \times \theta_{JA}) = 125 - ((55 \times 0.028) \times 42) = 60.3°\text{C}$
Maximum allowed supply voltage when operating at an ambient temperature of 85°C and driving 24 mA directly to ground	$\frac{T_{JMAX} - T_A}{AI_{DD} \times \theta_{JA}} = \frac{125 - 85}{(0.028 \times 42)} = 34\ \text{V}$

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5751 is mounted should be designed so that the AD5751 lies on the analog plane.

The AD5751 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

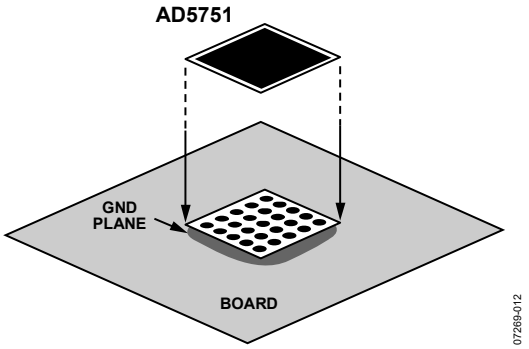


Figure 56. Paddle Connection to Board

The AD5751 has an exposed paddle beneath the device. Connect this paddle to the GND of the AD5751. For optimum performance, special considerations should be used to design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed paddle on the bottom of the package should be soldered to the corresponding thermal land paddle on the PCB (GND). Thermal vias should be designed into the PCB land paddle area to further improve heat dissipation.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler® family of products from Analog Devices, Inc., provides voltage isolation in excess of 5.0 kV. The serial loading structure of the AD5751 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 57 shows a 4-channel isolated interface to the AD5751 using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

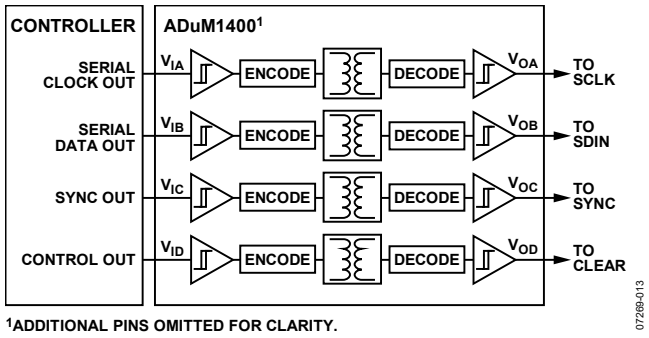


Figure 57. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5751 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communication channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a $\overline{\text{SYNC}}$ signal. The AD5751 requires a 16-bit data-word with data valid on the falling edge of SCLK.

OUTLINE DIMENSIONS

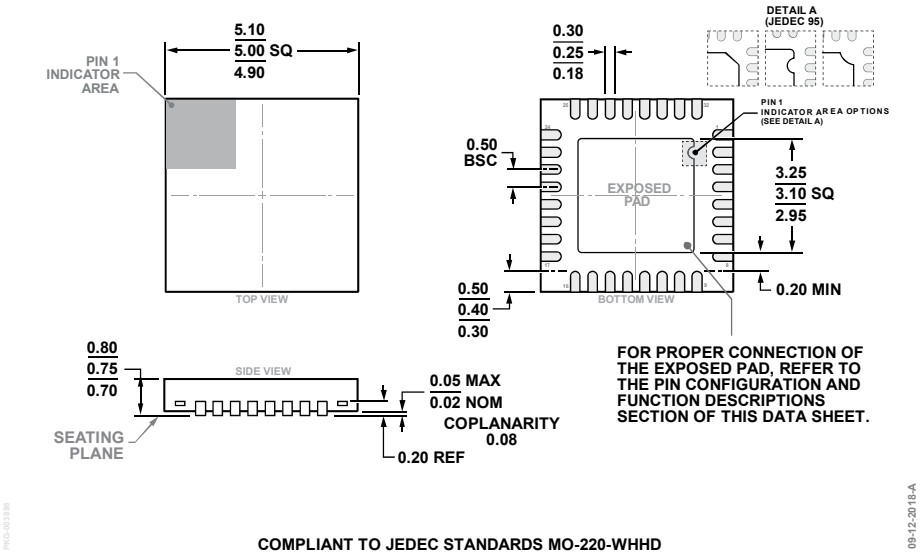


Figure 58. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5751ACPZ	−40°C to +105°C	32-Lead LFCSP	CP-32-7
AD5751ACPZ-REEL7	−40°C to +105°C	32-Lead LFCSP	CP-32-7
AD5751BCPZ	−40°C to +105°C	32-Lead LFCSP	CP-32-7

[1] Z = RoHS Compliant Part.

NOTES

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AD5751ACPZ AD5751BCPZ AD5751ACPZ-REEL7