- Serial read-out of multiple interconnected AS5045 devices using Daisy Chain mode
- Tolerant to magnet misalignment and airgap variations
- Wide temperature range: - 40ºC to 125ºC
- Small Pb-free package: SSOP-16 (5.3mm x 6.2mm)

Applications

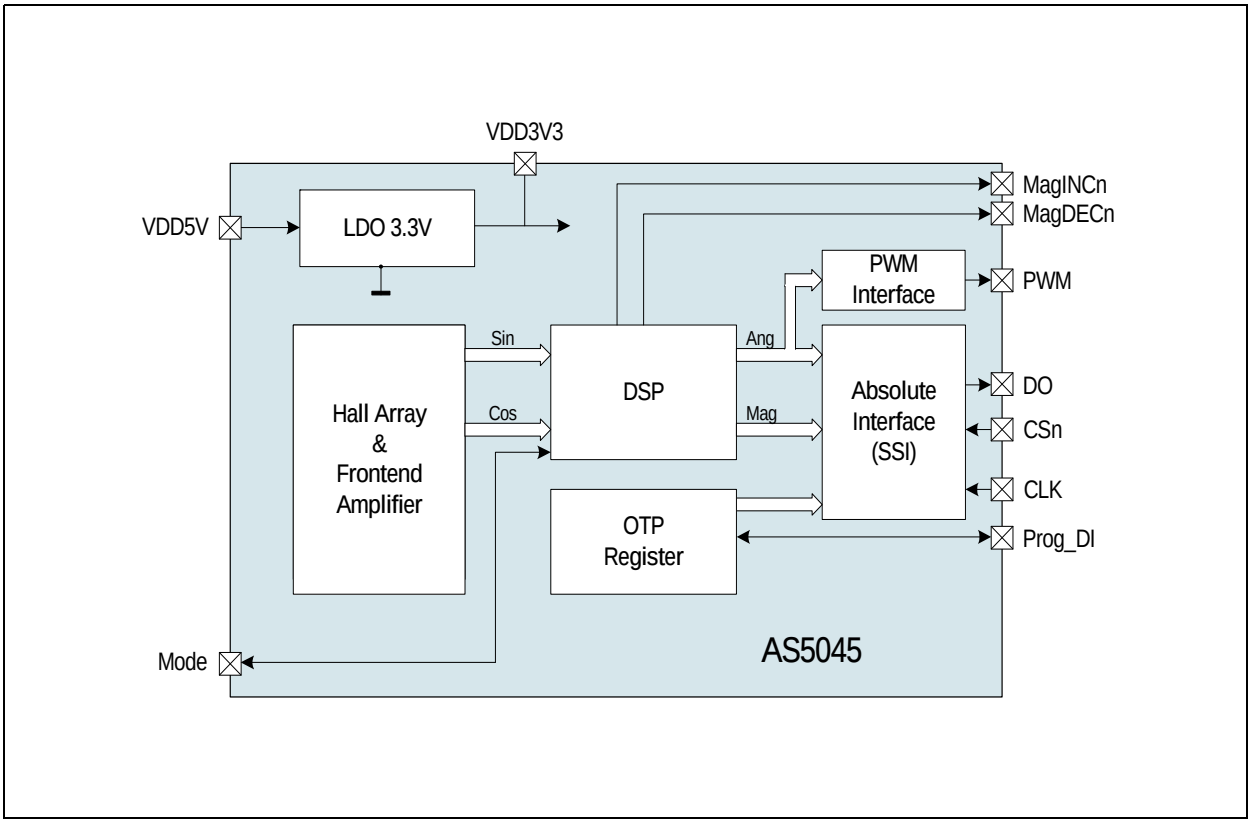
The AS5045 is ideal for industrial applications like

- Robotics,
- Stepper motor control,
- RC servo control and
- Replacement of high-end potentiometers.

Block Diagram

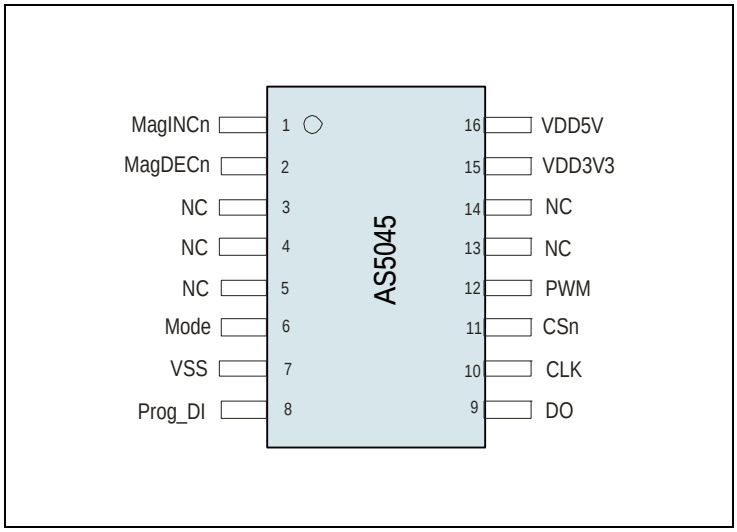
The functional blocks of this device are shown below:

Figure 2:
AS5045 Block Diagram



Pin Assignment

Figure 3:
Pin Assignment (Top View)



Pin Description

Figure 4 shows the description of each pin of the standard SSOP16 package (Shrink Small Outline Package, 16 leads, body size: 5.3mm x 6.2mmm; see Figure 3).

Pins 7, 15 and 16 supply pins, pins 3, 4, 5, 6, 13 and 14 are for internal use and must not be connected.

Pins 1 and 2 MagINCn and MagDECn are the magnetic field change indicators (magnetic field strength increase or decrease through variation of the distance between the magnet and the device). These outputs can be used to detect the valid magnetic field range. Furthermore those indicators can also be used for contact-less push-button functionality.

Pin 6 Mode allows switching between filtered (slow) and unfiltered (fast mode). This pin must be tied to VSS or VDD5V, and must not be switched after power up. See Mode Input Pin.

Pin 8 Prog is used to program the zero-position into the OTP. See Zero Position Programming.

This pin is also used as digital input to shift serial data through the device in Daisy Chain configuration. See Daisy Chain Mode.

Pin 11 Chip Select (CSn; active low) selects a device within a network of AS5045 magnetic position sensors and initiates serial data transfer. A logic high at CSn puts the data output pin (DO) to tri-state and terminates serial data transfer. This pin is also used for alignment mode and programming mode (see Figure 27).

Pin 12 PWM allows a single-wire output of the 10-bit absolute position value. The value is encoded into a pulse width modulated signal with 1µs pulse width per step (1µs to 4096µs over a full turn). By using an external low pass filter, the digital PWM signal is converted into an analog voltage, making a direct replacement of potentiometers possible.

Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	MagINCn	Digital output open drain	Magnet Field **Mag**nitude **INC**rease; active low, indicates a distance reduction between the magnet and the device surface (see Figure 16).
2	MagDECn		Magnet Field **Mag**nitude **DEC**rease; active low, indicates a distance increase between the device and the magnet see Figure 16).
3	NC	-	Must be left unconnected
4	NC	-	
5	NC	-	
6	Mode	-	Select between slow (low, VSS) and fast (high, VDD5V) mode. Internal pull-down resistor. Must be hard-wired on the PCB in application.
7	VSS	Supply pin	Negative Supply Voltage (GND)
8	Prog_DI	Digital input pull-down	OTP **Prog**ramming Input and Data Input for Daisy Chain mode. Internal pull-down resistor (~74kΩ). Connect to VSS if not used
9	DO	Digital output / tri-state	**D**ata **O**utput of Synchronous Serial Interface
10	CLK	Digital input, Schmitt-Trigger input	**Cl**oc**k** Input of Synchronous Serial Interface; Schmitt-Trigger input
11	CSn	Digital input pull-up, Schmitt-Trigger input	**C**hip **S**elect, active low; Schmitt-Trigger input, internal pull-up resistor (~50kΩ)
12	PWM	Digital output	**P**ulse **W**idth **M**odulation of approx. 244Hz; 1µs/step (optional 122Hz; 2µs/step)
13	NC	-	Must be left unconnected
14	NC	-	
15	VDD3V3	Supply pin	3V-Regulator Output, internally regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
16	VDD5V		Positive Supply Voltage, 3.0 to 5.5 V

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
DC supply voltage at pin VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3		5	V	
Input pin voltage	-0.3	VDD5V +0.3	V	Except VDD3V3
Input current (latchup immunity)	-100	100	mA	EIA/JESD78 Class II Level A
Electrostatic Discharge				
Electrostatic discharge	± 2		kV	JESD22-A114E
Temperature Ranges and Storage Conditions				
Storage temperature	-55	150	°C	Min -67°F; Max 302°F
Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative humidity non-condensing	5	85	%	
Moisture sensitivity level (MSL)	3			Represents a maximum floor life time of 168h

Electrical Characteristics

T_{AMB} = -40°C to 125°C, VDD5V = 3.0V to 3.6V (3V operation)
VDD5V = 4.5V to 5.5V (5V operation), unless otherwise noted.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Operating Conditions						
T_{AMB}	Ambient temperature	-40°F to 257°F	-40		125	°C
I_{supp}	Supply current			16	21	mA
VDD5V	Supply voltage at pin VDD5V	5V operation	4.5	5.0	5.5	V
VDD3V3	Voltage regulator output voltage at pin VDD3V3		3.0	3.3	3.6	
VDD5V	Supply voltage at pin VDD5V	3.3V operation (pin VDD5V and VDD3V3 connected)	3.0	3.3	3.6	V
VDD3V3	Supply voltage at pin VDD3V3		3.0	3.3	3.6	
DC Characteristics CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = Internal Pull-Up)						
V_{IH}	High level input voltage	Normal operation	0.7 * VDD5V			V
V_{IL}	Low level input voltage				0.3 * VDD5V	V
$V_{Ion-}V_{Ioff}$	Schmitt Trigger hysteresis		1			V
I_{LEAK}	Input leakage current	CLK only	-1		1	µA
I_{IL}	Pull-up low level input current	CSn only, VDD5V: 5.0V	-30		-100	µA
DC Characteristics CMOS / Program Input: Prog						
V_{IH}	High level input voltage		0.7 * VDD5V		VDD5V	V
VPROG	High level input voltage	During programming	Refer to programming conditions (Figure 10)			V
V_{IL}	Low level input voltage				0.3 * VDD5V	V
I_{IL}	High level input current	VDD5V: 5.5V	30		100	µA

Symbol	Parameter	Condition	Min	Typ	Max	Units
DC Characteristics CMOS Output Open Drain: MagINCn, MagDECn						
V_{OL}	Low level output voltage				VSS+0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	
I_{OZ}	Open drain leakage current				1	µA
DC Characteristics CMOS Output: PWM						
V_{OH}	High level output voltage		VDD5V-0.5			V
V_{OL}	Low level output voltage				VSS+0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	
DC Characteristics Tri-state CMOS Output: DO						
V_{OH}	High level output voltage		VDD5V-0.5			V
V_{OL}	Low level output voltage				VSS+0.4	V
I_O	Output current	VDD5V: 4.5V			4	mA
		VDD5V: 3V			2	
I_{OZ}	Tri-state leakage current				1	µA

Magnetic Input Specification

Two-pole cylindrical diametrically magnetized source:

Figure 7:
Magnetic Input Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
d_{mag}	Diameter	Recommended magnet: Ø 6mm x 2.5mm for cylindrical magnets	4	6		mm
t_{mag}	Thickness		2.5			mm
B_{pk}	Magnetic input field amplitude	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm	45		75	mT
B_{off}	Magnetic offset	Constant magnetic stray field			± 10	mT
	Field non-linearity	Including offset gradient			5	%
f_{mag_abs}	Input frequency (rotational speed of magnet)	146 rpm @ 4096 positions/rev.; fast mode			2.44	Hz
		36.6rpm @ 4096 positions/rev.; slow mode			0.61	
Disp	Displacement radius	Maximum offset between defined device center and magnet axis			0.25	mm
Ecc	Eccentricity	Eccentricity of magnet center to rotational axis			100	µm

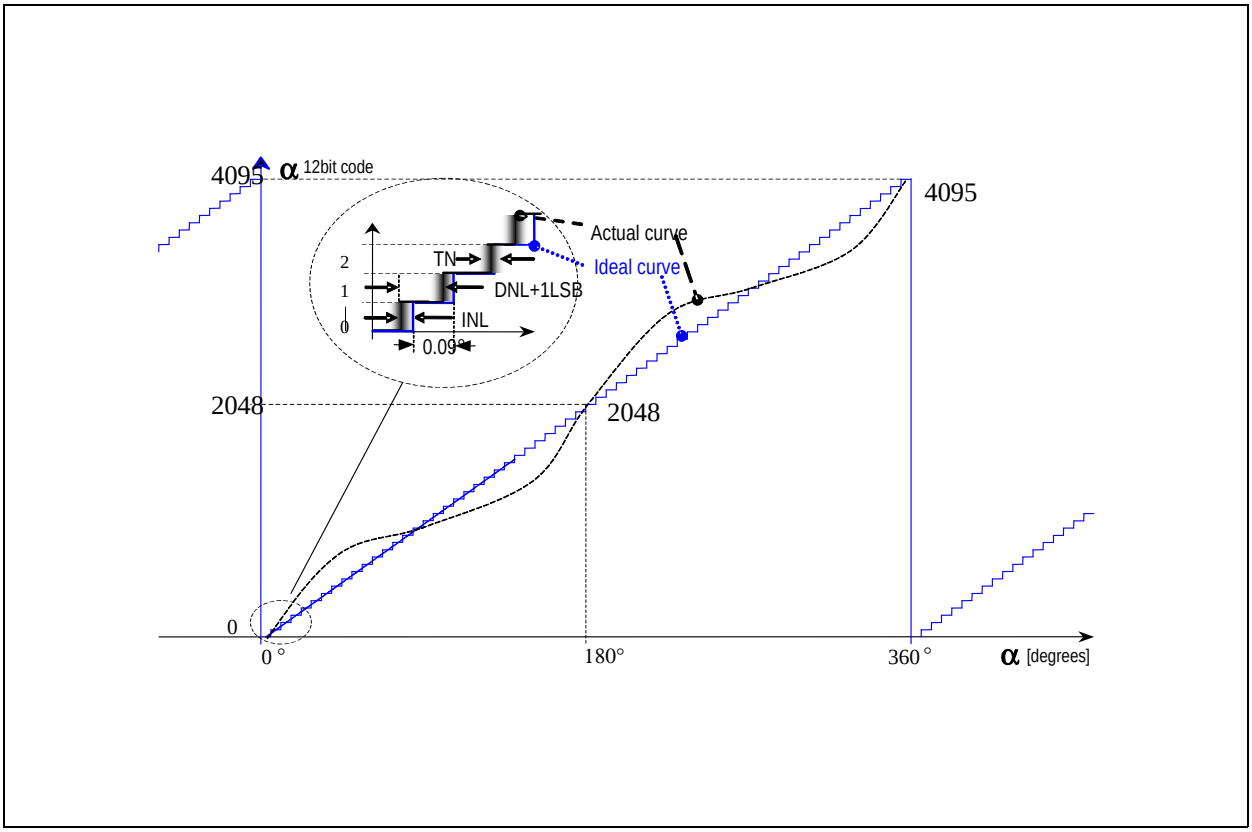
Electrical System Specifications

Figure 8:
Input Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution	0.088 deg			12	bit
INL_{opt}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} = 25°C			± 0.5	deg
INL_{temp}		Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} = -40°C to 125°C			± 0.9	
INL	Integral non-linearity	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration, T_{AMB} = -40°C to 125°C			± 1.4	deg
DNL	Differential non-linearity	12-bit, No missing codes			±0.044	deg
TN	Transition noise	1 sigma, fast mode (MODE = 1)			0.06	deg RMS
		1 sigma, slow mode (MODE=0 or open)			0.03	
V_{ON}	Power-on reset thresholds: On voltage; 300mV typ. hysteresis	DC supply voltage 3.3V (VDD3V3)	1.37	2.2	2.9	V
V_{OFF}	Power-on reset thresholds: Off voltage; 300mV typ. hysteresis		1.08	1.9	2.6	
t_{PwrUp}	Power-up time	Fast mode (Mode = 1); until status bit OCF = 1			20	ms
		Slow mode (Mode = 0 or open); until OCF = 1			80	
t_{delay}	System propagation delay absolute output : delay of ADC, DSP and absolute interface	Fast mode (MODE=1)			96	µs
		Slow mode (MODE=0 or open)			384	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_S	Internal sampling rate for absolute output:	T_{AMB} = 25°C, slow mode (MODE=0 or open)	2.48	2.61	2.74	kHz
		T_{AMB} = -40°C to 125°C, slow mode (MODE=0 or open)	2.35	2.61	2.87	
f_S	Internal sampling rate for absolute output	T_{AMB} = 25°C, fast mode (MODE = 1)	9.90	10.42	10.94	kHz
		T_{AMB} = -40°C to 125°C, fast mode (MODE = 1)	9.38	10.42	11.46	
CLK	Read-out frequency	Maximum clock frequency to read out serial data			1	MHz

Figure 9:
Integral and Differential Non-Linearity (Example)



Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position.

Timing Characteristics

Figure 10:
Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Synchronous Serial Interface (SSI)						
$t_{DO\ active}$	Data output activated (logic high)	Time between falling edge of CSn and data output activated			100	ns
$t_{CLK\ FE}$	First data shifted to output register	Time between falling edge of CSn and first falling edge of CLK	500			ns
$T_{CLK\ /\ 2}$	Start of data output	Rising edge of CLK shifts out one bit at a time	500			ns
$t_{DO\ valid}$	Data output valid	Time between rising edge of CLK and data output valid	357	375	394	ns
$t_{DO\ tristate}$	Data output tristate	After the last bit DO changes back to “tristate”			100	ns
t_{CSn}	Pulse width of CSn	CSn = high; To initiate read-out of next angular position	500			ns
f_{CLK}	Read-out frequency	Clock frequency to read out serial data	>0		1	MHz
Pulse Width Modulation Output						
f_{PWM}	PWM frequency	Signal period = 4097µs ±5% at T_{AMB} = 25°C	232	244	256	Hz
		Signal period = 4097µs ±10% at T_{AMB} = -40 to 125°C	220	244	268	
PW_{MIN}	Minimum pulse width	Position 0d; Angle 0°	0.95	1	1.05	µs
PW_{MAX}	Maximum pulse width	Position 4095d; Angle 359.91°	3891	4096	4301	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Programming Conditions						
$t_{Prog\ enable}$	Programming enable time	Time between rising edge at Prog pin and rising edge of CSn	2			µs
$t_{Data\ in}$	Write data start		2			µs
$t_{Data\ in\ valid}$	Write data valid	Write data at the rising edge of CLK_{PROG}	250			ns
$t_{Load\ PROG}$	Load programming data		3			µs
t_{PrgR}	Rise time of V_{PROG} before CLK_{PROG}		0			µs
t_{PrgH}	Hold time of V_{PROG} after CLK_{PROG}		0		5	µs
CLK_{PROG}	Write data – programming CLK_{PROG}	Ensure that V_{PROG} is stable with rising edge of CLK			250	kHz
t_{PROG}	CLK pulse width	During programming; 16 clock cycles	1.8	2	2.2	µs
$t_{PROG\ finished}$	Hold time of V_{PROG} after programming	Programmed data is available after next power-on	2			µs
V_{PROG}	Programming voltage, pin PROG	Must be switched off after zapping	7.3	7.4	7.5	V
$V_{ProgOff}$	Programming voltage off level	Line must be discharged to this level	0		1	V
I_{PROG}	Programming current	During programming			130	mA
CLK_{Aread}	Analog read CLK	Analog Readback mode			100	kHz
$V_{programmed}$	Programmed Zener voltage (log.1)	V_{Ref}-V_{PROG} during Analog Readback mode (see Analog Readback Mode)			100	mV
$V_{unprogrammed}$	Unprogrammed Zener voltage (log. 0)		1			V

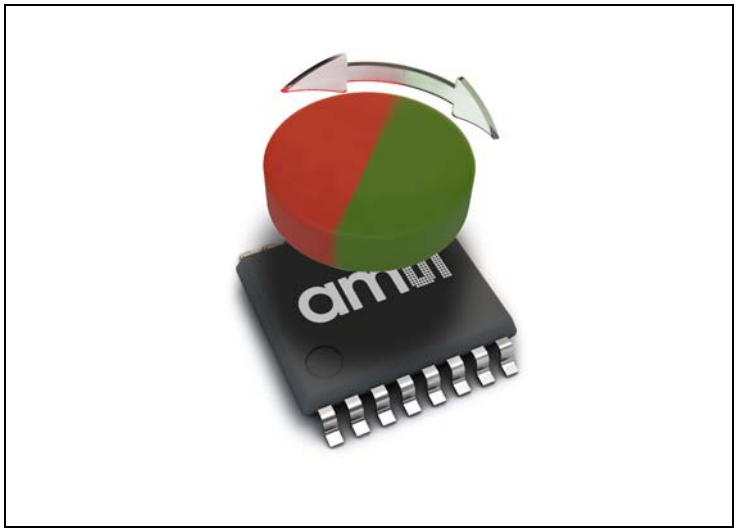
Detailed Description

The AS5045 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip. The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5045 provides accurate high-resolution absolute angular position information. For this purpose a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals. The DSP is also used to provide digital information at the outputs MagINCn and MagDECn that indicate movements of the used magnet towards or away from the device's surface. A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 30).

The AS5045 senses the orientation of the magnetic field and calculates a 12-bit binary code. This code can be accessed via a Synchronous Serial Interface (SSI). In addition, an absolute angular representation is given by a Pulse Width Modulated signal at pin 12 (PWM). This PWM signal output also allows the generation of a direct proportional analogue voltage, by using an external Low-Pass-Filter. The AS5045 is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

Figure 11:
Typical Arrangement of AS5045 and Magnet



Mode Input Pin

The mode input pin activates or deactivates an internal filter that is used to reduce the analog output noise. Activating the filter (Mode pin = LOW) provides a reduced output noise of 0.03° rms. At the same time, the output delay is increased to 384µs. This mode is recommended for high precision, low speed applications.

Deactivating the filter (Mode pin = HIGH) reduces the output delay to 96µs and provides an output noise of 0.06° rms. This mode is recommended for higher speed applications.

The MODE pin should be set at power-up. A change of the mode during operation is not allowed.

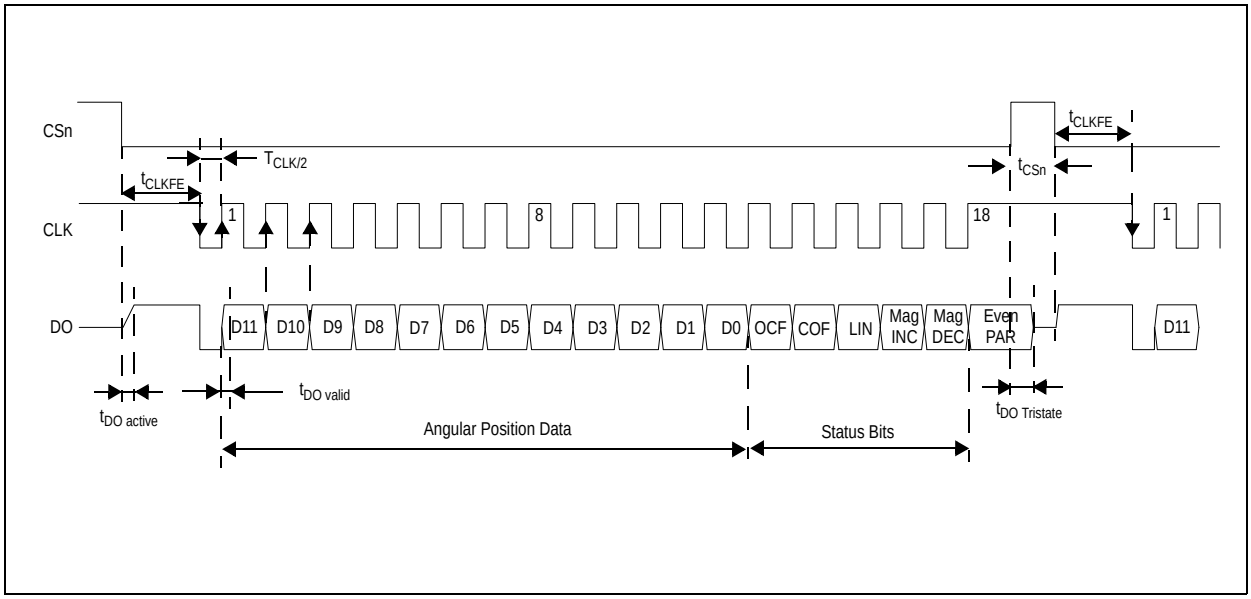
Switching the Mode pin affects the following parameters.

Figure 12:
Slow and Fast Mode Parameters 12-Bit Absolute Angular Position Output

Parameter	Slow Mode (Mode = Low)	Fast Mode (Mode = High, VDD5V)
Sampling rate	2.61 kHz (384 µs)	10.42 kHz (96µs)
Transition noise (1 sigma)	≤ 0.03° rms	≤ 0.06° rms
Output delay	384µs	96µs
Max. speed @ 4096 samples/rev. Max. speed @ 1024 samples/rev. Max. speed @ 256 samples/rev. Max. speed @ 64 samples/rev.	38 rpm 153 rpm 610 rpm 2441 rpm	153 rpm 610 rpm 2441 rpm 9766 rpm

Synchronous Serial Interface (SSI)

Figure 13:
Synchronous Serial Interface with Absolute Angular Position Data



If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

- After a minimum time $t_{CLK\ FE,}$ data is latched into the output shift register with the first falling edge of CLK.
- Each subsequent rising CLK edge shifts out one bit of data.
- The serial word contains 18 bits, the first 12 bits are the angular information D[11:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease).
- A subsequent measurement is initiated by a "high" pulse at CSn with a minimum duration of $t_{CSn.}$

Data Content

D11:D0 – absolute angular position data (MSB is clocked out first)

OCF – (**O**ffset **C**ompensation **F**inished), logic high indicates the finished Offset Compensation Algorithm

COF – (**C**ORDIC **O**ver**f**low), logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN – (**Lin**earity Alarm), logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D9:D0 may still be used, but can contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Even Parity – Bit for transmission error detection of bits 1 …17 (D11 …D0, OCF, COF, LIN, MagINC, MagDEC). Placing the magnet above the chip, angular values increase in clockwise direction by default.

Data D11:D0 is valid, when the status bits have the following configurations.

Figure 14:
Status Bit Outputs

OCF	COF	LIN	MagINC	MagDEC	Parity
1	0	0	0	0	Even checksum of bits 1:15
			0	1	
			1	0	
			1[(1)]	1[(1)]	

Note(s):

1. MagInc=MagDec=1 is only recommended in YELLOW mode (see Figure 16).

Z-Axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5045 provides several options of detecting movement and distance of the magnet in the Z-direction. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins 1 and 2) and as status bits in the serial data stream. Additionally, an OTP programming option is available with bit MagCompEn (see Figure 23) that enables additional features.

In the default state, the status bits MagINC, MagDec and pins MagINCn, MagDECn have the following function.

Figure 15:
Magnetic Field Strength Variation Indicator

Status Bits		Hardware Pins		OTP: Mag CompEn = 0 (default)
MagINC	MagDEC	MagINCn	MagDECn	Description
0	0	Off	Off	No distance change Magnetic input field OK (in range, ~45mT to 75mT)
0	1	Off	On	Distance increase; pull-function. This state is dynamic and only active while the magnet is moving away from the chip.
1	0	On	Off	Distance decrease; push- function. This state is dynamic and only active while the magnet is moving towards the chip.
1	1	On	On	Magnetic field is ~<45mT or >~75mT. It is still possible to operate the AS5045 in this range, but not recommended

When bit MagCompEn is programmed in the OTP, the function of status bits MagINC, MagDec and pins MagINCn, MagDECn is changed to the following function.

Figure 16:
Magnetic Field Strength Red-Yellow-Green Indicator (OTP Option)

Status Bits			Hardware Pins		OTP: Mag CompEn = 1 (Red-Yellow-Green Programming Option)
Mag INC	Mag DEC	LIN	Mag INCn	Mag DECn	Description
0	0	0	Off	Off	No distance change Magnetic input field OK (GREEN range, ~45mT to 75mT)
1	1	0	On	Off	YELLOW range: magnetic field is ~ 25mT to 45mT or ~75mT to 135mT. The AS5045 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	On	RED range: magnetic field is ~<25mT or >~135mT. It is still possible to operate the AS5045 in the red range, but not recommended.
All other combinations			n/a	n/a	Not available

Note(s):

1. Pin 1 (MagINCn) and pin 2 (MagDECn) are active low via open drain output and require an external pull-up resistor. If the magnetic field is in range, both outputs are turned off.

The two pins may also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see Figure 15 and Figure 16).

Daisy Chain Mode

The Daisy Chain mode allows connection of several AS5045's in series, while still keeping just one digital input for data transfer (see "Data IN" in Figure 17). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (PROG; pin 8) of the subsequent device. An RC filter must be implemented between each PROG pin of device n and DO pin of device n+1, to prevent then magnetic position sensors to enter the alignment mode, in case of ESD discharge, long cables, not conform signal levels or shape. Using the values R=100R and C=1nF allow a max. CLK frequency of 1MHz on the whole chain. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is n * (18+1) bits: For e.g., 38 bit for two devices, 57 bit for three devices, etc.

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D11), etc. (see Figure 18).

Figure 17:
Daisy Chain Hardware Configuration

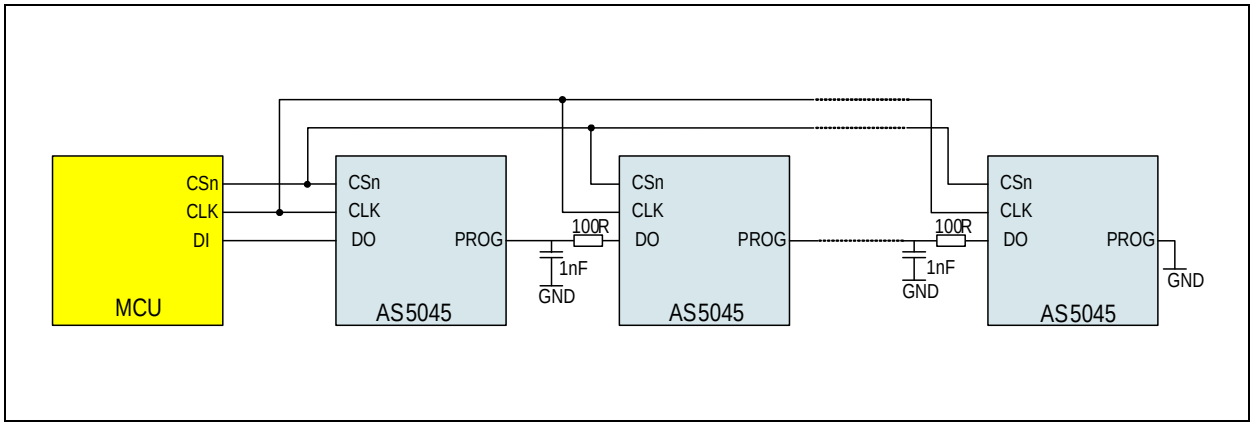
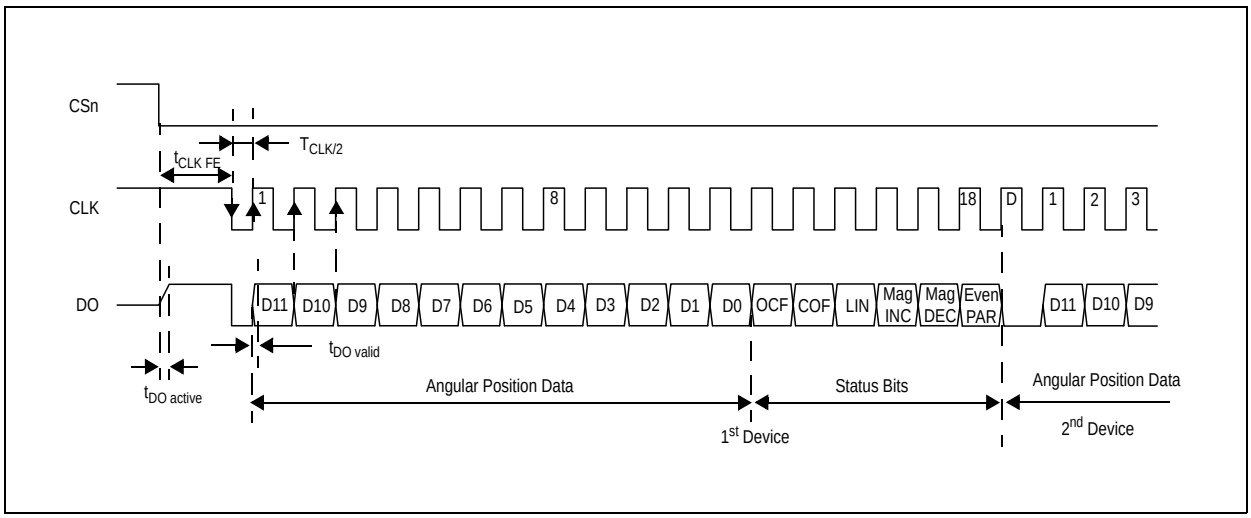


Figure 18:
Daisy Chain Mode Data Transfer



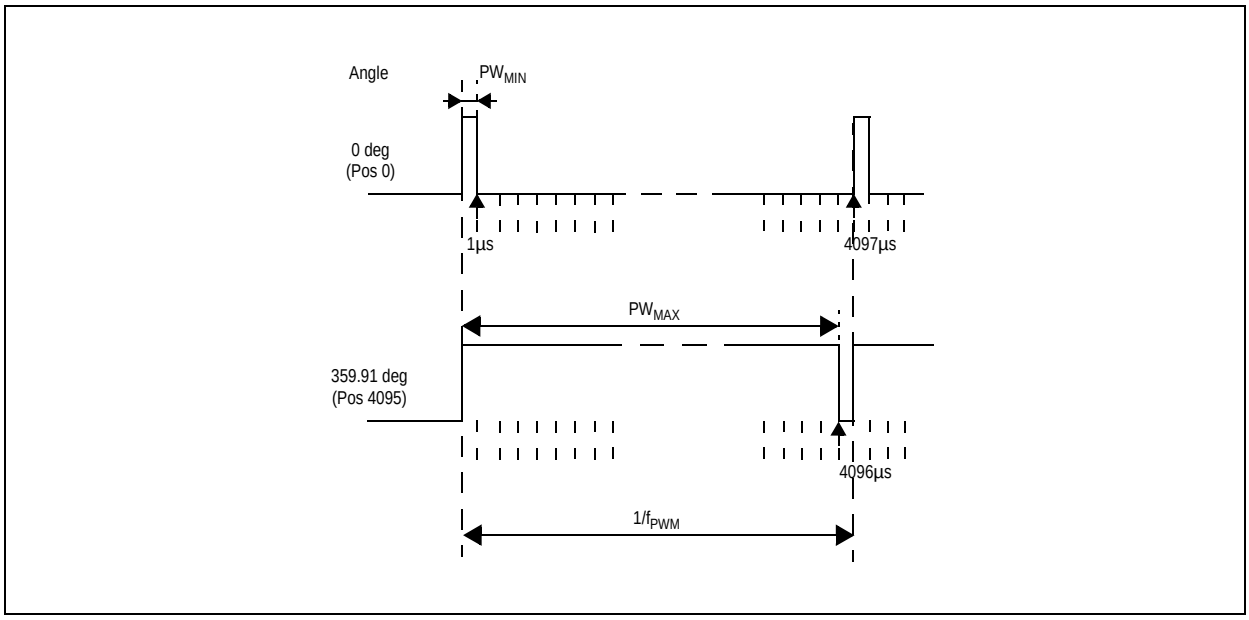
Pulse Width Modulation (PWM) Output

The AS5045 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle:

(EQ1)
$$Position = \frac{t_{on} \cdot 4097}{\left(t_{on} + t_{off}\right)} - 1$$

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be cancelled by measuring the complete duty cycle as shown above.

Figure 19:
PWM Output Signal



Changing the PWM Frequency

The PWM frequency of the AS5045 can be divided by two by setting a bit (PWMhalfEN) in the OTP register (see Programming the AS5045). With PWMhalfEN = 0, the PWM timing is as shown in Figure 20.

Figure 20:
PWM Signal Parameters (Default mode)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	244	Hz	Signal period: 4097µs
PW_{MIN}	MIN pulse width	1	µs	- Position 0d - Angle 0 deg
PW_{MAX}	MAX pulse width	4096	µs	- Position 4095d - Angle 359.91 deg

When PWMhalfEN = 1, the PWM timing is as shown in Figure 21.

Figure 21:
PWM Signal Parameters with Half Frequency (OTP Option)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	122	Hz	Signal period: 8194µs
PW_{MIN}	MIN pulse width	2	µs	• Position 0d • Angle 0 deg
PW_{MAX}	MAX pulse width	8192	µs	• Position 4095d • Angle 359.91 deg

Analog Output

An analog output can be generated by averaging the PWM signal, using an external active or passive low pass filter.

The analog output voltage is proportional to the angle: 0°= 0V; 360° = VDD5V.

Using this method, the AS5045 can be used as direct replacement of potentiometers.

Figure 22:
Simple 2nd Order Passive RC Low Pass Filter

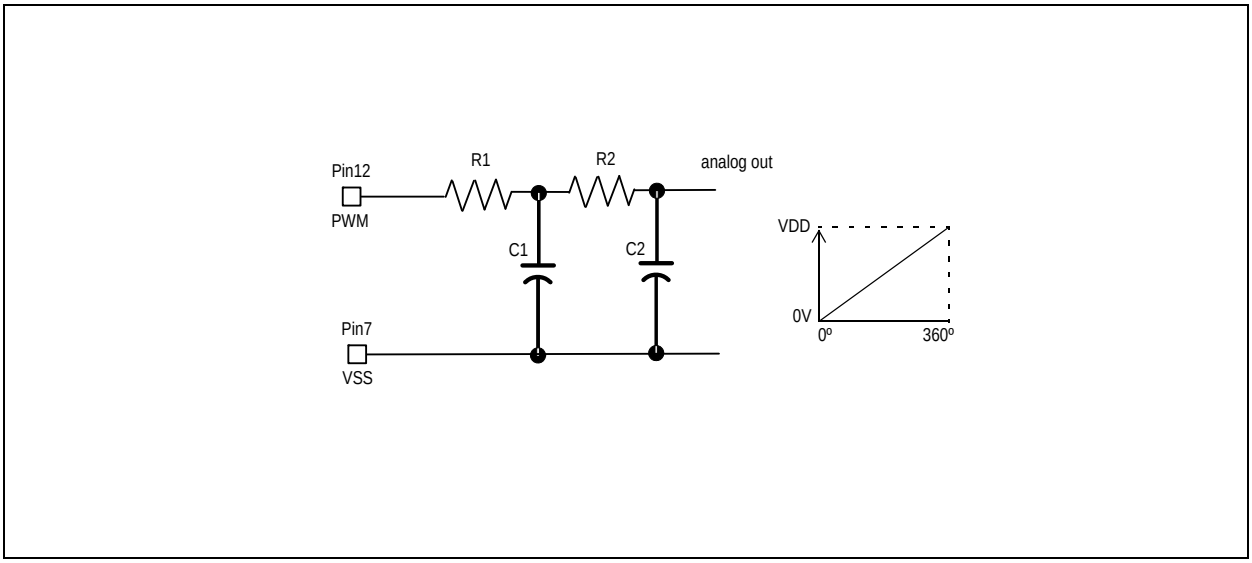


Figure 22 shows an example of a simple passive low pass filter to generate the analog output.

(EQ2) *R1, R2 ≥ 4k7 C1, C2 ≥ 1µF / 6V*

R1 should be greater than or equal to 4k7 to avoid loading of the PWM output. Larger values of Rx and Cx will provide better filtering and less ripple, but will also slow down the response time.

The benefits of AS5045 are as follows:

- Complete system-on-chip
- Flexible system solution provides absolute and PWM outputs simultaneously
- Ideal for applications in harsh environments due to contactless position sensing
- No calibration required

Programming the AS5045

After power-on, programming the AS5045 is enabled with the rising edge of CSn and Prog = logic high. 16 bit configuration data must be serially shifted into the OTP register via the Prog pin. The first "CCW" bit is followed by the zero position data (MSB first) and the Mode setting bits. Data must be valid at the rising edge of CLK (see Figure 23).

After writing the data into the OTP register it can be permanently programmed by rising the Prog pin to the programming voltage V_{PROG}. 16 CLK pulses (t_{PROG}) must be applied to program the fuses (see Figure 24). To exit the programming mode, the chip must be reset by a power-on-reset. The programmed data is available after the next power-up.

Note(s): During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals Prog and VSS must be kept as short as possible. The maximum wire length between the V_{PROG} switching transistor and pin Prog should not exceed 50mm (2 inches). To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins VPROG and VSS. This capacitor is only required for programming, it is not required for normal operation. The clock timing t_{clk} must be selected at a proper rate to ensure that the signal Prog is stable at the rising edge of CLK (see Figure 23). Additionally, the programming supply voltage should be buffered with a 10µF capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming. The specified programming voltage at pin Prog is 7.3 ~ 7.5V. Refer to programming conditions in Figure 10.

To compensate for the voltage drop across the V_{PROG} switching transistor, the applied programming voltage may be set slightly higher (7.5 ~ 8.0V, see Figure 25).

OTP Register Contents

CCW: Counter Clockwise Bit

ccw=0 – angular value increases in clockwise direction

ccw=1 – angular value increases in counter clockwise direction

Z [11:0]: Programmable Zero Position

PWM dis: Disable PWM output

MagCompEn: When set, activates LIN alarm both when magnetic field is too high and too low (see Figure 16)

PWMhalfEn: When set, PWM frequency is 122Hz or 2µs / step (when PWMhalfEN = 0, PWM frequency is 244Hz, 1µs / step)

Zero Position Programming

Zero position programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new zero position.

For zero position programming, the magnet is turned to the mechanical zero position (e.g. the “off”-position of a rotary switch) and the actual angular value is read.

This value is written into the OTP register bits Z11:Z0 (see Figure 23) and programmed (see Figure 24).

The zero position value may also be modified before programming, e.g. to program an electrical zero position that is 180° (half turn) from the mechanical zero position, just add 2048 to the value read at the mechanical zero position and program the new value into the OTP register.

Repeated OTP Programming

Although a single AS5045 OTP register bit can be programmed only once (from 0 to 1), it is possible to program other, unprogrammed bits in subsequent programming cycles. However, a bit that has already been programmed should not be programmed twice. Therefore it is recommended that bits that are already programmed are set to “0” during a programming cycle.

Non-Permanent Programming

It is also possible to re-configure the AS5045 in a non-permanent way by overwriting the OTP register.

This procedure is essentially a “Write Data” sequence (see Figure 23) without a subsequent OTP programming cycle.

The “Write Data” sequence may be applied at any time during normal operation. This configuration remains set while the power supply voltage is above the power-on reset level (see Electrical System Specifications).

See Application Note AN5000-20 for further information.

Figure 23:
Programming Access – Write Data (Section of Figure 24)

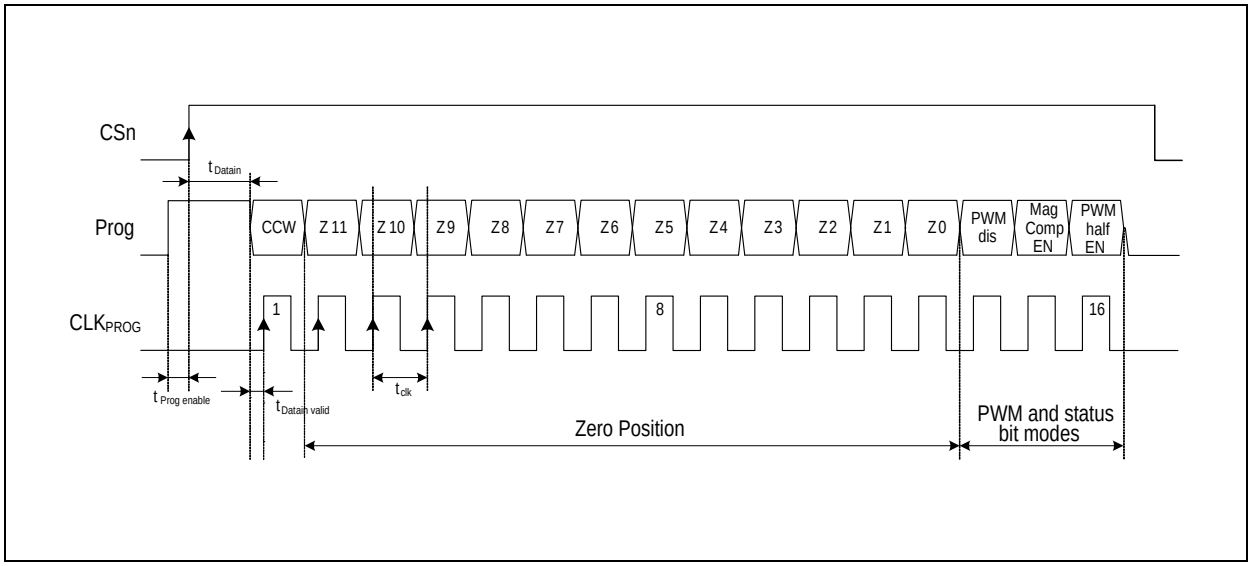


Figure 24:
Complete Programming Sequence

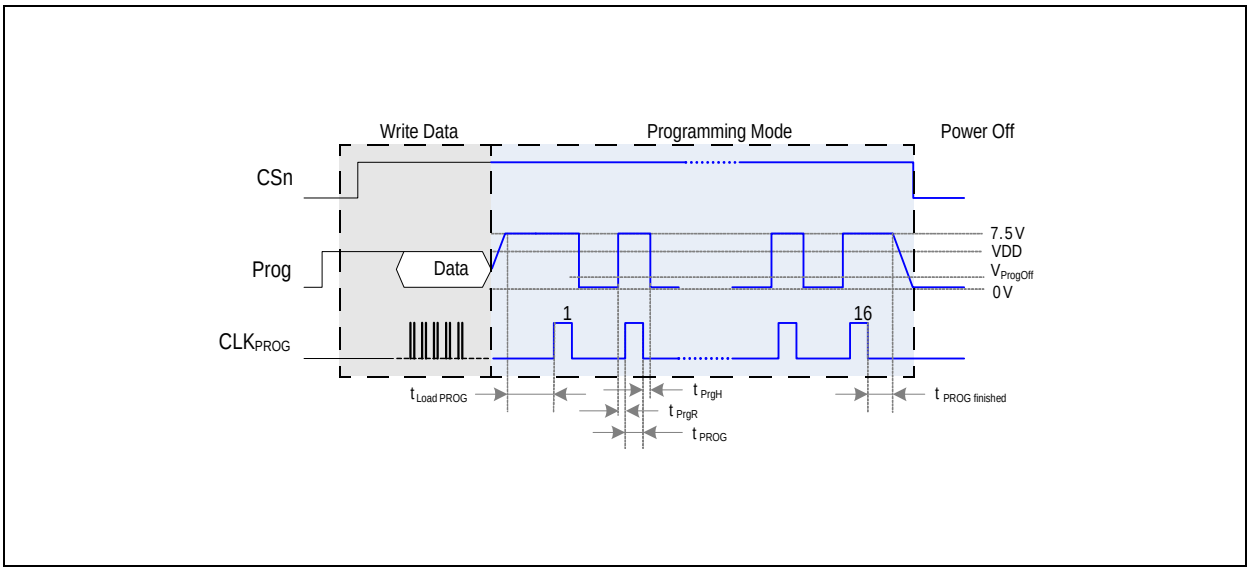
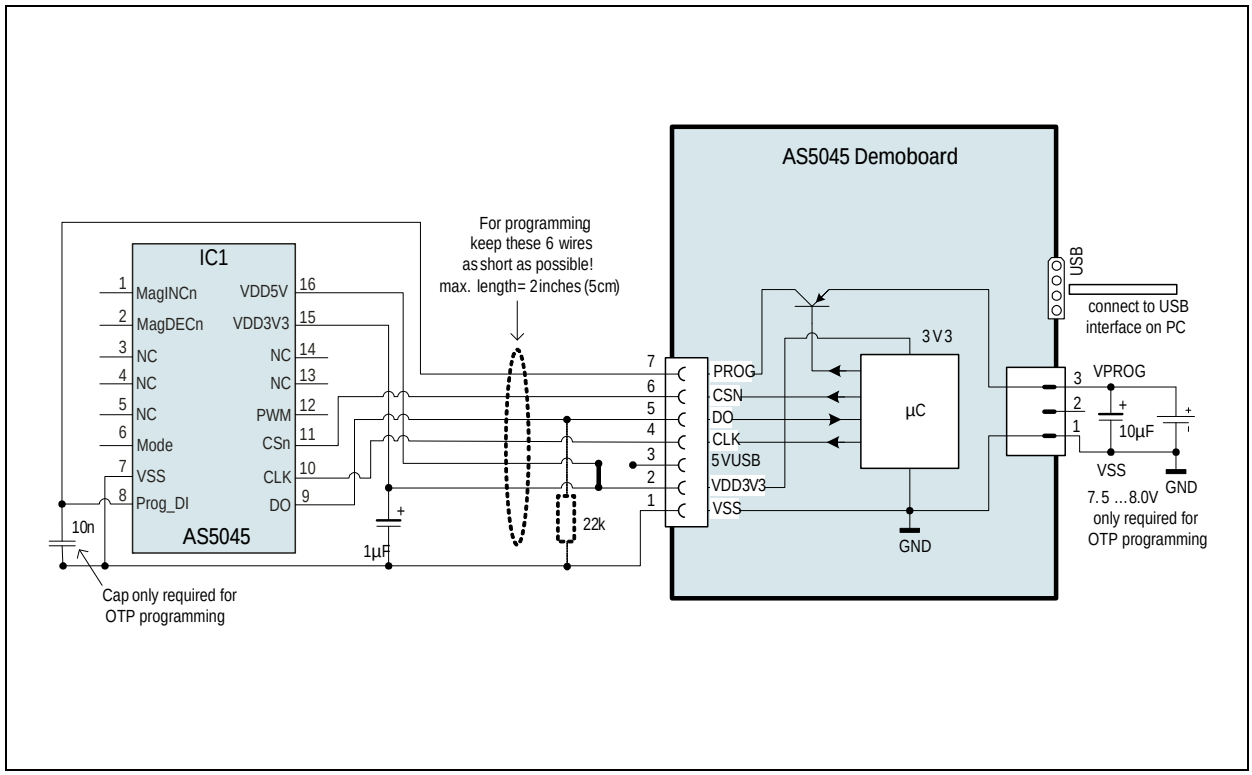


Figure 25:
OTP Programming Connection of AS5045 (Shown with AS5045 Demoboard)



Analog Readback Mode

Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current.

The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA). This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly.

In order to verify the quality of the programmed bit, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5045 in Analog Readback Mode, a digital sequence must be applied to pins CSn, PROG and CLK as shown in Figure 26. The digital level for this pin depends on the supply configuration (3.3V or 5V) (see 3.3V / 5V Operation).

The second rising edge on CSn (OutpEN) changes pin PROG to a digital output and the log. high signal at pin PROG must be removed to avoid collision of outputs (grey area in Figure 26).

The following falling slope of CSn changes pin PROG to an analog output, providing a reference voltage V_{ref}, that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits.
Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming

(see Figure 23: Md0-MD1-Div0,Div1-Indx-Z0…Z11, ccw).

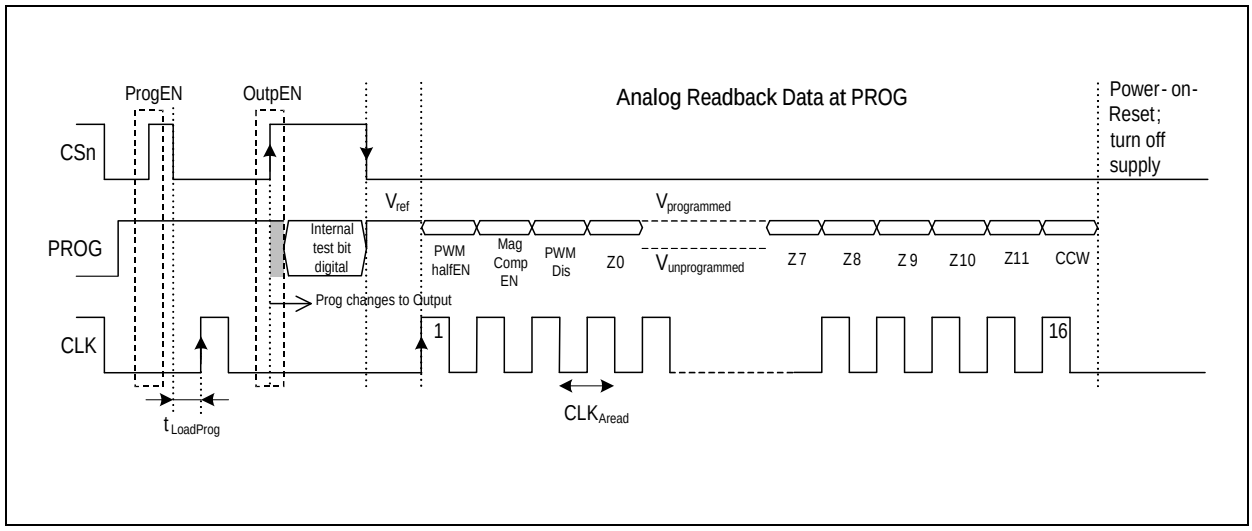
If a capacitor is connected to pin PROG, it should be removed during analog readback mode to allow a fast readout rate. If the capacitor is not removed the analog voltage will take longer to stabilize due to the additional capacitance.

The measured analog voltage for each bit must be subtracted from the previously measured V_{ref}, and the resulting value gives an indication on the quality of the programmed bit: a reading of <100mV indicates a properly programmed bit and a reading of >1V indicates a properly unprogrammed bit.

A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up.

Following the 18th clock (after reading bit "ccw"), the chip must be reset by disconnecting the power supply.

Figure 26:
OTP Register Analog Read



Alignment Mode

The alignment mode simplifies centering the magnet over the center of the chip to gain maximum accuracy.

Alignment mode can be enabled with the falling edge of CSn while Prog = logic high (see Figure 27). The Data bits D11-D0 of the SSI change to a 12-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum.

Under normal conditions, a properly aligned magnet will result in a reading of less than 128 over a full turn.
The MagINCn and MagDECn indicators will be = 1 when the alignment mode reading is < 128. At the same time, both hardware pins MagINCn (#1) and MagDECn (#2) will be pulled to VSS. A properly aligned magnet will therefore produce a MagINCn = MagDECn = 1 signal throughout a full 360° turn of the magnet.

Stronger magnets or short gaps between magnet and IC may show values larger than 128. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum.

The alignment mode can be reset to normal operation by a power-on-reset (disconnect / re-connect power supply) or by a falling edge on CSn with Prog = low.

Figure 27:
Enabling the Alignment Mode

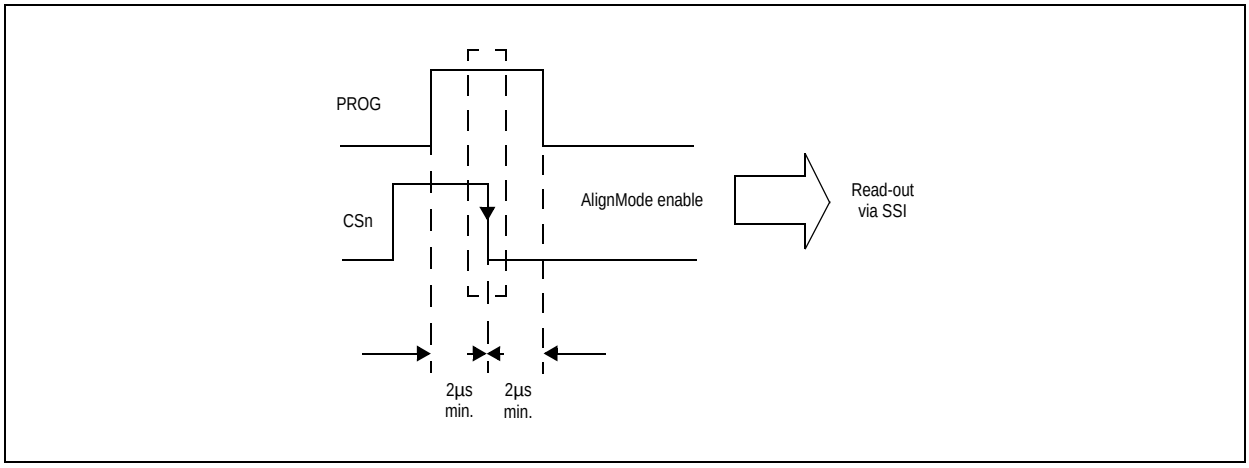
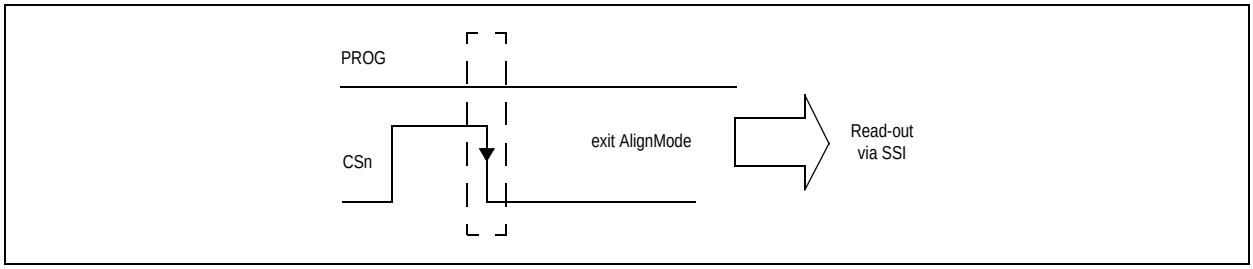


Figure 28:
Exiting the Alignment Mode



3.3V / 5V Operation

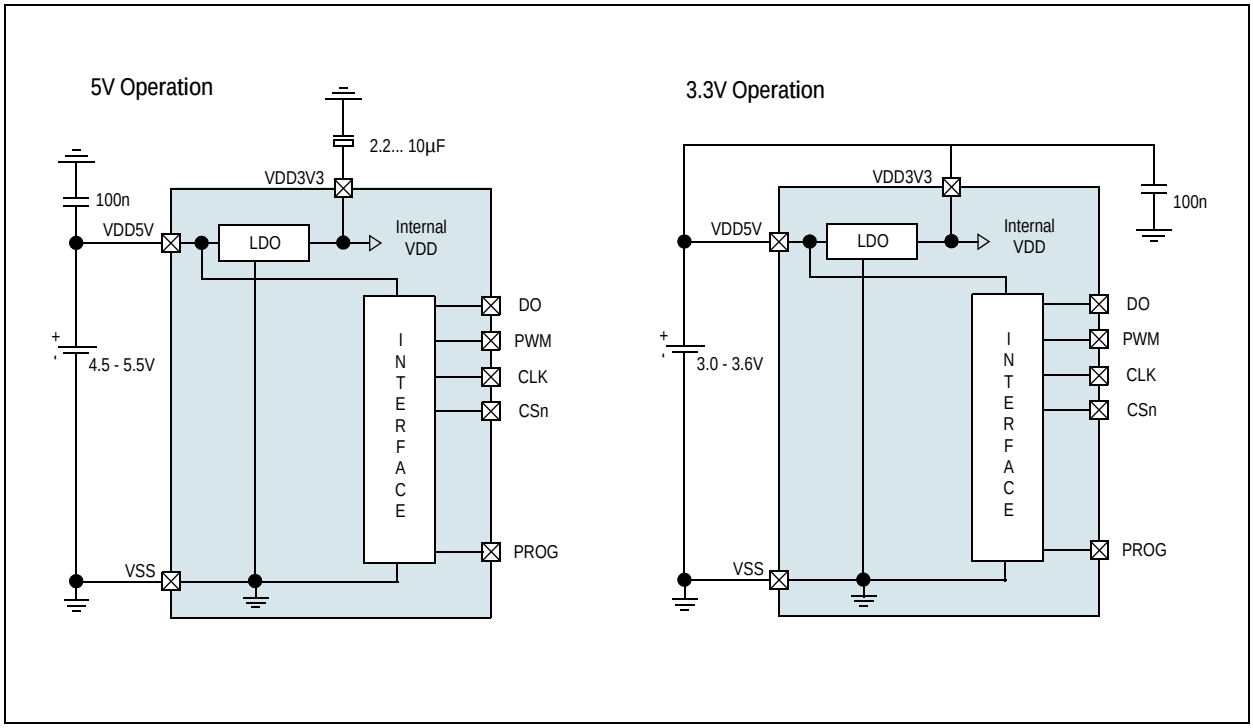
The AS5045 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The internal supply voltage is always taken from the output of the LDO, meaning that the internal blocks are always operating at 3.3V.

For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 29).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 2.2...10µF capacitor, which is supposed to be placed close to the supply pin (see Figure 29).

The VDD3V3 output is intended for internal use only It must not be loaded with an external load (see Figure 29).

Figure 29:
Connections for 5V / 3.3V Supply Voltages



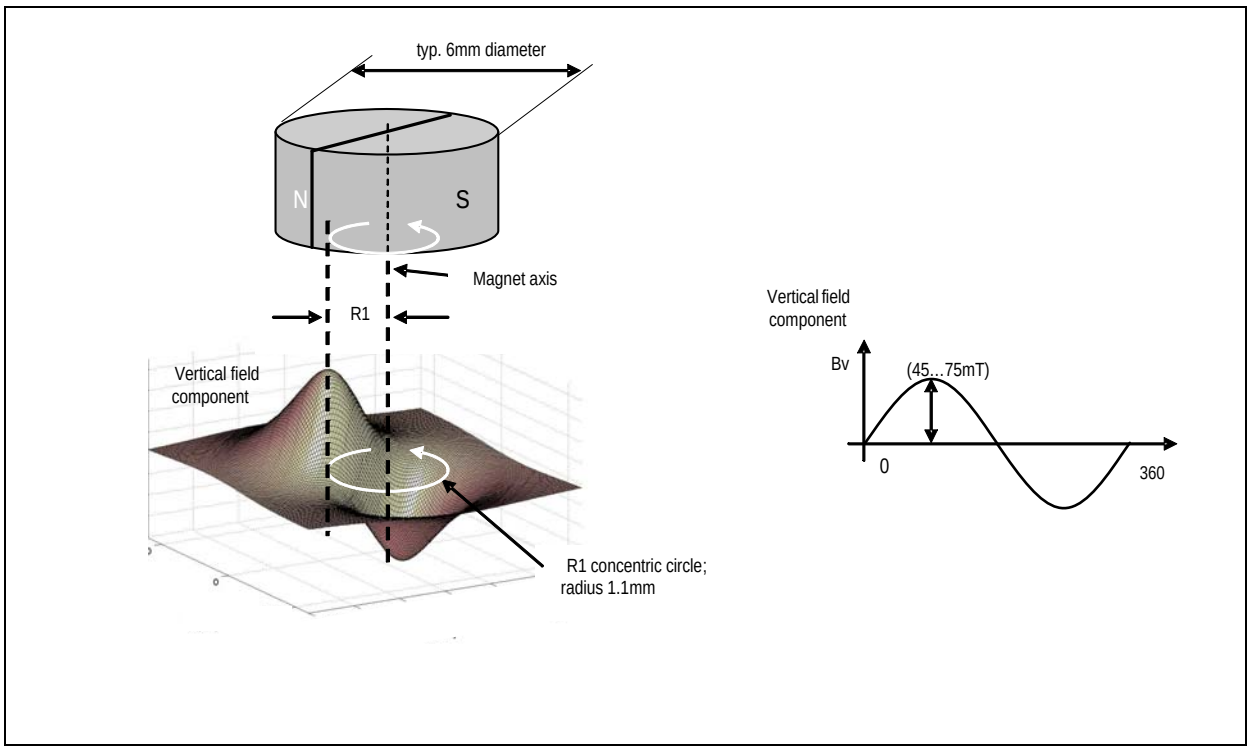
A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage which may lead to larger than normal jitter of the measured angle.

Choosing the Proper Magnet

Typically the magnet should be 6mm in diameter and ≥2.5mm in height. Magnetic materials such as rare earth AlNiCo/SmCo5 or NdFeB are recommended. The magnetic field strength perpendicular to the die surface has to be in the range of ±45mT to ±75mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic field B_V at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT to ±75mT (see Figure 30).

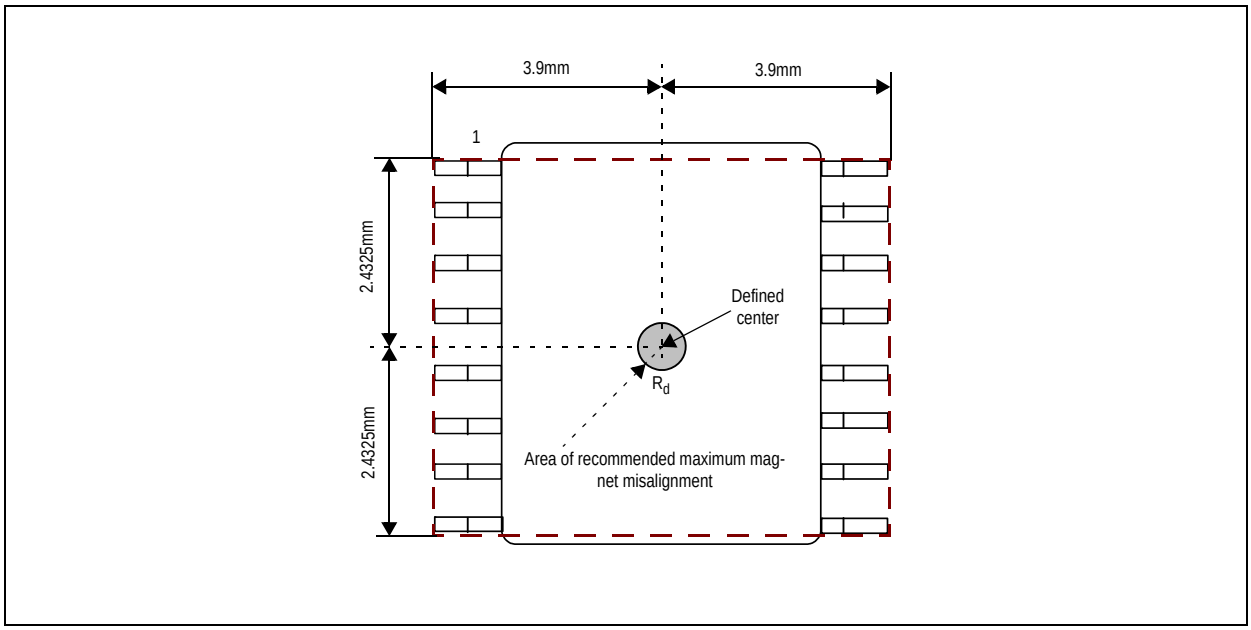
Figure 30:
Typical Magnet (6x3mm) and Magnetic Field Distribution



Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below.

Figure 31:
Defined Chip Center and Magnet Displacement Radius



Magnet Placement. The magnet's center axis should be aligned within a displacement radius Rd of 0.25mm from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 30). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagINCn (pin 1) and MagDECn (pin 2), see Figure 4.

Failure Diagnostics

The AS5045 also offers several diagnostic and failure detection features:

Magnetic Field Strength Diagnosis

By Software: The MagINC and MagDEC status bits will both be high when the magnetic field is out of range.

By Hardware: Pins #1 (MagINCn) and #2 (MagDECn) are open-drain outputs and will both be turned on (= low with external pull-up resistor) when the magnetic field is out of range. If only one of the outputs are low, the magnet is either moving towards the chip (MagINCn) or away from the chip (MagDECn).

Power Supply Failure Detection

By Software: If the power supply to the AS5045 is interrupted, the digital data read by the SSI will be all "0"s. Data is only valid, when bit OCF is high, hence a data stream with all "0"s is invalid. To ensure adequate low levels in the failure case, a pull-down resistor (~10kΩ) should be added between pin DO and VSS at the receiving side.

By Hardware: The MagINCn and MagDECn pins are open drain outputs and require external pull-up resistors. In normal operation, these pins are high ohmic and the outputs are high (see Figure 15). In a failure case, either when the magnetic field is out of range of the power supply is missing, these outputs will become low. To ensure adequate low levels in case of a broken power supply to the AS5045, the pull-up resistors (~10kΩ) from each pin must be connected to the positive supply at pin 16 (VDD5V).

By Hardware, PWM Output: The PWM output is a constant stream of pulses with 1kHz repetition frequency. In case of power loss, these pulses are missing.

Angular Output Tolerances

Accuracy

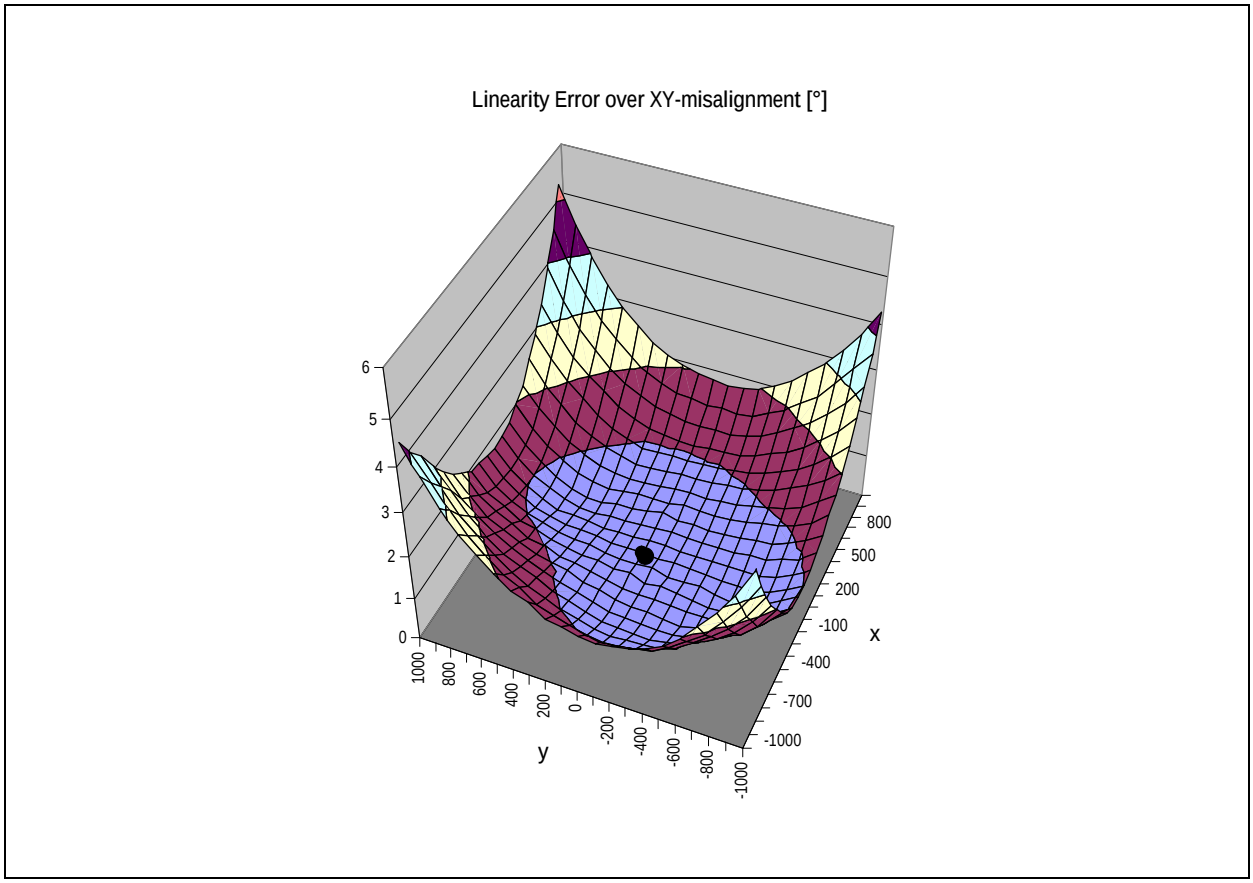
Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

- The non-linearity of the analog-digital converters
- Internal gain and mismatch errors
- Non-linearity due to misalignment of the magnet

As a sum of all these errors, the accuracy with centered magnet = $(Err_{max} - Err_{min})/2$ is specified as better than ±0.5 degrees @ 25°C (see Figure 33) Misalignment of the magnet further reduces the accuracy. Figure 32 shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ±1mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm.

For each misalignment step, the measurement as shown in Figure 33 is repeated and the accuracy (Errmax – Errmin)/2 (e.g. 0.25°) is entered as the Z-axis in the 3D-graph.

Figure 32:
Example of Linearity Error over XY Misalignment

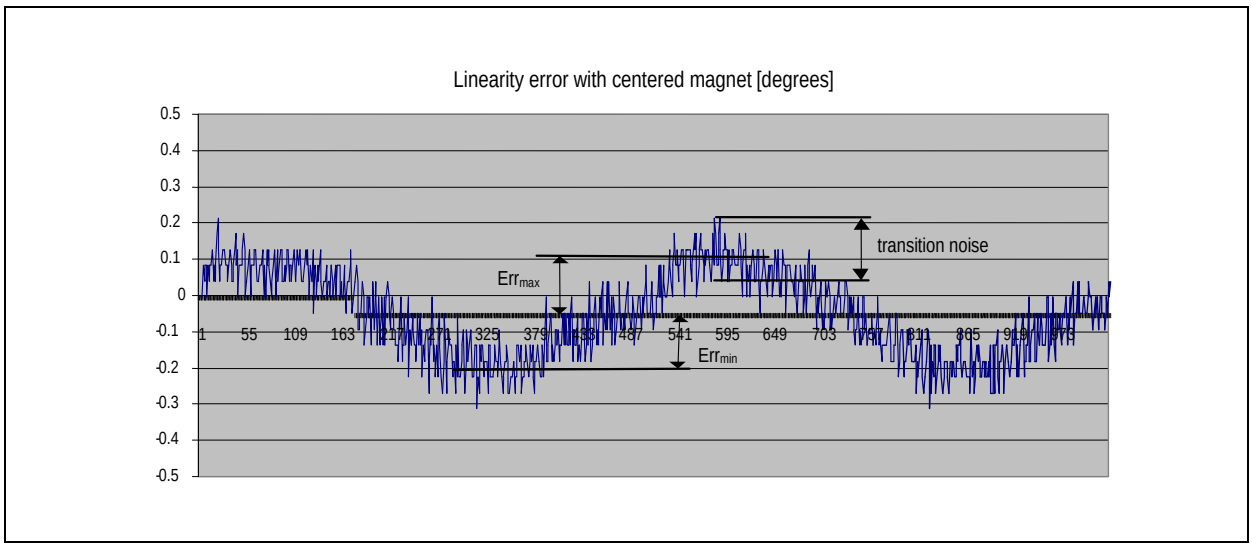


The maximum non-linearity error on this example is better than ±1 degree (inner circle) over a misalignment radius of ~0.7mm. For volume production, the placement tolerance of the IC within the package (±0.235mm) must also be taken into account.

The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ±1.4 degrees.

The magnet used for this measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

Figure 33:
Example of Linearity Error over 360°



Transition Noise

Transition noise is defined as the jitter in the transition between two steps. Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved. This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.06 degrees rms (1 sigma)[1] in fast mode (pin MODE = high) and 0.03 degrees rms (1 sigma) in slow mode (pin MODE = low or open). This is the repeatability of an indicated angle at a given mechanical position.

1. Statistically, 1 sigma represents 68.27% of readings, 3 sigma represents 99.73% of readings.

The transition noise has different implications on the type of output that is used:

- **Absolute Output; SSI Interface:** The transition noise of the absolute output can be reduced by the user by implementing averaging of readings. An averaging of 4 readings will reduce the transition noise by 6dB or 50%, e.g. from 0.03°rms to 0.015°rms (1 sigma) in slow mode.
- **PWM Interface:** If the PWM interface is used as an analog output by adding a low pass filter, the transition noise can be reduced by lowering the cutoff frequency of the filter. If the PWM interface is used as a digital interface with a counter at the receiving side, the transition noise may again be reduced by averaging of readings.

High Speed Operation

Sampling Rate: The AS5045 samples the angular value at a rate of 2.61k (slow mode) or 10.42k (fast mode, selectable by pin MODE) samples per second. Consequently, the absolute outputs are updated each 384µs (96µs in fast mode). At a stationary position of the magnet, the sampling rate creates no additional error.

Absolute Mode: At a sampling rate of 2.6kHz/10.4kHz, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by

(EQ3) $$n_{slowmode} = \frac{60}{rpm \cdot 384\mu s}$$

(EQ4) $$n_{fastmode} = \frac{60}{rpm \cdot 96\mu s}$$

The upper speed limit in slow mode is ~6.000rpm and ~30.000rpm in fast mode. The only restriction at high speed is that there will be fewer samples per revolution as the speed increases.

Regardless of the rotational speed, the absolute angular value is always sampled at the highest resolution of 12 bit.

Propagation Delays

The propagation delay is the delay between the time that the sample is taken until it is converted and available as angular data. This delay is 96µs in fast mode and 384µs in slow mode. Using the SSI interface for absolute data transmission, an additional delay must be considered, caused by the asynchronous sampling (0 … $1/f_{sample}$) and the time it takes the external control unit to read and process the angular data from the chip (maximum clock rate = 1MHz, number of bits per reading = 18).

Angular Error Caused by Propagation Delay: A rotating magnet will cause an angular error caused by the output propagation delay.
This error increases linearly with speed:

(EQ5)

$$e_{sampling,} = rpm * 6 * prop.delay$$

Where:

$e_{sampling}$ = angular error [°]
rpm = rotating speed [rpm]
prop.delay = propagation delay [seconds]

Note(s): Since the propagation delay is known, it can be automatically compensated by the control unit processing the data from the AS5045.

Internal Timing Tolerance

The AS5045 does not require an external ceramic resonator or quartz. All internal clock timings for the AS5045 are generated by an on-chip RC oscillator. This oscillator is factory trimmed to ±5% accuracy at room temperature (±10% over full temperature range). This tolerance influences the ADC sampling rate and the pulse width of the PWM output.

- **Absolute Output; SSI Interface:** A new angular value is updated every 96µs (typ.) in fast mode and every 384µs (typ.) in slow mode.
- **PWM Output:** A new angular value is updated every 400µs (typ.). The PWM pulse timings T_{on} and T_{off} also have the same tolerance as the internal oscillator. If only the PWM pulse width T_{on} is used to measure the angle, the resulting value also has this timing tolerance. However, this tolerance can be cancelled by measuring both T_{on} and T_{off} and calculating the angle from the duty cycle.

(EQ6)

$$Position = \frac{t_{on} \cdot 4097}{(t_{on} + t_{off})} - 1$$

Temperature

Magnetic Temperature Coefficient: One of the major benefits of the AS5045 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5045 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5045 operates with magnetic field strengths from ±45…±75mT.

Example:

An NdFeB magnet has a field strength of 75mT @ -40°C and a temperature coefficient of -0.12% per Kelvin. The temperature change is from -40° to 125° = 165K. The magnetic field change is: 165 x -0.12% = -19.8%, which corresponds to 75mT at -40°C and 60mT at 125°C.

The AS5045 can compensate for this temperature related field strength change automatically, no user adjustment is required.

Accuracy over Temperature:

The influence of temperature in the absolute accuracy is very low. While the accuracy is ≤ ±0.5° at room temperature, it may increase to ≤±0.9° due to increasing noise at high temperatures.

Timing Tolerance over Temperature: The internal RC oscillator is factory trimmed to ±5%. Over temperature, this tolerance may increase to ±10%. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation. The only concern to the user is the width of the PWM output pulse, which relates directly to the timing tolerance of the internal oscillator. This influence however can be cancelled by measuring the complete PWM duty cycle instead of just the PWM pulse.

Differences Between AS5045 and AS5040

All parameters are similar for AS5045 and AS5040, except for the parameters given below:

Figure 34:
Differences Between AS5045 and AS5040

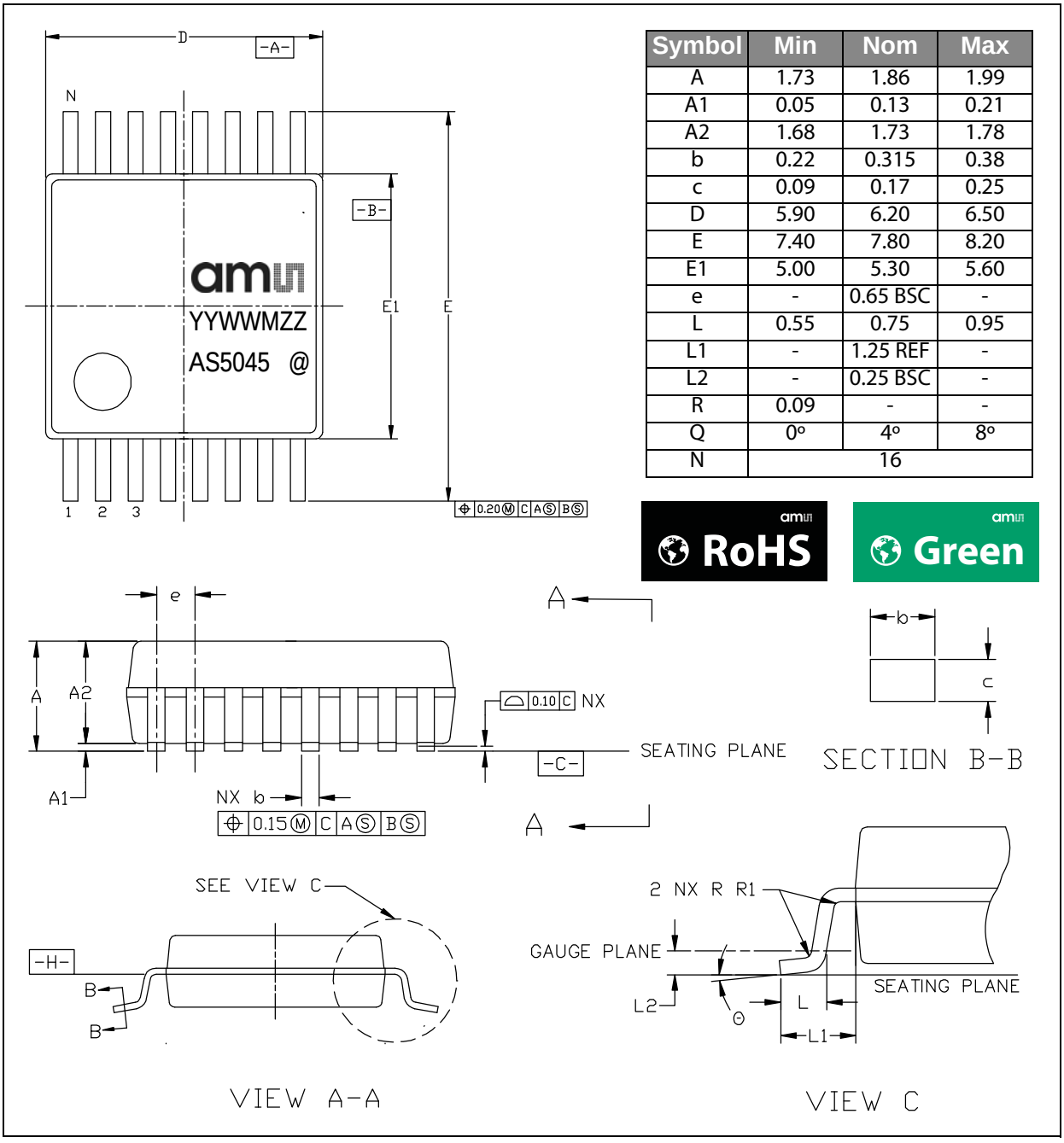
Building Block	AS5045	AS5040
Resolution	12bits, 0.088°/step	10bit, 0.35°/step
Data length	Read: 18bits (12bits data + 6 bits status) OTP write: 18 bits (12bits zero position + 6 bits mode selection)	Read: 16bits (10bits data + 6 bits status) OTP write: 16 bits (10bits zero position + 6 bits mode selection)
Incremental signals	Not used Pin 3: not used Pin 4: not used	Quadrature, step/direction and BLDC motor commutation modes Pin 3: incremental output A_LSB_U Pin 4: incremental output B_DIR_V
Pins 1 and 2	MagINCn, MagDECn: same feature as AS5040, additional OTP option for red-yellow-green magnetic range	MagINCn, MagDECn indicate in-range or out-of-range magnetic field plus movement of magnet in z-axis
Pin 6	MODE pin, switch between fast and slow mode	Pin 6: Index output

Building Block	AS5045	AS5040
Pin 12	PWM output: frequency selectable by OTP: 1µs / step, 4096 steps per revolution, f=244Hz 2µs/ step, 4096 steps per revolution, f=122Hz	PWM output: 1µs / step, 1024 steps per revolution, 976Hz PWM frequency
Sampling frequency	Selectable by MODE input pin: 2.5kHz, 10kHz	Fixed at 10kHz @10bit resolution
Propagation delay	384µs (slow mode) 96µs (fast mode)	48µs
Transition noise (rms; 1sigma)	0.03 degrees max. (slow mode) 0.06 degrees max. (fast mode)	0.12 degrees
OTP programming options	Zero position, rotational direction, PWM disable, 2 Magnetic Field indicator modes, 2 PWM frequencies	Zero position, rotational direction, incremental modes, index bit width.

Package Drawings & Markings

The device is available in 16-pin SSOP.

Figure 35:
Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.315	0.38
c	0.09	0.17	0.25
D	5.90	6.20	6.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
Q	0°	4°	8°
N		16	

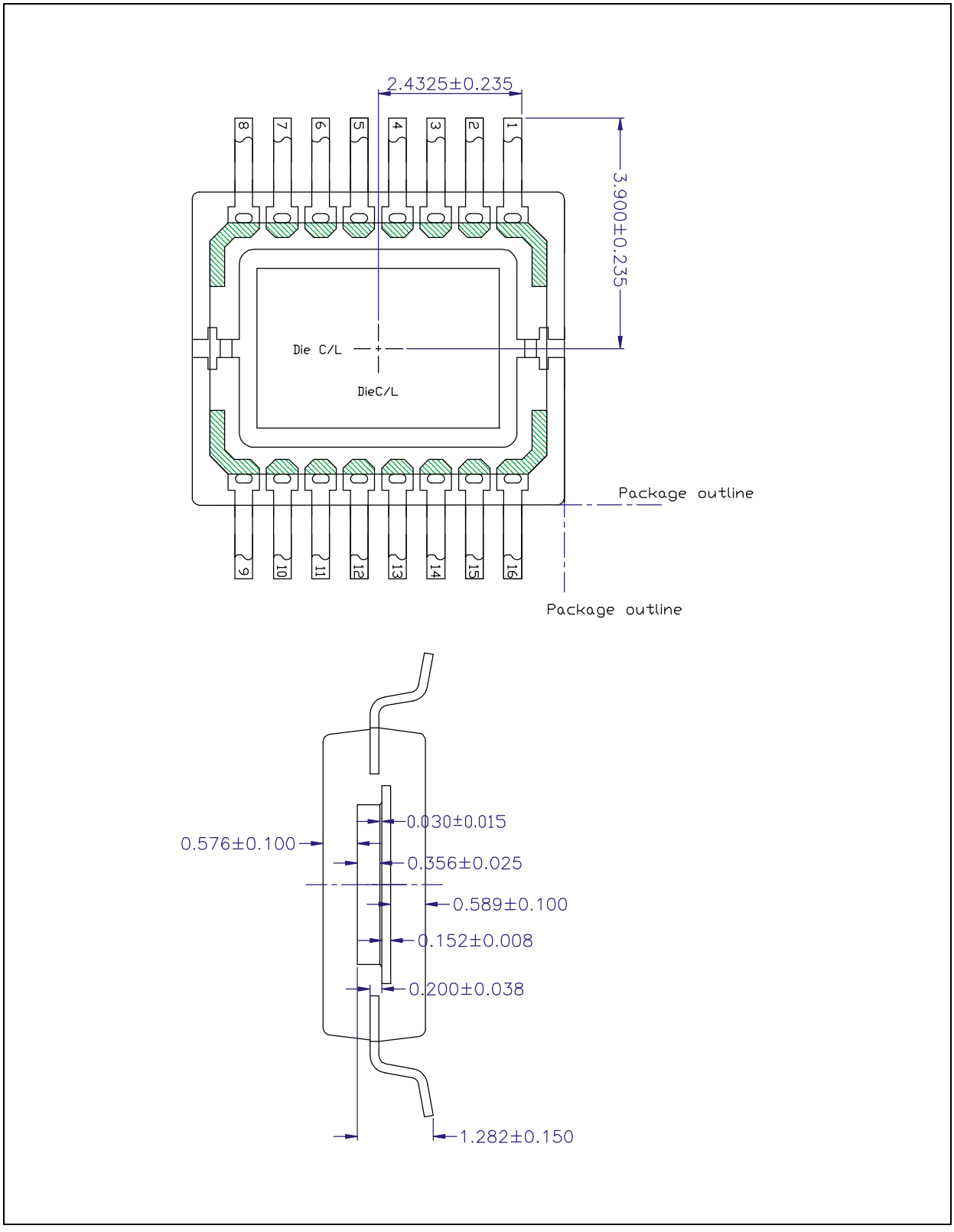
Note(s):

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.

Figure 36:
Marking: YYWWMZZ

YY	WW	M	ZZ	@
Year	Manufacturing week	Plant identifier	Assembly traceability code	Sublot identifier

Figure 37:
Vertical Cross Section of SSOP-16

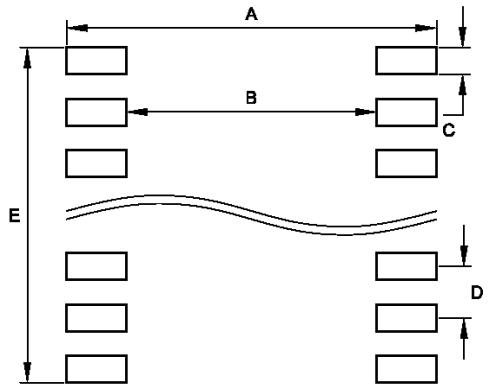


Note(s):

1. All dimensions in mm.

Recommended PCB Footprint

Figure 38:
PCB Footprint



Recommended Footprint Data		
Symbol	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

Ordering & Contact Information

The devices are available as the standard products shown in Figure 39.

Figure 39:
Ordering Information

Ordering Code	Description	Package	Delivery Form	Delivery Quantity
AS5045-ASSM	12-Bit Programmable Magnetic Position Sensor	16-pin SSOP	Tape & Reel	500 pcs/reel
AS5045-ASST		16-pin SSOP	Tape & Reel	2000 pcs/reel

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Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1.8 (2013-Aug-14) to current revision 2-01 (2017-Jul-13)	Page
1.8 (2013-Aug-14) to 2-00 (2016-Sep-12)	
Content was updated to the latest **ams** design	
Added Figure 1	1
Updated Figure 39	41
2-00 (2016-Sep-12) to 2-01 (2017-Jul-13)	
Updated Figure 39	41

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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