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## 1 Overview

IRMCF588 is a new generation International Rectifier integrated circuit device primarily designed as a one-chip solution for complete two motor inverterized appliance motor control applications. Particular application includes a full DC inverter Air Conditioner which requires two motor sensorless control plus power factor control. Unlike a traditional microcontroller or DSP, the IRMCF588 provides a built-in two parallel running computation engines for two closed loop sensorless control algorithm using the unique Flexible Motion Control Engine (MCE™). The MCE™ consists of a collection of control elements, motion peripherals, a dedicated motion control sequencer and dual port RAM to map internal signal nodes. IRMCF588 also employs a unique single shunt current reconstruction circuit to eliminate additional analog/digital circuitry and enables a direct shunt resistor interface to the IC, while still supporting leg shunt current sensing. Motion control programming is achieved using a dedicated graphical compiler integrated into the MATLAB/Simulink™ development environment. Sequencing, user interface, host communication, and upper layer control tasks can be implemented in the 8051 high-speed 8-bit microcontroller. The 8051 microcontroller is equipped with a JTAG port to facilitate emulation and debugging. Figure 1 shows a typical application schematic using the IRMCF588 in leg shunt mode.

IRMCF588 contains 64K bytes of Flash program memory plus 16K bytes of OTP memory and comes in a 100-pin QFP package.

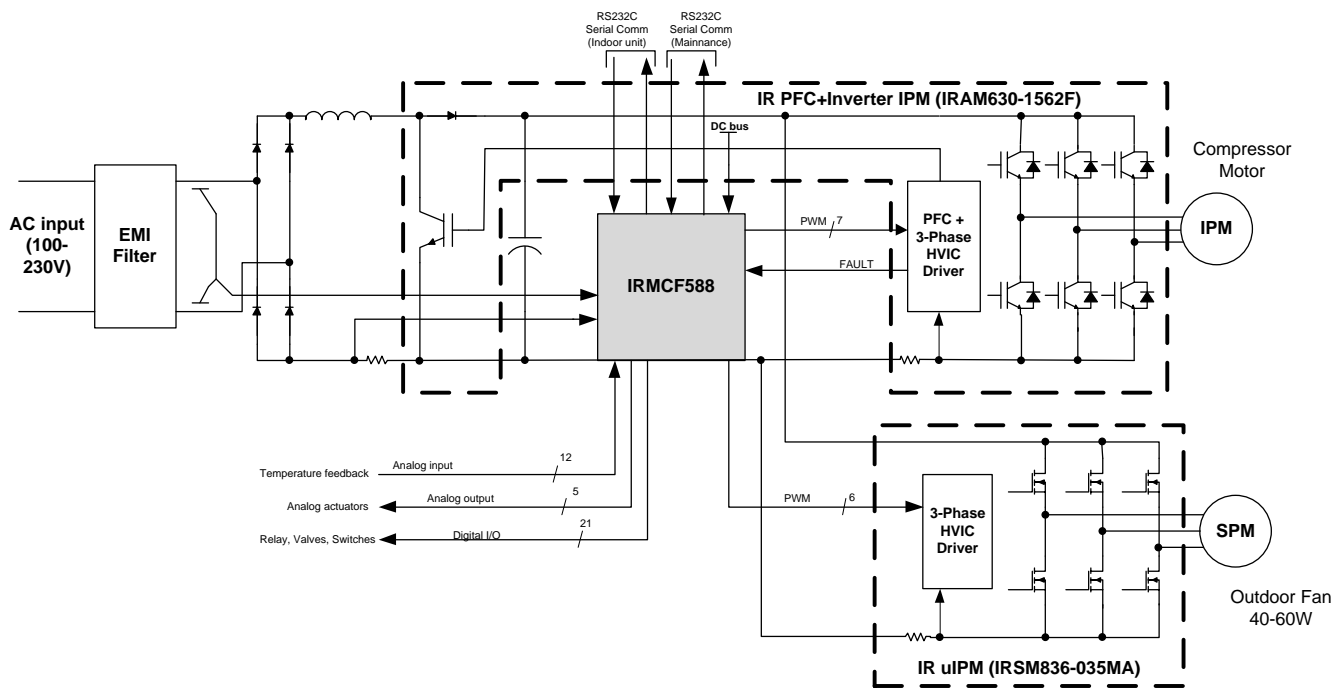
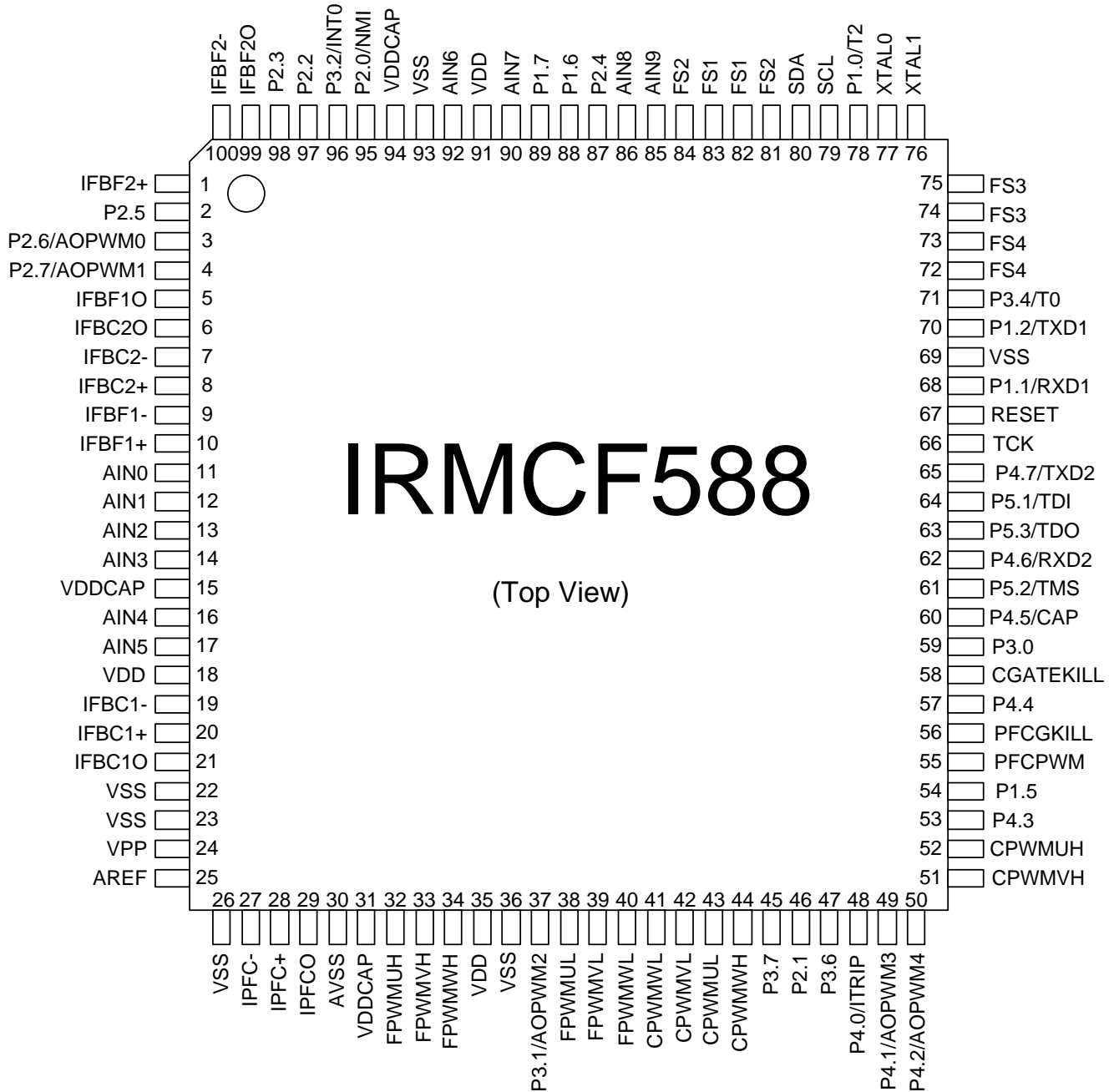
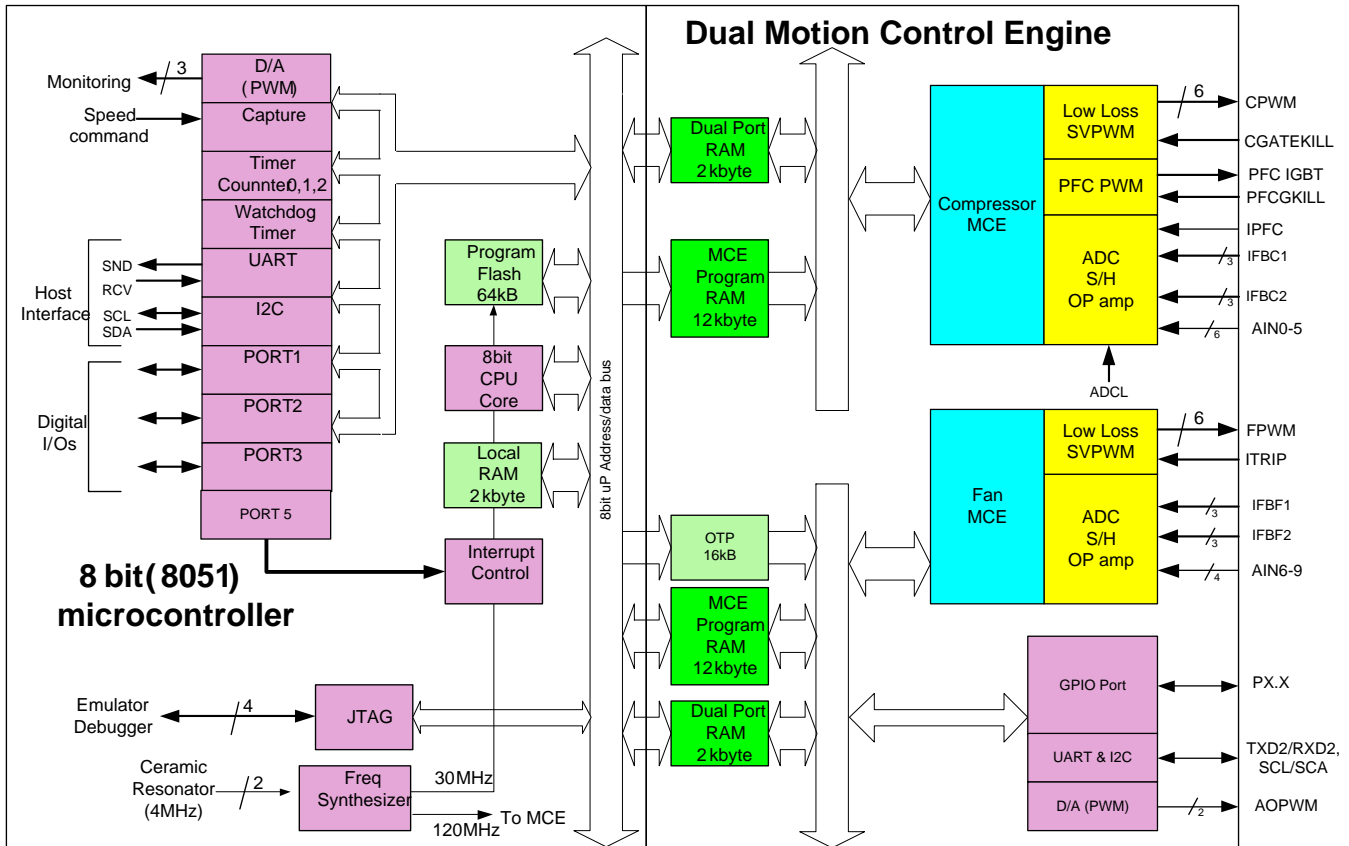


Figure 1. Typical Application Block Diagram Using IRMCF588

**2 Pinout**

**Figure 2. Pinout of IRMCF588**

### 3 IRMCF588 Block Diagram and Main Functions

IRMCF588 block diagram for leg shunt mode is shown in Figure 3.



**Figure 3. IRMCF588 Block Diagram**

IRMCF588 contains the following functions for sensorless AC motor control applications:

#### Motion Control Engine (MCE™)

- Sensorless FOC (complete sensorless field oriented control)
- Proportional plus Integral block
- Low pass filter
- Differentiator and lag (high pass filter)
- Ramp
- Limit
- Angle estimate (sensorless control)
- Inverse Clark transformation
- Vector rotator
- Bit latch
- Peak detect
- Transition
- Multiply-divide (signed and unsigned)

#### 8051 microcontroller

- Two 16 bit timer/counters
- One 16 bit periodic timer
- One 16 bit watchdog timer
- One 16 bit capture timer
- Up to 31 discrete digital I/Os
- Ten-channel 12 bit A/D
  - Buffered (current sensing) three channels (0 – 1.2V input)
  - Unbuffered seven channels (0 – 1.2V input)
- JTAG port (4 pins)
- Up to five channels of analog output (8 bit PWM)
- UART

- |  |   |
|--|---|
| <ul style="list-style-type: none"> <li>• I<sup>2</sup>C port</li> <li>• Dual MCE™ control sequencer</li> <li>• Adder</li> <li>• MCE™ program memory (12 K byte X 2 )</li> <li>• Divide (signed and unsigned)</li> <li>• Subtractor</li> <li>• Comparator</li> <li>• Counter</li> <li>• Accumulator</li> <li>• Switch</li> <li>• Shift</li> <li>• ATAN (arc tangent)</li> <li>• Function block (any curve fitting, nonlinear function)</li> <li>• 16 bit wide Logic operations (AND, OR, XOR, NOT, NEGATE)</li> </ul> | <ul style="list-style-type: none"> <li>• 64K byte Flash memory</li> <li>• 2K byte data RAM</li> </ul> |
|--|---|

## 4 Application connection and Pin function

Figure 4 shows the application connections in single shunt mode. Figure 5 shows the analog front end diagram with a single shunt configuration.

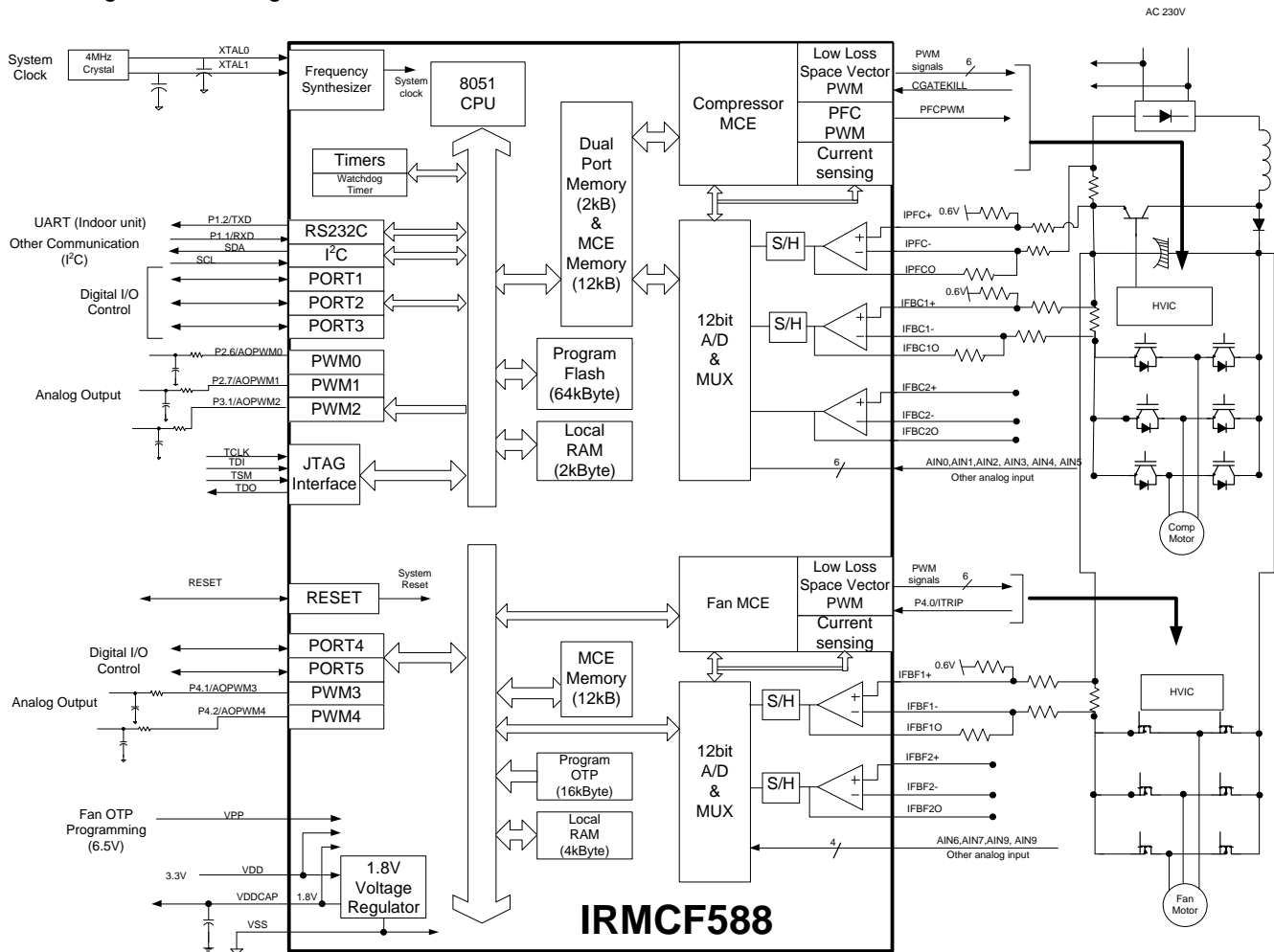
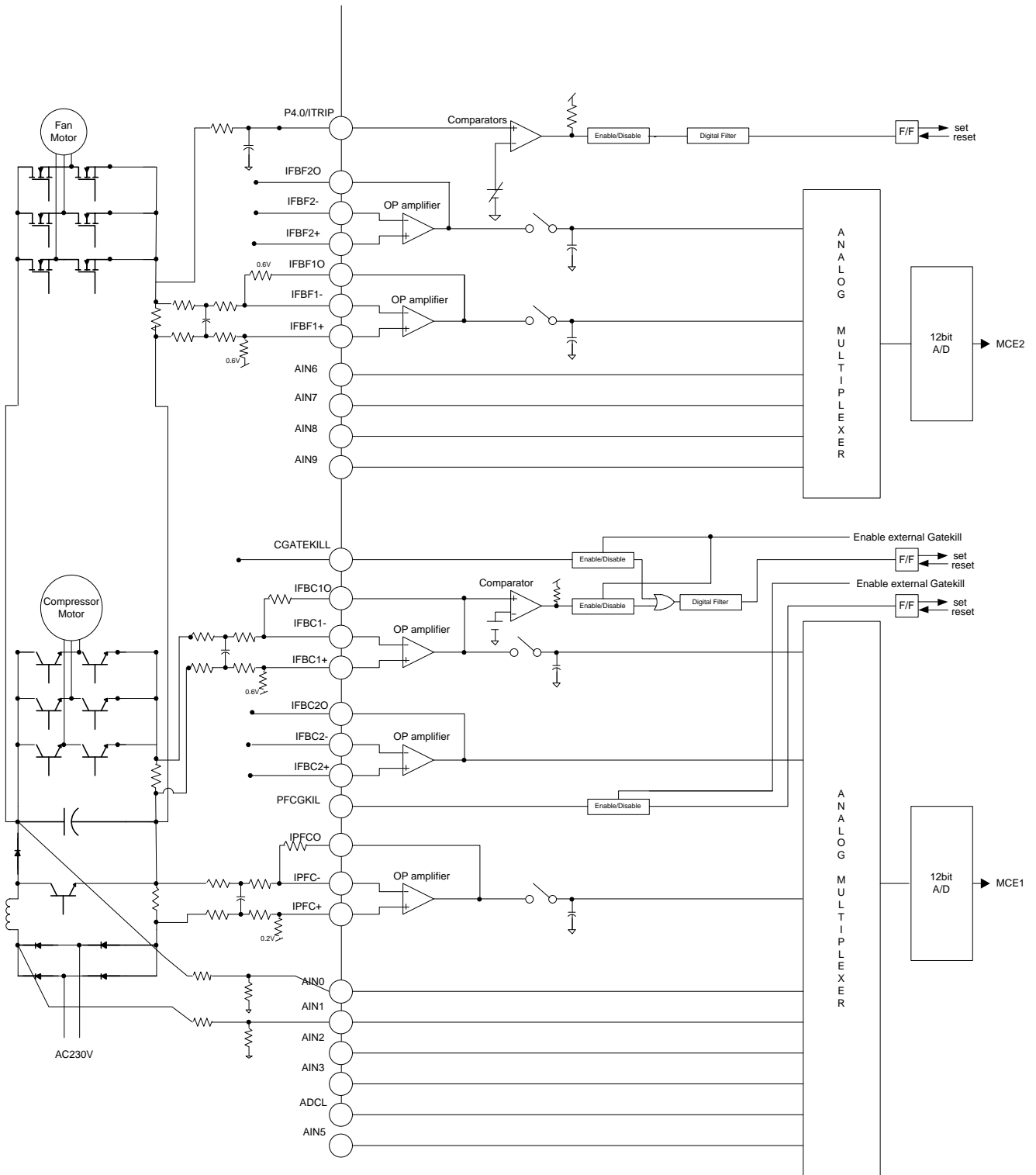


Figure 4. IRMCF588 Single Shunt Connection Diagram





**Figure 5. IRMCF588 Analog Front End Diagram**

## 4.1 8051 Peripheral Interface Group

### UART Interface

P1.2/TXD	Output, Channel 1 Transmit data from IRMCF588
P1.1/RXD	Input, Channel 1 Receive data to IRMCF588
P4.6/TXD2	Output, Channel 2 Transmit data from IRMCF588
P4.7/RXD2	Input, Channel 2 Receive data to IRMCF588

### Discrete I/O Interface

P1.0/T2	Input/output port 1.0, can be configured as Timer/Counter 2 input
P1.1/RXD	Input/output port 1.1, can be configured as RXD input
P1.2/TXD	Input/output port 1.2, can be configured as TXD output
P1.5	Input/output port 1.5
P1.6	Input/output port 1.6
P1.7	Input/output port 1.6
P2.0/NMI	Input/output port 2.0, can be configured as non-maskable interrupt input
P2.1	Input/output port 2.1
P2.2	Input/output port 2.2
P2.3	Input/output port 2.3
P2.4	Input/output port 2.4
P2.5	Input/output port 2.5
P2.6/AOPWM0	Input/output port 2.6, can be configured as AOPWM0 output
P2.7/AOPWM1	Input/output port 2.7, can be configured as AOPWM1 output
P3.0	Input/output port 3.0
P3.1/AOPWM2	Input/output port 3.1, can be configured as AOPWM2 output
P3.2/INT0	Input/output port 3.2, can be configured as INT0 input
P3.4/T0	Input/output port 3.4, can be configured as T0 input for counter mode
P3.6	Input/output port 3.6
P3.7	Input/output port 3.7
P4.0/ITRIP	Input/output port 4.0, can be configured as overcurrent trip input for Fan motor
P4.1/AOPWM3	Input/output port 4.1, can be configured as AOPWM3 analog output
P4.2/AOPWM4	Input/output port 4.2, can be configured as AOPWM4 analog output
P4.3	Input/output port 4.3
P4.4	Input/output port 4.4
P4.5/CAP	Input/output port 4.5, can be configured as Capture Timer input
P4.6/TXD2	Input/output port 4.6, can be configured as UART2 transmit
P4.7/RXD2	Input/output port 4.7, can be configured as UART2 receive
P5.1/TDI	Input port 5.1, configured as JTAG port by default
P5.2/TMS	Input port 5.2, configured as JTAG port by default
P5.3/TDO	Output port 5.3, configured as JTAG port by default

### Analog Output Interface

P2.6/AOPWM0	Input/output, can be configured as 8-bit PWM output 0 with programmable carrier frequency
P2.7/AOPWM1	Input/output, can be configured as 8-bit PWM output 1 with programmable carrier frequency
P3.1/AOPWM2	Input/output, can be configured as 8-bit PWM output 2 with programmable carrier frequency
P4.1/AOPWM3	Input/output, can be configured as 8-bit PWM output 3 with programmable carrier frequency
P4.2/AOPWM4	Input/output, can be configured as 8-bit PWM output with programmable carrier frequency

**Crystal Interface**

XTAL0	Input, connected to crystal
XTAL1	Output, connected to crystal

**Reset Interface**

RESET	Input and Output, system reset, doesn't require external RC time constant
-------	---

**I<sup>2</sup>C Interface**

SCL	Output, I <sup>2</sup> C clock output
SDA	Input/output, I <sup>2</sup> C Data line

**4.2 Motion Peripheral Interface Group**
**PWM**

CPWMUH	Output, Compressor motor PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMUL	Output, Compressor motor PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMVH	Output, Compressor motor PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMVL	Output, Compressor motor PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMWH	Output, Compressor motor PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
CPWMWL	Output, Compressor motor PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
PFCPWM	Output, Compressor motor PFCPWM output signal, internally pulled up by 70kΩ, configured low true at a power up
FPWMUH	Output, Fan motor PWM phase U high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMUL	Output, Fan motor PWM phase U low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMVH	Output, Fan motor PWM phase V high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMVL	Output, Fan motor PWM phase V low side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMWH	Output, Fan motor PWM phase W high side gate signal, internally pulled down by 58kΩ, configured high true at a power up
FPWMWL	Output, Fan motor PWM phase W low side gate signal, internally pulled down by 58kΩ, configured high true at a power up

**Fault**

CGATEKILL	Input, upon assertion this negates all six PWM signals, active low, internally pulled up by 70kΩ
PFCGKILL	Input, upon assertion, this negates PFCPWM signal, active low, internally pulled up by 70kΩ
P4.0/ITRIP	Input/output port 4.0, can be configured as overcurrent trip input for Fan motor according to the setting of active_pol register, pulled up by 49kΩ internal resistor

### 4.3 Analog Interface Group

AVSS	Analog power return, (analog internal 1.8V power is shared with VDDCAP)
AREF	0.6V buffered output
IFBC1+	Input, Operational amplifier positive input for compressor motor shunt sensing
IFBC1-	Input, Operational amplifier negative input for compressor motor shunt sensing
IFBC1O	Output, Operational amplifier output for compressor motor shunt sensing
IFBC2+	Input, Operational amplifier positive input for compressor motor leg shunt sensing
IFBC2-	Input, Operational amplifier negative input for compressor motor leg shunt sensing
IFBC2O	Output, Operational amplifier output for compressor motor leg shunt sensing
IPFC+	Input, Operational amplifier positive input for PFC current sensing
IPFC-	Input, Operational amplifier negative input for PFC current sensing
IPFCO	Output, Operational amplifier output for PFC current sensing
IFBF1+	Input, Operational amplifier positive input for Fan motor shunt sensing
IFBF1-	Input, Operational amplifier negative input for Fan motor shunt sensing
IFBF1O	Output, Operational amplifier output for Fan motor shunt sensing
IFBF2+	Input, Operational amplifier positive input for Fan motor leg shunt sensing
IFBF2-	Input, Operational amplifier negative input for Fan motor leg shunt sensing
IFBF2O	Output, Operational amplifier output for Fan motor leg shunt sensing
AIN0	Input, DC voltage sensing or Analog input channel 0 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN1	Input, AC Input voltage sensing or Analog input channel 1 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN2	Input, Analog input channel 2 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN3	Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN4	Input, Analog input channel 3 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN5	Input, Analog input channel 5 (0 – 1.2V), needs to be pulled down to AVSS if unused
AIN6	Input, Analog input channel 6 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused
AIN7	Input, Analog input channel 7 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused
AIN8	Input, Analog input channel 8 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused
AIN9	Input, Analog input channel 9 (0 – 1.2V), associated with Fan MCE, needs to be pulled down to AVSS if unused

Analog Channel	Leg Shunt Mode	Single Shunt Mode	Pin number(s)
IPFC	PFC Current	PFC Current	27,28,29
IFBC1	Motor U Phase Current	Motor Shunt Current	19,20,21
IFBC2	Motor V Phase Current	-	6,7,8
AIN1	AC Voltage	AC Voltage	12

**Table 1. Analog channel sensing functions in Leg and Single Shunt Modes**

#### 4.4 Power Interface Group

VDD	Digital power (3.3V)
VDDCAP	Internal 1.8V output, requires capacitors to the pin. Shared with analog power pad internally <b>Note:</b> The internal 1.8V supply is not designed to power any external circuits or devices. Only capacitors should be connected to this pin.
VSS	System common

#### 4.5 Test Interface Group

P5.2/TMS	JTAG test mode input or input digital port for compressor MCE
P5.3/TDO	JTAG data output port for compressor MCE
P5.1/TDI	JTAG data input, or input digital port for compressor MCE
TCK	JTAG test clock port for compressor MCE

#### 4.6 Factory use Group

FS1	Pin82 and Pin83 need to be connected and pulled up by 4.7K resistor for factory purpose
FS2	Pin81 and Pin84 need to be connected and pulled up by 4.7K resistor for factory purpose
FS3	Pin74 and Pin75 need to be connected and pulled up by 4.7K resistor for factory purpose
FS4	Pin73 and Pin72 need to be connected and pulled up by 4.7K resistor for factory purpose

## 5 DC Characteristics

### 5.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Condition
V <sub>DD</sub>	Supply Voltage	-0.3 V	-	3.6 V	Respect to VSS
V <sub>IA</sub>	Analog Input Voltage	-0.3 V	-	1.98 V	Respect to AVSS
V <sub>ID</sub>	Digital Input Voltage	-0.3 V	-	6.0 V	Respect to VSS
T <sub>A</sub>	Ambient Temperature	-40 °C	-	85 °C	
T <sub>S</sub>	Storage Temperature	-65 °C	-	150 °C	

**Table 2. Absolute Maximum Ratings**

**Caution:** Stresses beyond those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

### 5.2 System Clock Frequency and Power Consumption

C<sub>CAREF</sub> = 1nF, C<sub>CMEXT</sub> = 100nF. VDD=3.3V, Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
SYCLK	System Clock	32	-	120	MHz
P <sub>D</sub>	Power consumption		150 <sup>1</sup>	-	mW

**Table 3. System Clock Frequency**

Note

1) The value is based on the condition of MCE clock=100MHz, 8051 clock 20MHz with an actual motor and PFC running by a typical MCE application program and 8051 code.

### 5.3 Digital I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
$V_{DD1}$	Supply Voltage	3.0 V	3.3 V	3.6 V	Recommended
$V_{IL}$	Input Low Voltage	-0.3 V	-	0.8 V	Recommended
$V_{IH}$	Input High Voltage	2.0 V		3.6 V	Recommended
$C_{IN}$	Input capacitance	-	3.6 pF	-	<sup>(1)</sup>
$I_L$	Input leakage current		$\pm 10$ nA	$\pm 1$ $\mu$ A	$V_O = 3.3$ V or 0 V
$I_{OL1}^{(2)}$	Low level output current	8.9 mA	13.2 mA	15.2 mA	$V_{OL} = 0.4$ V <sup>(1)</sup>
$I_{OH1}^{(2)}$	High level output current	12.4 mA	24.8 mA	38 mA	$V_{OH} = 2.4$ V <sup>(1)</sup>
$I_{OL2}^{(3)}$	Low level output current	17.9 mA	26.3 mA	33.4 mA	$V_{OL} = 0.4$ V <sup>(1)</sup>
$I_{OH2}^{(3)}$	High level output current	24.6 mA	49.5 mA	81 mA	$V_{OH} = 2.4$ V <sup>(1)</sup>

**Table 4. Digital I/O DC Characteristics**

Note:

- (1) Data guaranteed by design.
- (2) Applied to SCL, SDA pins.
- (3) Applied to all digital I/O pins except SCL and SDA pins.

### 5.4 Analog I/O DC Characteristics

- OP amps for compressor, fan and PFC current sensing

$C_{AREF} = 1nF$ .  $V_{DD}=3.3V$ , Unless specified,  $T_a = 25^{\circ}C$ .

Symbol	Parameter	Min	Typ	Max	Condition
$V_{OFFSET}$	Input Offset Voltage	-	-	26 mV	$V_{AVDD} = 1.8 V$
$V_I$	Input Voltage Range	0 V		1.2 V	Recommended
$V_{OUTSW}$	OP amp output operating range	50 mV <sup>(1)</sup>	-	1.2 V	$V_{AVDD} = 1.8 V$
$C_{IN}$	Input capacitance	-	3.6 pF	-	(1)
$R_{FDBK}$	OP amp feedback resistor	5 k $\Omega$	-	20 k $\Omega$	Requested between IFBO and IFB-
OP $GAIN_{CL}$	Operating Close loop Gain	80 db	-	-	(1)
CMRR	Common Mode Rejection Ratio	-	80 db	-	(1)
$I_{SRC}$	Op amp output source current	-	1 mA	-	$V_{OUT} = 0.6 V$ (1)
$I_{SNK}$	Op amp output sink current	-	100 $\mu A$	-	$V_{OUT} = 0.6 V$ (1)
$V_{min}$	Min Voltage for Ain 0 -9	60 mV	NA	NA	(1)

**Table 5. Analog I/O DC Characteristics**

Note:

(1) Data guaranteed by design.

### 5.5 A/D Accuracy

Unless specified,  $T_a = 25^{\circ}C$ .

A/D accuracy for current sensing (IFBC1+,IFBC1-,IFBC1O, IFBC2+,IFBC2-,IFBC2O, IFBF1+,IFBF1-,IFBF1O, IFBF2+,IFBF2-,IFBF2O,IPFC+,IPFC-,IPFCO), and analog input channels (AIN0-AIN9)

Symbol	Parameter	Min	Typ	Max	Condition
$ADC_{error}$	Error is the difference between ideal counts and compensated counts for any applied voltage in 0-1.2V range	-	$\pm 10$ Counts	-	(1)

**Table 5. A/D Accuracy**

Note:

(1) Characterized not tested at manufacturing.

### 5.5 Under Voltage Lockout DC characteristics

Unless specified,  $T_a = 25^{\circ}C$ .

Symbol	Parameter	Min	Typ	Max	Condition
$UV_{CC+}$	UVcc positive going Threshold	2.78 V	3.04 V	3.23 V	(1)
$UV_{CC-}$	UVcc negative going Threshold	2.78 V	2.97 V	3.23 V	



UV <sub>CC</sub> H	UV <sub>CC</sub> Hysteresys	-	73 mV	-	(1)
--------------------	-----------------------------	---	-------	---	-----

**Table 6. UV<sub>CC</sub> DC Characteristics**

Note:

(1) Data guaranteed by design.

## 5.6 Itrip comparator DC characteristics

Unless specified, V<sub>DD</sub>=3.3V, T<sub>a</sub> = 25°C.

Symbol	Parameter	Min	Typ	Max	Condition
Itrip <sub>+</sub>	Itrip positive going Threshold	-	1.22V	-	V <sub>DD</sub> = 3.3 V
Itrip <sub>-</sub>	Itrip negative going Threshold	-	1.10V	-	V <sub>DD</sub> = 3.3 V
ItripH	Itrip Hysteresys	-	120mV	-	

**Table 7. Itrip DC Characteristics**

## 5.7 AREF Characteristics

C<sub>AREF</sub> = 1nF. Unless specified, T<sub>a</sub> = 25°C.

Symbol	Parameter	Min	Typ	Max	Condition
V <sub>AREF</sub>	Buffer Output Voltage	-	600 mV	-	V <sub>VDD</sub> = 3.3 V
ΔV <sub>o</sub>	Load regulation (V <sub>DC</sub> -0.6)	-	1 mV	-	(1)
PSRR	Power Supply Rejection Ratio	-	75 db	-	(1)

**Table 8. CMEXT and AREF DC Characteristics**

Note:

(1) Data guaranteed by design.

## 6 AC Characteristics

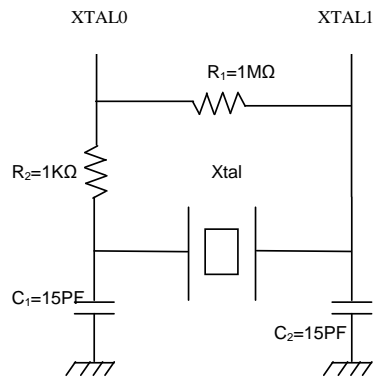
### 6.1 Digital PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Condition
F <sub>CLKIN</sub>	Crystal input frequency	3.2 MHz	4 MHz	60 MHz	<sup>(1)</sup> (see figure below)
F <sub>PLL</sub>	Internal clock frequency	32 MHz	50 MHz	128 MHz	<sup>(1)</sup>
F <sub>LWPPW</sub>	Sleep mode output frequency	F <sub>CLKIN</sub> ÷ 256	-	-	<sup>(1)</sup>
J <sub>S</sub>	Short time jitter	-	200 psec	-	<sup>(1)</sup>
D	Duty cycle	-	50 %	-	<sup>(1)</sup>
T <sub>LOCK</sub>	PLL lock time	-	-	500 μsec	<sup>(1)</sup>

**Table 9. PLL AC Characteristics**

Note:

(1) Data guaranteed by design.



**Figure 6. Crystal circuit example**

## 6.2 Analog to Digital Converter AC Characteristics

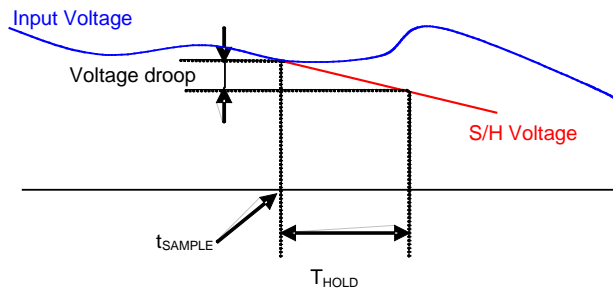
Unless specified,  $T_a = 25^\circ\text{C}$ .

Symbol	Parameter	Min	Typ	Max	Condition
$T_{\text{CONV}}$	Conversion time	-	-	2.05 $\mu\text{sec}$	(1)
$T_{\text{HOLD}}$	Sample/Hold maximum hold time	-	-	10 $\mu\text{sec}$	Voltage droop $\leq 15$ LSB (see figure below)

**Table 10 . A/D Converter AC Characteristics**

Note:

(1) Data guaranteed by design.



**Figure 7. Voltage droop and S/H hold time**

### 6.3 Op amp AC Characteristics

Unless specified,  $T_a = 25^\circ\text{C}$ .

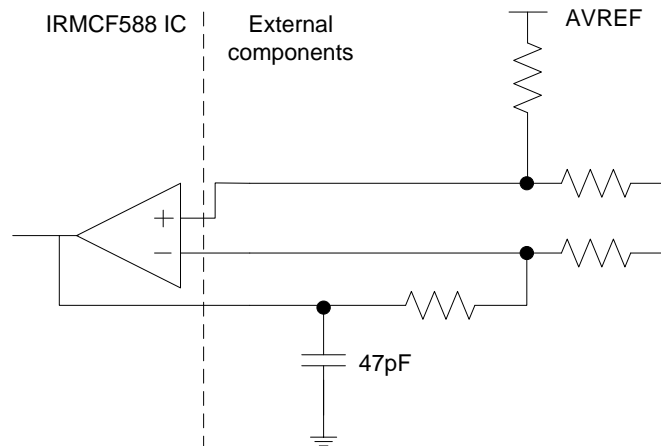
Symbol	Parameter	Min	Typ	Max	Condition
$OP_{SR}$	OP amp slew rate	-	10 V/ $\mu\text{sec}$	-	$V_{DD} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup>
$OP_{IMP}$	OP input impedance	-	$10^8\ \Omega$	-	<sup>(1)</sup> <sup>(2)</sup>
$T_{SET}$	Settling time	-	400 ns	-	$V_{DD} = 3.3\text{ V}$ , $CL = 33\text{ pF}$ <sup>(1)</sup>

**Table 11 Current Sensing OP Amp AC Characteristics**

Note:

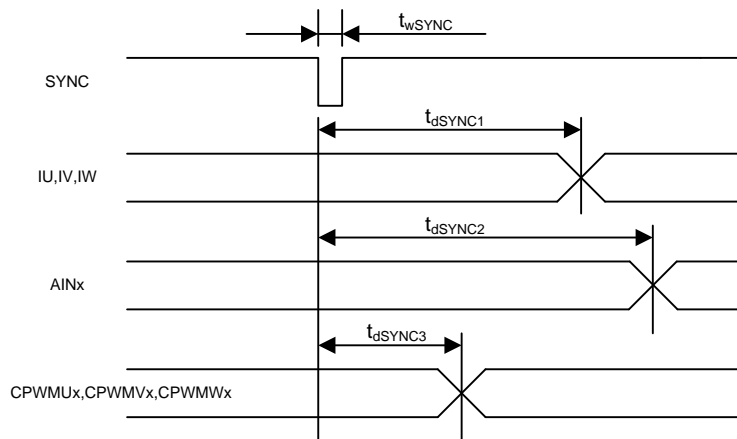
(1) Data guaranteed by design.

(2) To guarantee stability of the operational amplifier, it is recommended to load the output pin by a capacitor of 47pF, see Figure 8. Here typical OP amp connection is shown but all op amp outputs should be loaded with this capacitor value.



**Figure 8. Op amp output capacitor**

### 6.4 SYNC to SVPWM and A/D Conversion AC Timing



**Figure 9. SYNC timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

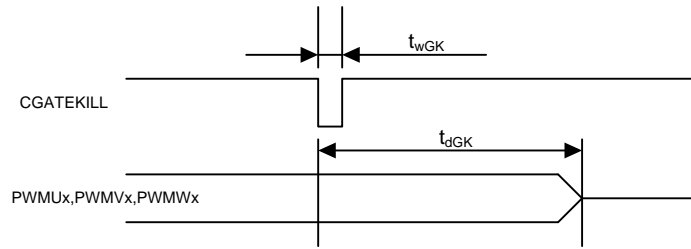
Symbol	Parameter	Min	Typ	Max	Unit
$t_{w\text{SYNC}}$	SYNC pulse width	-	32	-	SYSClk
$t_{d\text{SYNC}1}$	SYNC to current feedback conversion time	-	-	100	SYSClk
$t_{d\text{SYNC}2}$	SYNC to AIN0-9	-	-	200	SYSClk <sup>(1)</sup>
$t_{d\text{SYNC}3}$	SYNC to PWM output delay time	-	-	2	SYSClk

**Table 12. SYNC AC Characteristics**

Note:

(1) Only any 3 AINx from the compressor AIN channels (AIN0 -AIN6) and any 2 AINx (AIN7 - AIN9) from the fan AIN channels are converted once every SYNC events at the same time and the rest of the channels will be sampled once every 5 SYNC events.

### 6.5 GATEKILL to SVPWM AC Timing



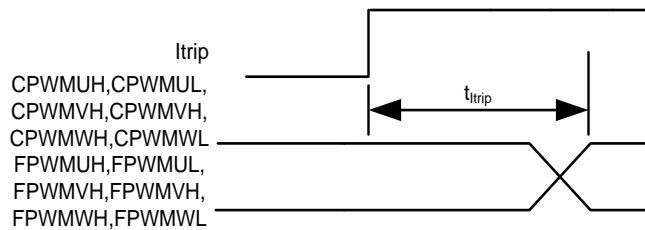
**Figure 10. Gatekill timing**

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{wGK}$	GATEKILL pulse width	32	-	-	SYCLK
$t_{dGK}$	GATEKILL to PWM output delay	-	-	100	SYCLK

**Table 13. GATEKILL to SVPWM AC Timing**

### 6.6 Internal Overcurrent trip AC Timing



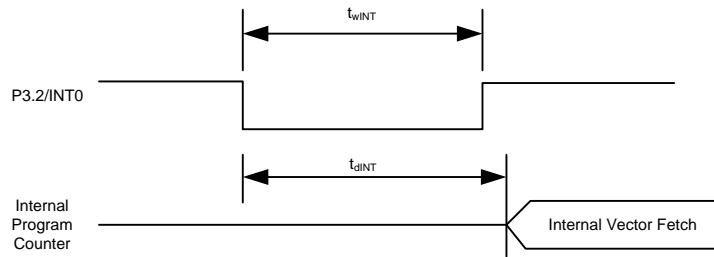
**Figure 11. ITRIP timing**

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{ITRIP}$	Itrip propagation delay	-	-	100(sysclk)+1.0usec	SYCLK+usec

**Table 14. Itrip AC Timing**

**6.7 Interrupt AC Timing**



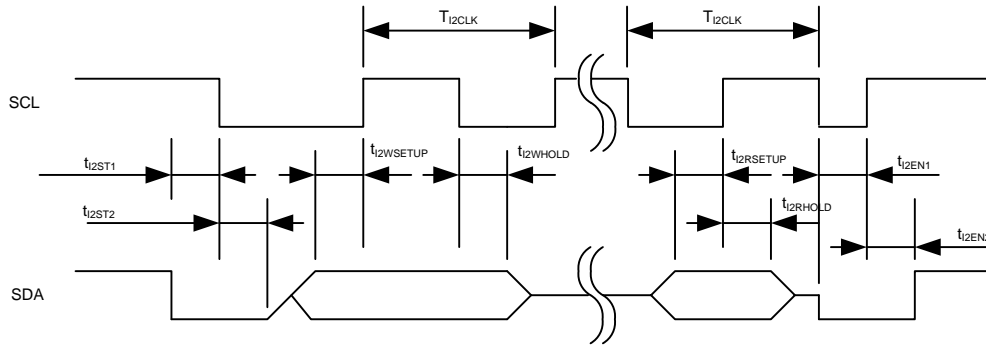
**Figure 12. Interrupt timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

Symbol	Parameter	Min	Typ	Max	Unit
$t_{wINT}$	INT0, NMI Interrupt Assertion Time	4	-	-	SYSCCLK
$t_{dINT}$	INT0, NMI latency	-	-	4	SYSCCLK

**Table 15. Interrupt AC Timing**

## 6.8 I<sup>2</sup>C AC Timing



**Figure 13. I<sup>2</sup>C Timing**

Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>I2CLK</sub>	I <sup>2</sup> C clock period	10	-	8192	SYSCLK
t <sub>I2ST1</sub>	I <sup>2</sup> C SDA start time	0.25	-	-	T <sub>I2CLK</sub>
t <sub>I2ST2</sub>	I <sup>2</sup> C SCL start time	0.25	-	-	T <sub>I2CLK</sub>
t <sub>I2WSETUP</sub>	I <sup>2</sup> C write setup time	0.25	-	-	T <sub>I2CLK</sub>
t <sub>I2WHOLD</sub>	I <sup>2</sup> C write hold time	0.25	-	-	T <sub>I2CLK</sub>
t <sub>I2RSETUP</sub>	I <sup>2</sup> C read setup time	I <sup>2</sup> C filter time <sup>(1)</sup>	-	-	SYSCLK
t <sub>I2RHOLD</sub>	I <sup>2</sup> C read hold time	1	-	-	SYSCLK

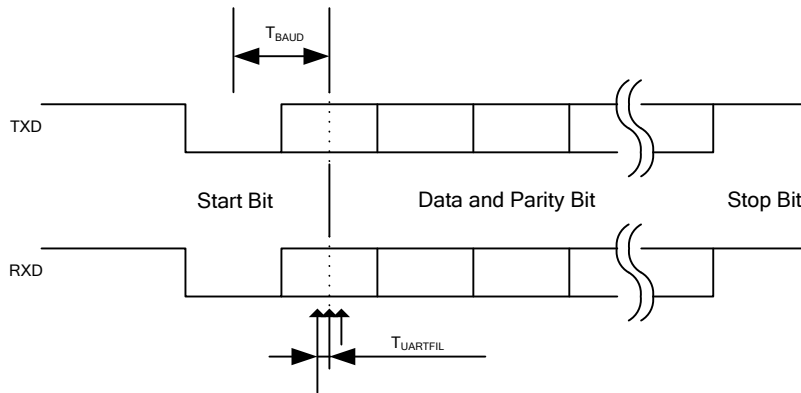
**Table 16. I<sup>2</sup>C AC Timing**

Note:

(1) I<sup>2</sup>C read setup time is determined by the programmable filter time applied to I<sup>2</sup>C communication.



**6.9 UART AC Timing**



**Figure 14. UART timing**

Unless specified, Ta = 25°C.

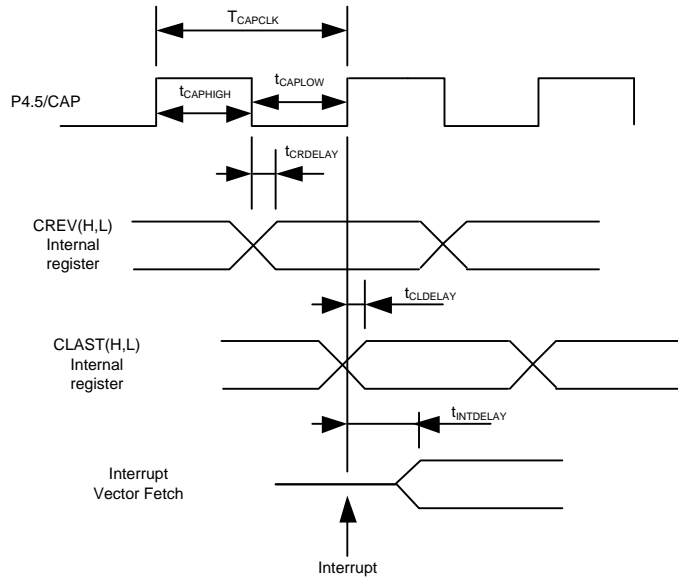
Symbol	Parameter	Min	Typ	Max	Unit
T <sub>BAUD</sub>	Baud Rate Period	-	57600	-	bit/sec
T <sub>UARTFIL</sub>	UART sampling filter period <sup>(1)</sup>	-	1/16	-	T <sub>BAUD</sub>

**Table 17. UART AC Timing**

Note:

- (1) Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T<sub>BAUD</sub>. If three sampled values do not agree, then UART noise error is generated.

### 6.10 CAPTURE Input AC Timing



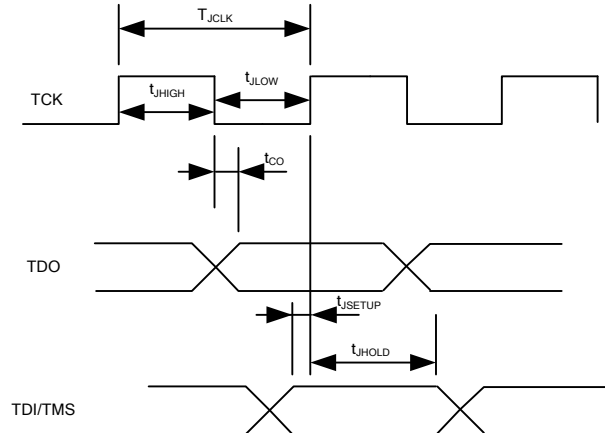
**Figure 15. CAPTURE timing**

Unless specified,  $T_a = 25^\circ\text{C}$ .

Symbol	Parameter	Min	Typ	Max	Unit
$T_{CAPCLK}$	CAPTURE input period	8	-	-	SYCLK
$t_{CAPHIGH}$	CAPTURE input high time	4	-	-	SYCLK
$t_{CAPLOW}$	CAPTURE input low time	4	-	-	SYCLK
$t_{CRDELAY}$	CAPTURE falling edge to capture register latch time	-	-	4	SYCLK
$t_{CLDELAY}$	CAPTURE rising edge to capture register latch time	-	-	4	SYCLK
$t_{INTDELAY}$	CAPTURE input interrupt latency time	-	-	4	SYCLK

**Table 18. CAPTURE AC Timing**

### 6.11 JTAG AC Timing



**Figure 16. JTAG timing**

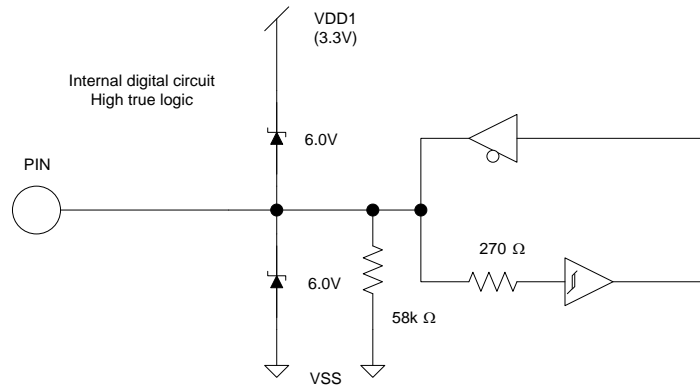
Unless specified, Ta = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
T <sub>JCLK</sub>	TCK Period	-	-	50	MHz
t <sub>JHIGH</sub>	TCK High Period	10	-	-	nsec
t <sub>JLOW</sub>	TCK Low Period	10	-	-	nsec
t <sub>CO</sub>	TCK to TDO propagation delay time	0	-	5	nsec
t <sub>JSETUP</sub>	TDI/TMS setup time	4	-	-	nsec
t <sub>JHOLD</sub>	TDI/TMS hold time	0	-	-	nsec

**Table 19. JTAG AC Timing**

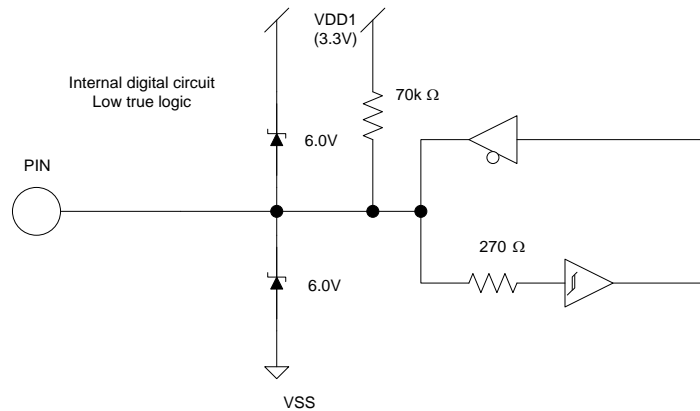
## 7 I/O Structure

The following figure shows the PWM output (CPWMUH/CPWMUL/CPWMVH/CPWMVL/CPWMWH/CPWMWL/PFCPWM/FPWMUL/FPWMUH/FPWMVL/FPWMVH/FPWMWL/FPWMWH)



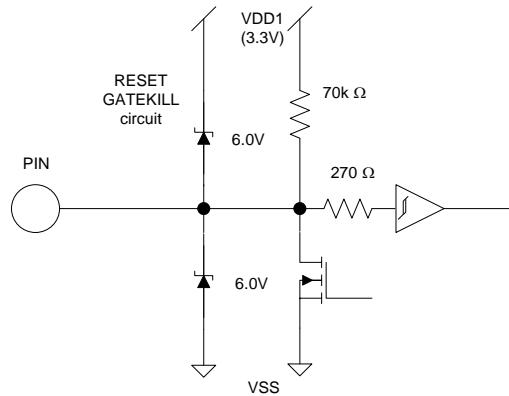
**Figure 17. Compressor, Fan and PFC PWM outputs**

The following figure shows the digital I/O structure except the PWM output



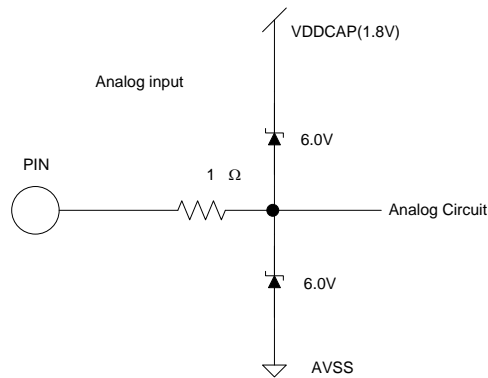
**Figure 18. All digital I/O except PWM output**

The following figure shows RESET and CGATEKILL, PFCGKILL I/O for structure.



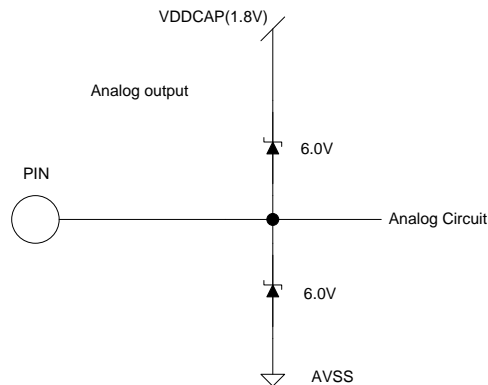
**Figure 19. RESET, GATEKILL I/O**

The following figure shows the analog input structure:



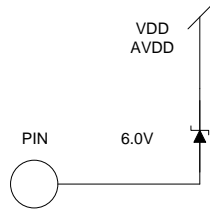
**Figure 20. Analog input**

The following figure shows all analog operational amplifier output pins and AREF pin I/O structure.



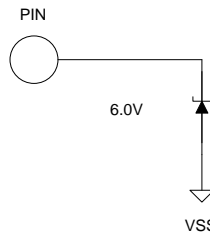
**Figure 21 Analog operational amplifier output and AREF I/O structure**

The following figure shows the VSS,AVSS pin I/O structure



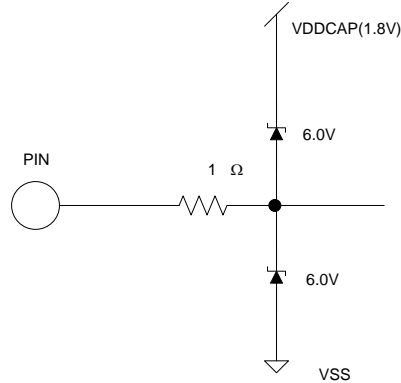
**Figure 22. VSS,AVSS pin I/O structure**

The following figure shows the VDD,VDDCAP pin I/O structure



**Figure 23. VDD,VDDCAP pin I/O structure**

The following figure shows the XTAL0 and XTAL1 pins structure



**Figure 24. XTAL0/XTAL1 pins structure**

## 8 Pin List

Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
1	IFBF2-		I	Op amp positive input for 2 <sup>nd</sup> leg shunt resistor current sensing of Fan motor, 0-1.2V range
2	P2.5		I/O	Discrete programmable I/O
3	P2.6/AOPWM0		I/O	Discrete programmable I/O or PWM 0 digital output
4	P2.7/AOPWM1		I/O	Discrete programmable I/O or PWM 1 digital output
5	IFBF1O		O	Op amp output for 1 <sup>st</sup> leg or single shunt resistor current sensing of Fan motor, 0-1.2V range
6	IFBC2O		O	Op amp output 2 <sup>nd</sup> leg shunt current sensing of compressor motor, 0-1.2V range
7	IFBC2-		I	Op amp negative input 2 <sup>nd</sup> leg shunt current sensing of compressor motor, 0-1.2V range, needs to be pulled down to AVSS if unused
8	IFBC2+		I	Op amp positive input 2 <sup>nd</sup> leg shunt current sensing of compressor motor, 0-1.2V range, needs to be pulled down to AVSS if unused
9	IFBF1-		I	Op amp negative input for 1 <sup>st</sup> leg or single shunt resistor current sensing of Fan motor, 0-1.2V range
10	IFBF1+		I	Op amp positive input for 1 <sup>st</sup> leg or single shunt resistor current sensing of Fan motor, 0-1.2V range
11	AIN0		I	Analog input channel (0 – 1.2V) for DC voltage sensing, needs to be pulled down to AVSS if unused
12	AIN1		I	Analog input channel 1, 0-1.2V range, for AC voltage sensing, needs to be pulled down to AVSS if unused
13	AIN2		I	Analog input channel 2, 0-1.2V range, needs to be pulled down to AVSS if unused
14	AIN3		I	Analog input channel 3, 0-1.2V range, needs to be pulled down to AVSS if unused
15	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
16	AIN4		I	Analog input channel 4, 0-1.2V range, needs to be pulled down to AVSS if unused
17	AIN5		I	Analog input channel 5, 0 – 1.2V range, needs to be pulled down to AVSS if unused
18	VDD		P	3.3V digital power
19	IFBC-		I	Op amp negative input for 1 <sup>st</sup> leg or single shunt current sensing of compressor motor, 0-1.2V range, needs to be pulled down to AVSS if unused
20	IFBC+		I	Op amp positive input for 1 <sup>st</sup> leg or single shunt current sensing of compressor motor, 0-1.2V range, needs to be pulled down to AVSS if unused
21	IFBCO		O	Op amp output for 1 <sup>st</sup> leg or single shunt current sensing of compressor motor, 0-1.2V range
22	VSS		P	Analog and Digital Common
23	VSS		P	Analog and Digital Common
24	VPP		P	OTP programming voltage for Fan MCE
25	AREF		O	Analog reference voltage output (0.6V)
26	VSS		P	Analog and Digital Common
27	IPFC-		I	Op amp negative input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused

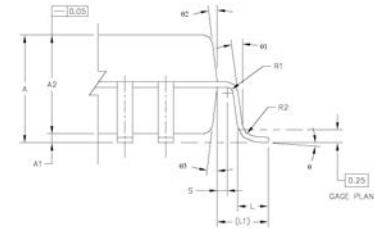
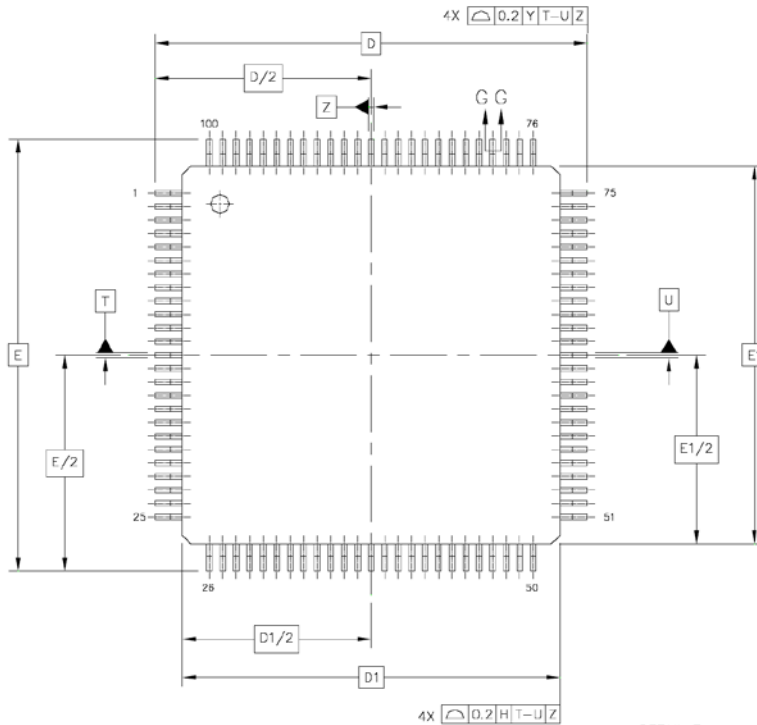
Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
28	IPFC+		I	Op amp positive input for application sensing, 0-1.2V range, needs to be pulled down to AVSS if unused
29	IPFCO		O	Op amp output for application sensing, 0-1.2V range
30	AVSS		P	Analog common
31	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
32	FPWMUL	58 kΩ Pull down	O	PWM gate drive for phase U low side of Fan motor, configurable either high or low true
33	FPWMVL	58 kΩ Pull down	O	PWM gate drive for phase V low side of Fan motor, configurable either high or low true
34	FPWMWL	58 kΩ Pull down	O	PWM gate drive for phase W low side of Fan motor, configurable either high or low true
35	VDD		P	3.3V power
36	VSS		P	Analog and Digital common
37	P3.1/AOPWM2		I/O	Discrete programmable I/O or PWM 2 digital output
38	FPWMUH	58 kΩ Pull down	O	PWM gate drive for phase U high side of Fan, configurable either high or low true
39	FPWMVH	58 kΩ Pull down	O	PWM gate drive for phase V high side of Fan motor, configurable either high or low true.
40	FPWMWH	58 kΩ Pull down	O	PWM gate drive for phase W high side of Fan motor, configurable either high or low true
41	CPWMWL	58 kΩ Pull down	O	PWM gate drive for phase W low side of compressor motor, configurable either high or low true.
42	CPWMVL	58 kΩ Pull down	O	PWM gate drive for phase V low side of compressor motor, configurable either high or low true
43	CPWMUL	58 kΩ Pull down	O	PWM gate drive for phase U low side of compressor motor, configurable either high or low true
44	CPWMWH	58 kΩ Pull down	O	PWM gate drive for phase W high side of compressor motor, configurable either high or low true
45	P3.7		I/O	Discrete programmable I/O
46	P2.1		I/O	Discrete programmable I/O
47	P3.6		I/O	Discrete programmable I/O
48	P4.0/ITRIP	49 kΩ Pull up	I/O	Discrete programmable I/O or Fan motor overcurrent trip input, active low
49	P4.1/AOPWM3		I/O	Discrete programmable I/O or PWM 3 digital output
50	P4.2/AOPWM4		I/O	Discrete programmable I/O or PWM 4 digital output
51	CPWMVH	58 kΩ Pull down	O	PWM gate drive for phase V high side of compressor motor, configurable either high or low true
52	CPWMUH	58 kΩ Pull down	O	PWM gate drive for phase U high side of compressor motor, configurable either high or low true
53	P4.3		I/O	Discrete programmable I/O
54	P1.5		I/O	Discrete programmable I/O
55	PFCPWM		I/O	PFC PWM gate drive , configurable either high or low
56	PFCGKILL	70 kΩ Pull up	I	PFCPWM shutdown input, active low input.
57	P4.4		I/O	Discrete programmable I/O
58	CGATEKILL	70 kΩ Pull up	I	PWM shutdown input, configurable digital filter, active low input.
59	P3.0	70 kΩ Pull up	I/O	Discrete programmable I/O
60	P4.5/CAP		I/O	Discrete programmable I/O or Capture timer input
61	P5.2/TMS		I	JTAG test mode select or digital input port
62	P4.6/RXD2		I/O	Discrete programmable I/O, 2 <sup>nd</sup> UART receive



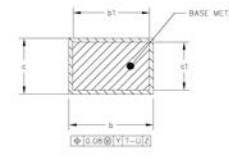
Pin Number	Pin Name	Internal Pull-up /Pull-down	Pin Type	Description
63	P5.3/TDO		O	JTAG test data output
64	P5.1/TDI		I	JTAG test data input or digital input port
65	P4.7/TXD2		I/O	Discrete programmable I/O, 2 <sup>nd</sup> UART transmit
66	TCK		I	JTAG test clock
67	RESET		I	Reset, low true, Schmitt trigger input
68	P1.1/RXD1		I/O	UART receiver input or Discrete programmable I/O
69	VSS		P	Analog and Digital common
70	P1.2/TXD1		I/O	UART transmitter output or Discrete programmable I/O
71	P3.4/T0		I/O	Discrete programmable I/O or Timer/Counter 2 input
72	FS4		I/O	Factory use, need to be connected to pin73
73	FS4		I/O	Factory use, need to be connected to pin72
74	FS3		I/O	Factory use, need to be connected to pin75
75	FS3		I/O	Factory use, need to be connected to pin74
76	XTAL0		I	Crystal input
77	XTAL1		O	Crystal output
78	P1.0/T2		I/O	Discrete programmable I/O or Timer/Counter 2 input
79	SCL		I/O	I <sup>2</sup> C clock output (open drain, need pull up)
80	SDA		I/O	I <sup>2</sup> C data (open drain, need pull up)
81	FS2		I/O	Factory use, need to be connected to pin84
82	FS1		I/O	Factory use, need to be connected to pin83
83	FS1		I/O	Factory use, need to be connected pin82
84	FS2		I/O	Factory use, need to be connected to pin81
85	AIN9		I	Analog input channel (0 – 1.2V), needs to be pulled down to AVSS if unused
86	AIN8		I	Analog input channel (0 – 1.2V), needs to be pulled down to AVSS if unused
87	P2.4		I/O	Discrete programmable I/O
88	P1.6		I/O	Discrete programmable I/O
89	P1.7			Discrete programmable I/O
90	AIN7		I	Analog input channel (0 – 1.2V), needs to be pulled down to AVSS if unused
91	VDD		P	3.3V digital power
92	AIN6		I	Analog input channel (0 – 1.2V)
93	VSS		P	Digital common
94	VDDCAP		P	Internal 1.8V output, Capacitor(s) to be connected
95	P2.0/NMI		I/O	Discrete programmable I/O or Non-maskable Interrupt input
96	P3.2/INT0		I/O	Discrete programmable I/O or Interrupt 0 input
97	P2.2		I/O	Discrete programmable I/O
98	P2.3		I/O	Discrete programmable I/O
99	IFB2O		O	Op amp output for 2 <sup>nd</sup> leg shunt resistor current sensing of Fan motor, 0-1.2V range
100	IFB2-		I	Op amp negative input for 2 <sup>nd</sup> leg shunt resistor current sensing of Fan motor, 0-1.2V range

**Table 20. Pin List**

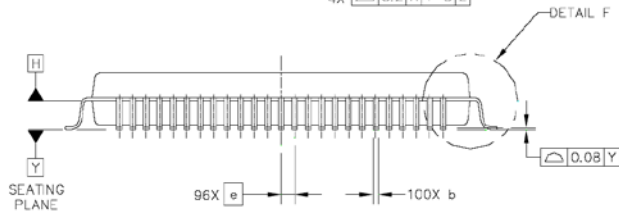
## 9 Package Dimensions



DETAIL F



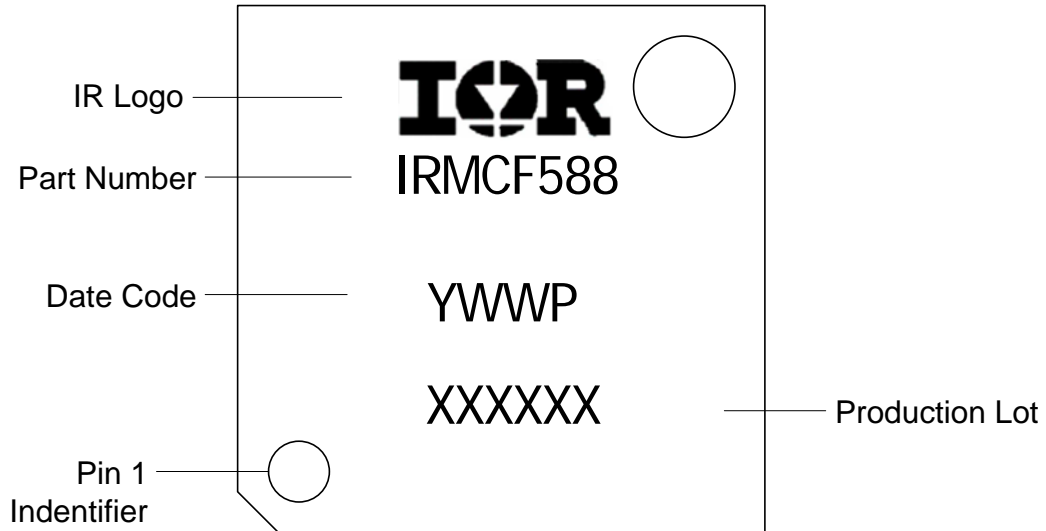
SECTION G-G


**NOTES:**

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.2	0.27	S	0.2		---				
b1	0.17		0.23	ø	0*	3.5*	7*				
c	0.09		0.2	ø1	0*		---				
c1	0.09		0.16	ø2	11*	12*	13*				
D		16 BSC		ø3	11*	12*	13*				
D1		14 BSC									
e		0.5 BSC									
E		16 BSC									
E1		14 BSC									
L	0.45	0.6	0.75								
			UNIT			DIMENSION AND TOLERANCES			REFERENCE DOCUMENT		
			MM			ASME Y14.5M			64-06-A000-PT03-C		
TITLE: LOFP 100 LD 14X14X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT (JEDEC)											

## 10 Part Marking Information



**Part Marking**

## 11 Qualification Information

<b>Qualification Level</b>		Industrial <sup>††</sup> (per JEDEC JESD 47E)
<b>Moisture Sensitivity Level</b>		MSL3 <sup>†††</sup> (per IPC/JEDEC J-STD-020C)
<b>ESD</b>	<b>Machine Model</b>	Class B (per JEDEC standard JESD22-A114D)
	<b>Human Body Model</b>	Class 2 (per EIA/JEDEC standard EIA/JESD22-A115-A)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Note:** Test condition for Temperature Cycling test is -40C to 125C.

## Revision History

International  
 Rectifier

Data and Specifications are subject to change without notice  
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