ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V+, IN_ .....-0.3V to +4V
COM_, NO_, NC_ (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current (COM_, NO_, NC_).....±100mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms 10% duty cycle).....±200mA
Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 9.1W/°C above +70°C) 727mW
QFN (derate 16.9W/°C above +70°C) 1349mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, $V_{IH\_}$ = +1.4V, $V_{IL\_}$ = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance (Note 4)	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.6	0.9	Ω
			T_{MIN} to T_{MAX}			1	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.03	0.12	Ω
			T_{MIN} to T_{MAX}			0.15	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1V, 1.5V, 2V	+25°C		0.04	0.1	Ω
			T_{MIN} to T_{MAX}			0.12	
NO_ or NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.6V, $V_{NO\_}$ or $V_{NC\_}$ = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T_{MIN} to T_{MAX}	-5		+5	
COM_ Off-Leakage Current (Note 7)	$I_{COM\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.6V, $V_{NO\_}$ or $V_{NC\_}$ = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T_{MIN} to T_{MAX}	-5		+5	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.6V, $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.6V, or unconnected	+25°C	-2.5	0.002	+2.5	nA
			T_{MIN} to T_{MAX}	-5		+5	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, $V_{IH\_}$ = +1.4V, $V_{IL\_}$ = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		6	30	ns
			T_{MIN} to T_{MAX}			30	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		10	25	ns
			T_{MIN} to T_{MAX}			25	
Break-Before-Make (Note 8) (MAX4753 Only)	t_{BBM}	$V_{NO\_}$ and $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		7		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 2	+25°C		21		pC
NO_ or NC_ Off-Capacitance	C_{OFF}	f = 1MHz, Figure 3	+25°C		31		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 3	+25°C		30		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 3	+25°C		75		pF
Off-Isolation (Note 9)	V_{ISO}	R_L = 50Ω, C_L = 5pF, Figure 4, f = 10MHz	+25°C		-51		dB
		R_L = 50Ω, C_L = 5pF, Figure 4, f = 1MHz	+25°C		-65		
Crosstalk		R_L = 50Ω, C_L = 5pF, Figure 4, f = 10MHz	+25°C		-70		dB
		R_L = 50Ω, C_L = 5pF, Figure 4, f = 1MHz	+25°C		-80		
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $V_{COM\_}$ = $2V_{P-P}$, R_L = 32Ω	+25°C		0.031		%
DIGITAL I/O							
Input Logic High	$V_{IH\_}$		T_{MIN} to T_{MAX}	1.4			V
Input Logic Low	$V_{IL\_}$		T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	$I_{IN\_}$	$V_{IN\_}$ = 0 or V+	T_{MIN} to T_{MAX}	-1	0.0005	+1	µA
POWER SUPPLY							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	V+ = 3.6V, $V_{IN\_}$ = 0 or V+				1	µA

ELECTRICAL CHARACTERISTICS—Single +1.8V Supply

(V+ = +1.8V, V_{IH} = +1V, V_{IL} = +0.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance (Note 4)	R_{ON}	V+ = 1.8V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0.9V	+25°C		1.4	2.5	Ω
			T_{MIN} to T_{MAX}			3	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 1.8V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0.9V	+25°C		0.05	0.25	Ω
			T_{MIN} to T_{MAX}			0.25	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.0V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		25	35	ns
			T_{MIN} to T_{MAX}			35	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 1.0V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		20	25	ns
			T_{MIN} to T_{MAX}			30	
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 2	+25°C		8		pC
DIGITAL I/O							
Input Logic High	$V_{IH\_}$		T_{MIN} to T_{MAX}	1.0			V
Input Logic Low	$V_{IL\_}$		T_{MIN} to T_{MAX}			0.4	V
Input Leakage Current	$I_{IN\_}$	$V_{IN\_}$ = 0 or V+	T_{MIN} to T_{MAX}	-1	0.0005	+1	µA
POWER SUPPLY							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	$V_{IN\_}$ = 0 or V+				1	µA

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Parts are tested at +85°C and guaranteed by design and correlation over the full temperature range.

Note 4: R_{ON} and ΔR_{ON} matching specifications for QFN-packaged parts are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Leakage parameters are 100% tested at the maximum-rated hot operating temperature and guaranteed by correlation at T_A = +25°C.

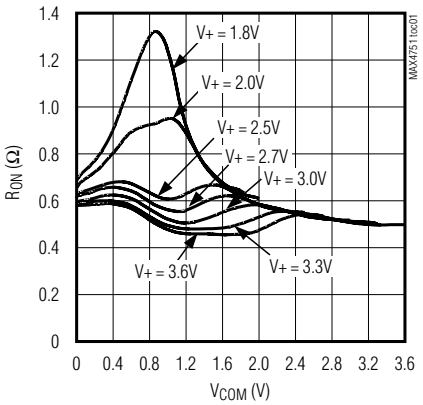
Note 8: Guaranteed by design, not production tested.

Note 9: Off-Isolation = $20\log_{10}[V_{COM} / (V_{NC}$ or $V_{NO})]$, V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

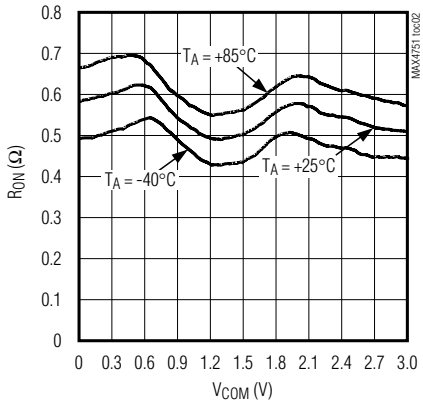
Typical Operating Characteristics

(V+ = +3V and T_A = +25°C, unless otherwise noted.)

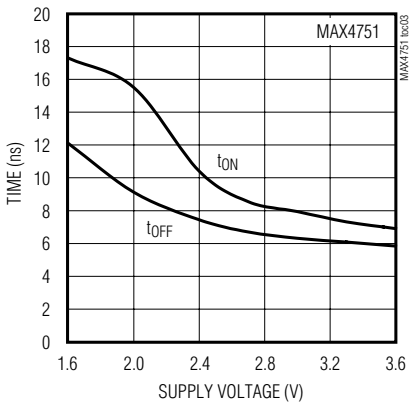
ON-RESISTANCE vs. V_{COM}



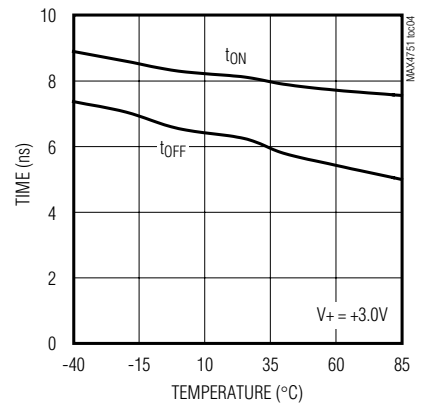
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



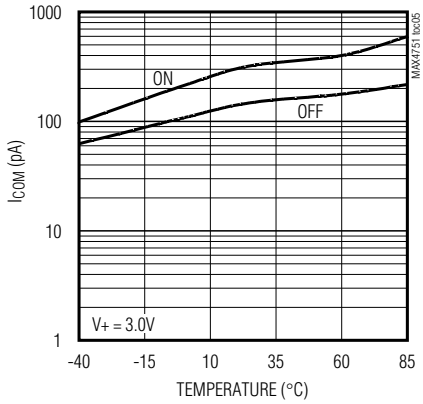
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



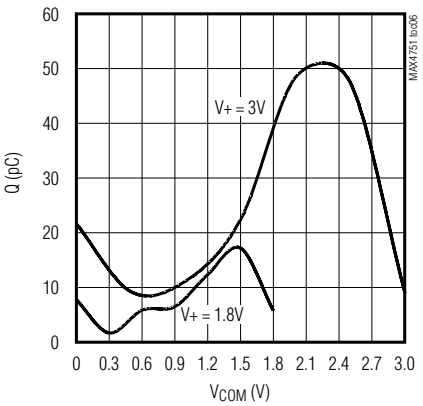
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



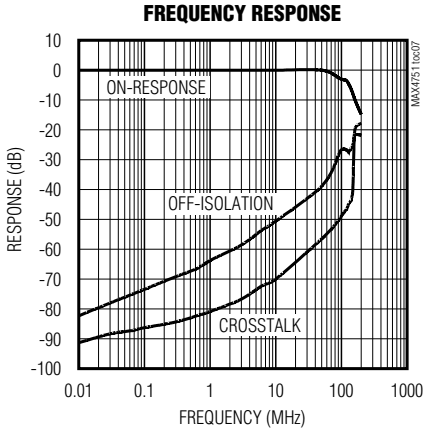
LEAKAGE CURRENT vs. TEMPERATURE



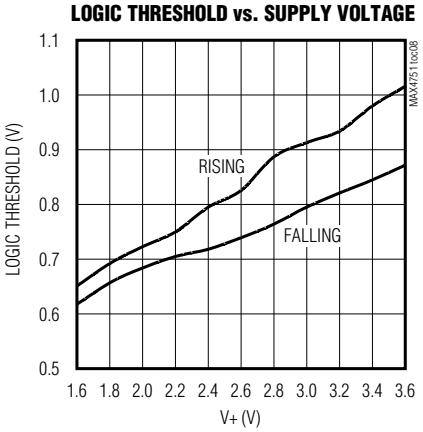
CHARGE INJECTION vs. V_{COM}



FREQUENCY RESPONSE



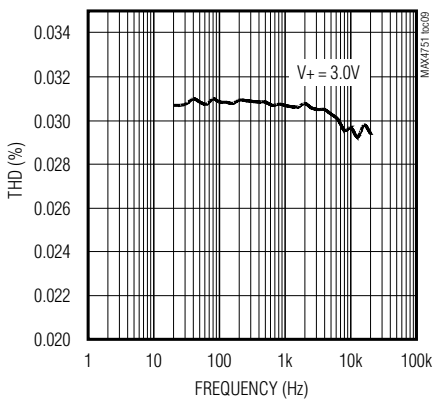
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



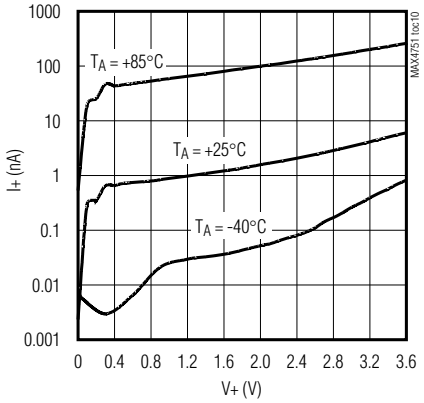
Typical Operating Characteristics (continued)

(V+ = +3V and T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION vs. FREQUENCY



SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



Pin Description

PIN						NAME	FUNCTION
MAX4751		MAX4752		MAX4753			
TSSOP	QFN-EP	TSSOP	QFN-EP	TSSOP	QFN-EP		
1, 3, 8, 11	15, 1, 7, 11	—	—	—	—	NO1, NO2, NO3, NO4	Switch Normally Open Terminals
—	—	1, 3, 8, 11	15, 1, 7, 11	—	—	NC1, NC2, NC3, NC4	Switch Normally Closed Terminals
—	—	—	—	3, 11	1, 11	NC2, NC4	Switch Normally Closed Terminals
—	—	—	—	1, 8	15, 7	NO1, NO3	Switch Normally Open Terminals
2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	COM1, COM2, COM3, COM4	Switch Common Terminals
7	6	7	6	7	6	GND	Ground
13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	IN1, IN2, IN3, IN4	Logic Control Inputs
14	14	14	14	14	14	V+	Positive Supply Voltage
—	3, 10	—	3, 10	—	3, 10	N.C.	No Connection. Not internally connected.
—	—	—	—	—	—	EP	Exposed Pad (QFN Only). Connect EP to GND.

Test Circuits/Timing Diagrams

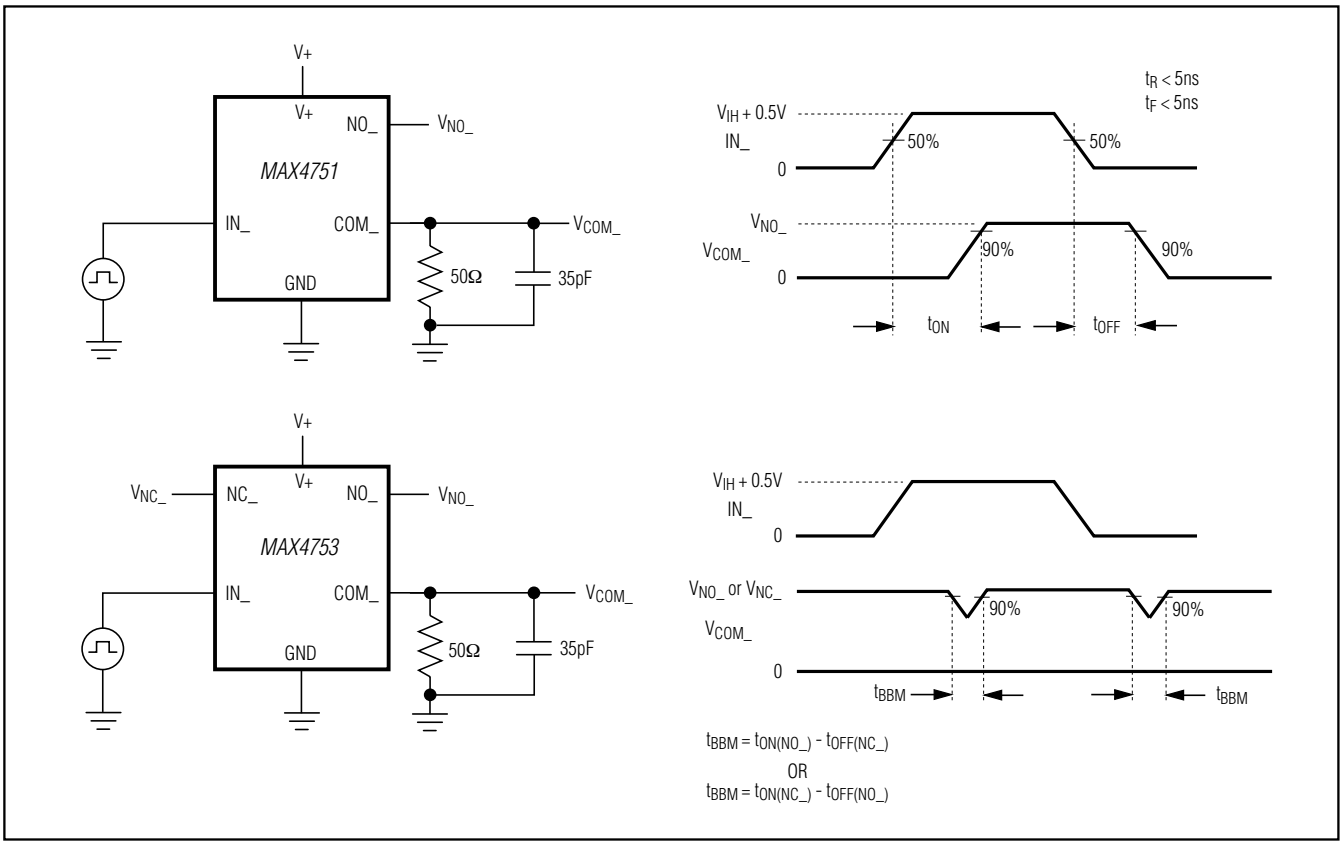


Figure1. Switching Times

Test Circuits/Timing Diagrams (continued)

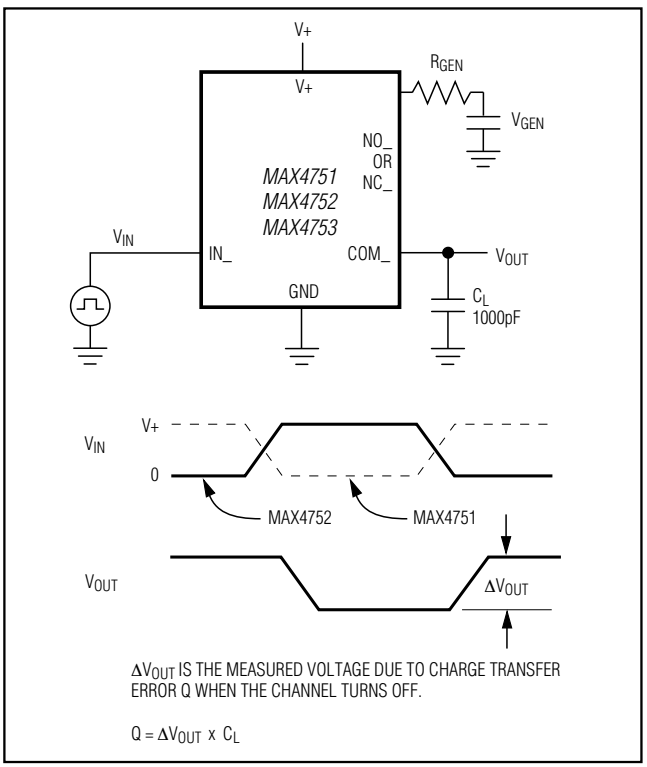


Figure 2. Charge Injection

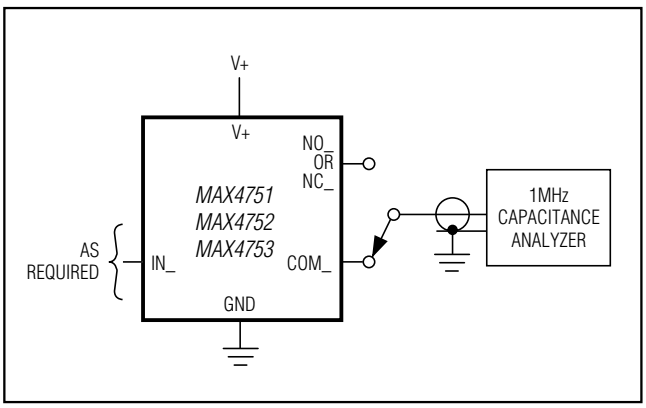


Figure 3. NO_, NC_, and COM_ Capacitance

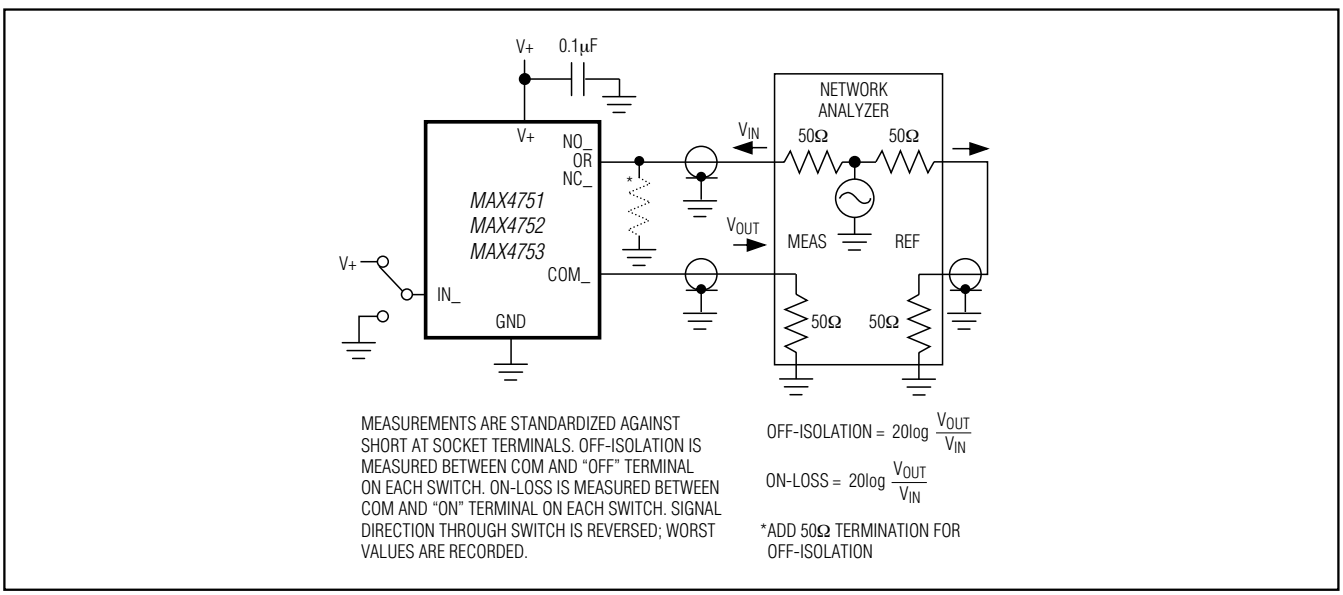


Figure 4. Off-Isolation, On-Loss, and Crosstalk

Detailed Description

The MAX4751/MAX4752/MAX4753 are low 0.9Ω max (at V+ = 3V) on-resistance, low-voltage quad analog switches that operate from a +1.6V to +3.6V single supply. CMOS construction allows switching analog signals that are within the supply voltage range (GND to V+).

When powered from a +3V supply, the 0.9Ω (max) R_{ON} allows high continuous currents to be switched in a variety of applications.

Applications Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, followed by NO_, NC_, or COM_. If power-supply sequencing is not possible, add two small-signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 5). Adding these diodes reduces the analog signal by one diode drop below V+ and one diode drop above GND, but does not affect the low switch resistance and low leakage characteristics of the device. Device operation is unchanged, and the difference between V+ and GND should not exceed 4V.

Power-supply bypassing is needed to improve noise margin and to prevent switching noise propagation from the V+ supply to other components. A 0.1µF capacitor, connected from V+ to GND, is adequate for most applications.

Logic Inputs

The MAX4751/MAX4752/MAX4753 logic inputs can be driven up to +3.6V regardless of the supply voltage. For example, with a +1.8V supply, IN_ may be driven low to GND and high to +3.6V. Driving IN_ rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be passed with very little change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be used as either inputs or outputs.

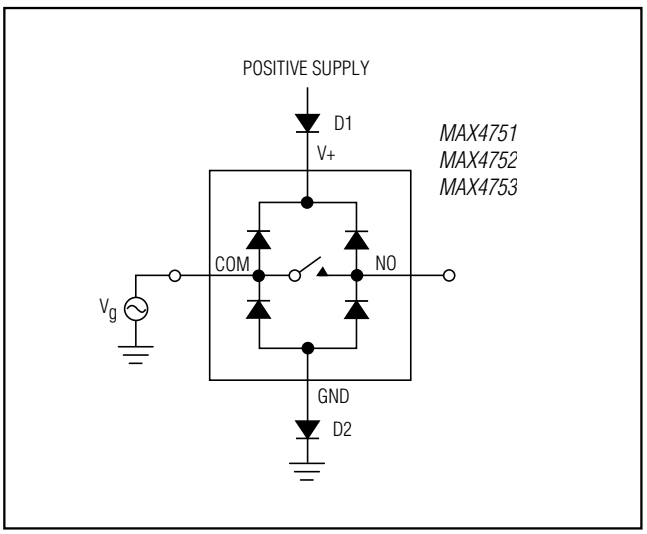


Figure 5. Overvoltage Protection Using Two External Blocking Diodes

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

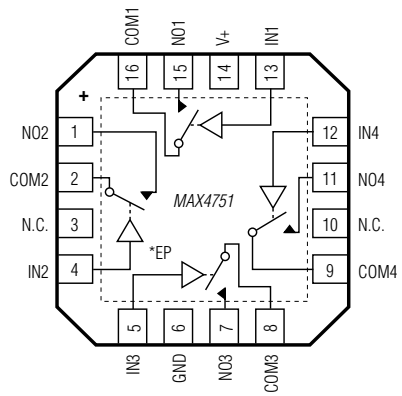
Chip Information

TRANSISTOR COUNT: 228

PROCESS: CMOS

Pin Configurations/Functional Diagrams/Truth Tables (continued)

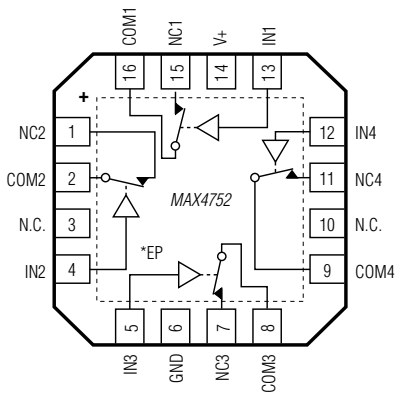
TOP VIEW



QFN

*CONNECT EP TO GND

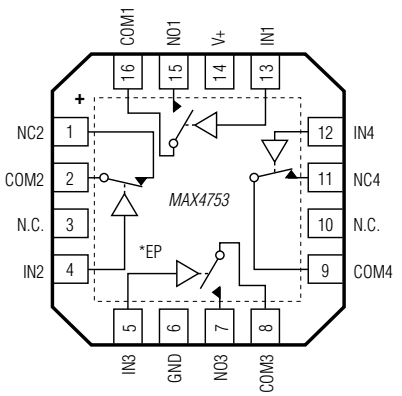
MAX4751	
INPUT	SWITCH STATE
LOW	OFF
HIGH	ON



QFN

*CONNECT EP TO GND

MAX4752	
INPUT	SWITCH STATE
LOW	ON
HIGH	OFF



QFN

*CONNECT EP TO GND

MAX4753		
INPUT	SWITCHES 1, 8	SWITCHES 2, 4
LOW	OFF	ON
HIGH	ON	OFF

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	21-0066	90-0113
16 QFN	G1633+2	21-0102	90-0215

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	1/13	Corrected packaging information	1, 2, 6, 10–13

Mouser Electronics

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Maxim Integrated:

MAX4751EGE+ MAX4751EGE+T MAX4751EUD+ MAX4751EUD+T MAX4752EGE+ MAX4752EGE+T MAX4752EUD+ MAX4752EUD+T MAX4753EGE+ MAX4753EGE+T MAX4753EUD+T MAX4753EUD+