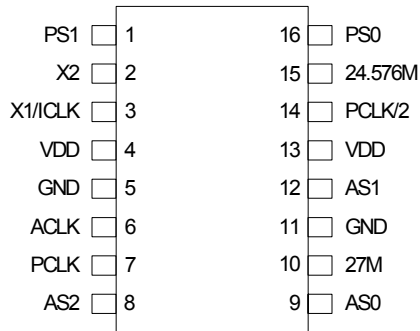


Pin Assignment



16-pin (150 mil) SOIC

Audio Clock (MHz) Decoding Table

AS2	AS1	AS0	ACLK
0	0	0	12.288
0	0	1	11.2896
0	1	0	8.192
0	1	1	24.576
1	0	0	8.192
1	0	1	16.9344
1	1	0	18.432
1	1	1	11.2896

Processor Clock (MHz)

PS1	PS0	PCLK	PCLK/2
0	0	66.66	33.33
0	1	80	40
1	0	50	25
1	1	60	30

0 = connect directly to ground

1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	PS1	Input	Processor clock Select 1. Selects processor clock outputs per table above.
2	X2	XO	Crystal connection. Connect to 27 MHz crystal. Leave unconnected for clock input.
3	X1/CLK	XI	Crystal connection. Connect to 27 MHz crystal or to a 27 MHz input clock.
4	VDD	Power	Connect to +3.3 V or +5 V. Must be same as other VDD.
5	GND	Power	Connect to ground.
6	ACLK	Output	Audio Clock output. Determined by status of AS2, AS1, AS0. See table above.
7	PCLK	Output	Processor Clock output. Determined by status of PS1, PS0. See table above.
8	AS2	Input	Audio clock Select 2. Selects audio clock on pin 6 per table above.
9	AS0	Input	Audio clock Select 0. Selects audio clock on pin 6 per table above.
10	27M	Output	27 MHz clock output.
11	GND	Power	Connect to ground.
12	AS1	Input	Audio clock Select 1. Selects audio clock on pin 6 per table above.
13	VDD	Power	Connect to +3.3 V or +5 V. Must be same as other VDD.

Pin Number	Pin Name	Pin Type	Pin Description
14	PCLK/2	Output	Processor Clock divided by two output. Determined by status of PS1, PS0. See table above.
15	24.576M	Output	24.576 MHz clock output.
16	PS0	Input	Processor clock Select 0. Selects processor clock outputs per table above.

External Components

The MK2745-21 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1 μ F should be connected between VDD and GND, as close to the MK2745-21 as possible. A series termination resistor of 33 Ω may be used for each clock output. If a clock input is not used, the 27 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant, 50 ppm or better. Crystal capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where CL is the crystal load capacitance: Crystal caps (pF) = (CL-6) x 2. So, for a crystal with 16 pF load capacitance, two 20 pF caps should be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2745-21. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD = 5.0 V (unless noted), Temp 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V _{IH}	X1/ICLK pin only	(VDD/2)+1			V
Input Low Voltage	V _{IL}	X1/ICLK pin only			(VDD/2)-1	V
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -8 mA	VDD-0.4			V
Operating Supply Current	IDD	No Load, Note 1		37		mA
Short Circuit Current	I _{OS}	Each output		±100		mA
Input Capacitance	C _{IN}			7		pF

Note 1: With processor clock at 50 MHz and ACLK at 16.93 MHz.

AC Electrical Characteristics

VDD = 5.0 V (unless noted), Temp 0 to +70° C

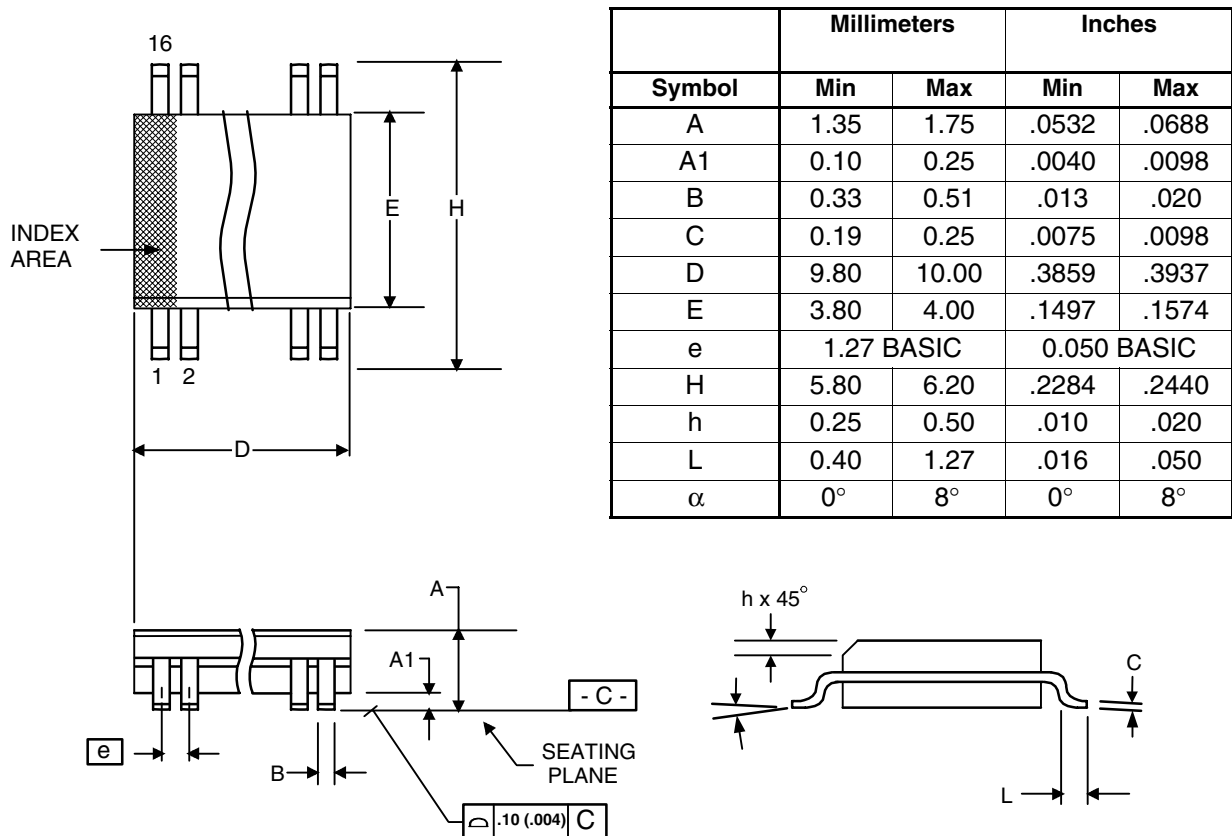
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				27		MHz
Output Clock Rise Time	t _{OR}	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	t _{OF}	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		at VDD/2	40		60	%
Frequency Error				0	1	ppm
Absolute Jitter, short term		Variation from mean		200		ps

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ _{JA}	Still air		120		°C/W
	θ _{JA}	1 m/s air flow		115		°C/W
	θ _{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ _{JC}			58		°C/W

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK2745-21SLF	2745-21SLF	Tubes	16-pin SOIC	0 to 70° C
MK2745-21SLFTR	2745-21SLF	Tape and Reel	16-pin SOIC	0 to 70° C

“LF” denotes Pb (lead) free package

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