MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec)	V_{CC}, V_C	30	V
Total Power Supply and Zener Current	(I_{CC} + I_Z)	30	mA
Output Current, Source or Sink	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Voltage Feedback, V_{ref} and Rt/Ct Inputs	V_{in}	−0.3 to + 5.5	V
Compensation	V_{comp}	−0.3 to + 7.2	V
Output	V_o	−0.3 to V_{CC} or V_C + 0.3	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SOIC−14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SOIC−8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3842B, UC3843B		0 to 70	
UC2842B, UC2843B		−25 to + 85	
UC2843D		−40 to +85	
UC3842BV, UC3843BV		−40 to +105	
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC Standard JESD22-A114B
   Machine Model Method 200 V per JEDEC Standard JESD22-A115-A
2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 3], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

Characteristics	Symbol	UC284XB, UC2843D			UC384XB, XBV			Unit
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}							V
UC284XB		4.9	–	5.1	4.82	–	5.18	
UC2843D		4.82	–	5.18				
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
T_A = T_{low} to T_{high}		48	–	56	48	–	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature, T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak−to−Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C, T_A = T_{low} to T_{high}		7.8	8.3	8.8	7.8	8.3	8.8	
UC284XB, UC384XB		7.5	–	8.8	7.6	–	8.8	
UC2843D, UC384XBV		–	–	–	7.2	–	8.8	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V) UC284XB	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
UC2843D		2.42	2.5	2.58				
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	−0.1	−1.0	–	−0.1	−2.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	−0.5	−1.0	–	−0.5	−1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
UC284XB, UC384XB		–	0.8	1.1	–	0.8	1.1	
UC2843D, UC384XBV		–	–	–	–	0.8	1.2	

3. Adjust V_{CC} above the Startup threshold before setting to 15 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842B, UC3843B; −25°C for UC2842B, UC2843B; −40°C for UC3842BV, UC3843BV, UC2843D
T_{high} = +70°C for UC3842B, UC3843B; +85°C for UC2842B, UC2843B, UC2843D; +105°C for UC3842BV, UC3843BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 7], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 8], unless otherwise noted.)

Characteristics	Symbol	UC284XB, UC2843D			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 5 and 6)	A_V							V/V
UC2843D, UC284XB, UC384XB		2.85	3.0	3.15	2.85	3.0	3.15	
UC384XBV		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 5)	V_{th}							V
UC2843D, UC284XB, UC384XB		0.9	1.0	1.1	0.9	1.0	1.1	
UC384XBV		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V, Note 5)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	−2.0	−10	–	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA) UC284XB, UC384XB		–	1.6	2.2	–	1.6	2.2	
UC384XBV, UC2843D		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA) UC284XB, UC384XB	V_{OH}	13	13.5	–	13	13.5	–	
UC384XBV, UC2843D		–	–	–	12.9	13.5	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold (V_{CC})	V_{th}							V
UCX842B, BV		15	16	17	14.5	16	17.5	
UCX843B, BV, D		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn−On (V_{CC})	$V_{CC(min)}$							V
UCX842B, BV		9.0	10	11	8.5	10	11.5	
UCX843B, BV, D		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum UC284XB, UC384XB, UC2843D	$DC_{(max)}$	94	96	–	94	96	–	
UC384XBV		–	–	–	93	96	–	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	$I_{CC} + I_C$							mA
Startup (V_{CC} = 6.5 V for UCX843B, UC2843D		–	0.3	0.5	–	0.3	0.5	
V_{CC} 14 V for UCX842B, BV)								
(Note 7)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

5. This parameter is measured at the latch trip point with V_{FB} = 0 V.
6. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$
7. Adjust V_{CC} above the Startup threshold before setting to 15 V.
8. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for UC3842B, UC3843B; −25°C for UC2842B, UC2843B; −40°C for UC3842BV, UC3843BV, UC2843D
   T_{high} = +70°C for UC3842B, UC3843B; +85°C for UC2842B, UC2843B, UC2843D; +105°C for UC3842BV, UC3843BV

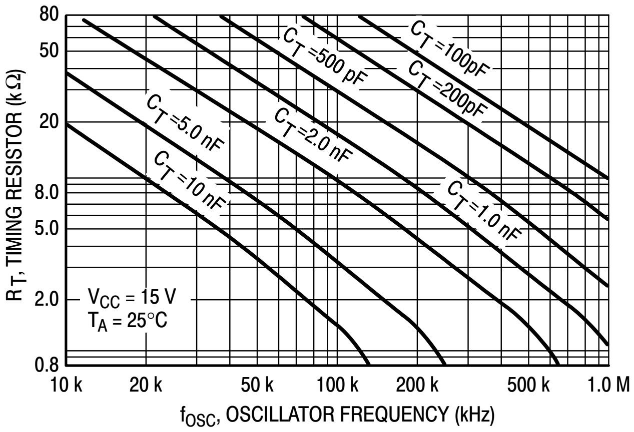


Figure 2. Timing Resistor versus Oscillator Frequency

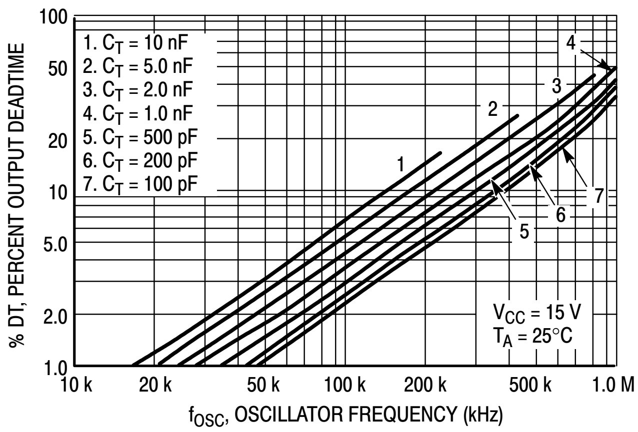


Figure 3. Output Deadtime versus Oscillator Frequency

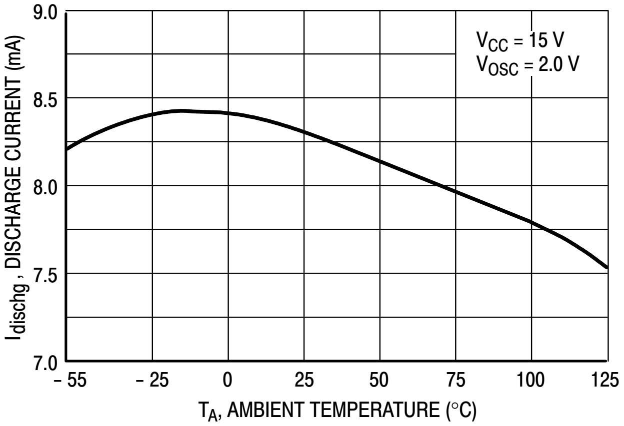


Figure 4. Oscillator Discharge Current versus Temperature

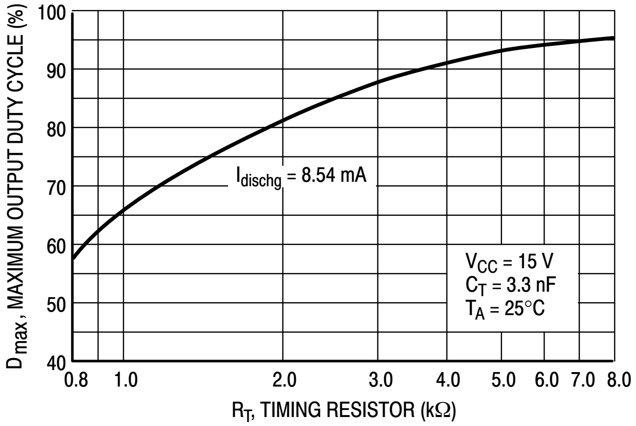


Figure 5. Maximum Output Duty Cycle versus Timing Resistor

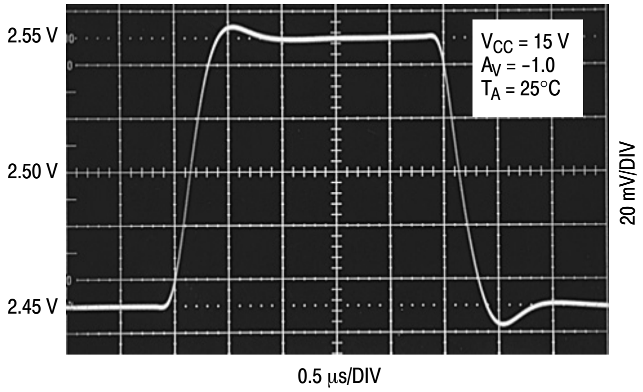


Figure 6. Error Amp Small Signal Transient Response

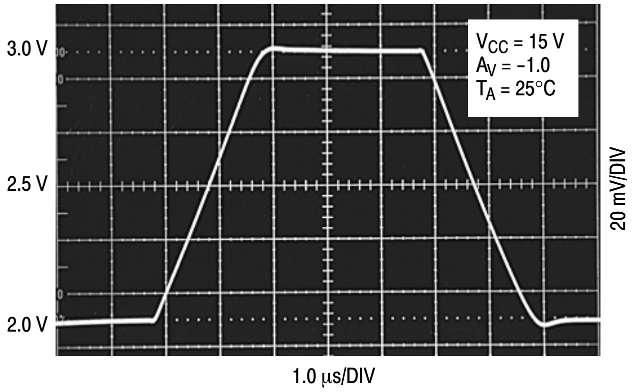


Figure 7. Error Amp Large Signal Transient Response

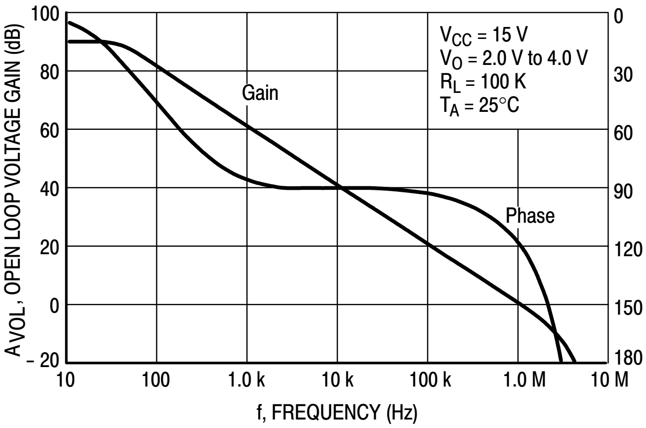


Figure 8. Error Amp Open Loop Gain and Phase versus Frequency

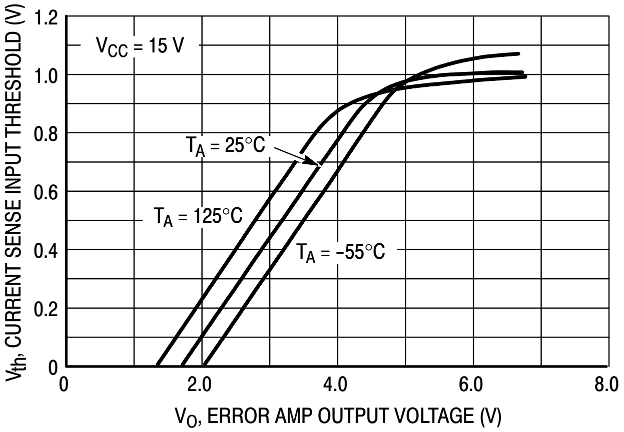


Figure 9. Current Sense Input Threshold versus Error Amp Output Voltage

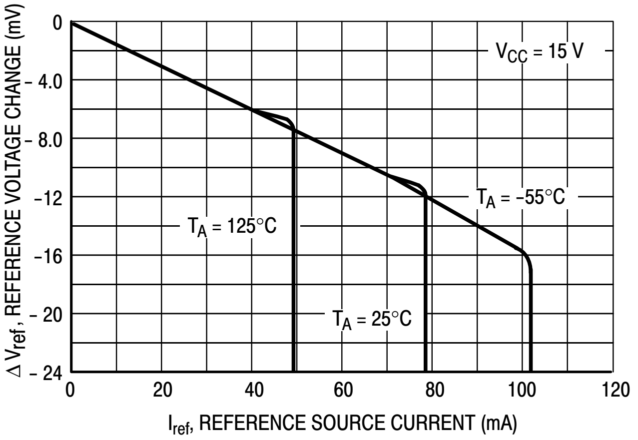


Figure 10. Reference Voltage Change versus Source Current

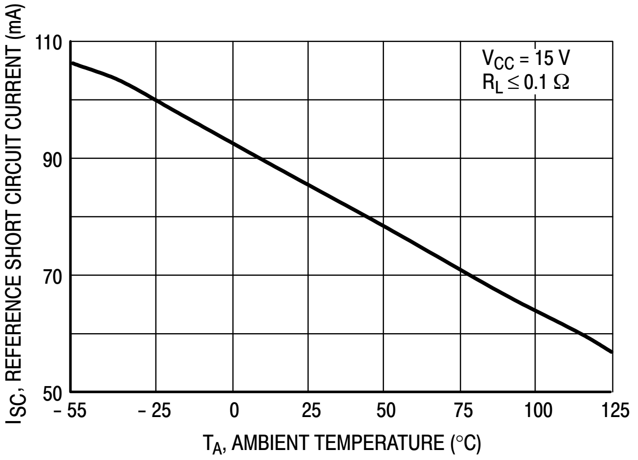


Figure 11. Reference Short Circuit Current versus Temperature

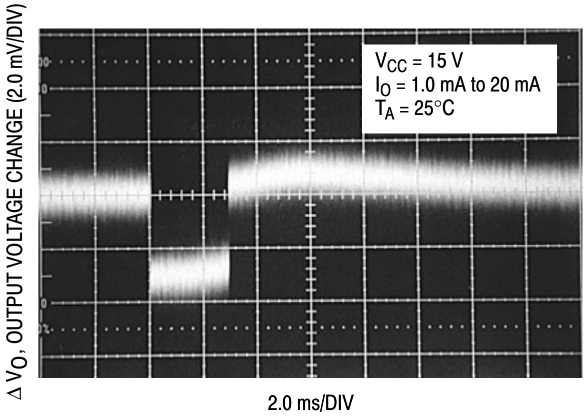


Figure 12. Reference Load Regulation

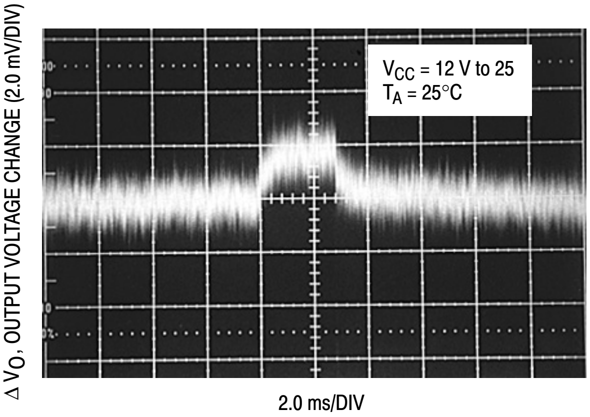


Figure 13. Reference Line Regulation

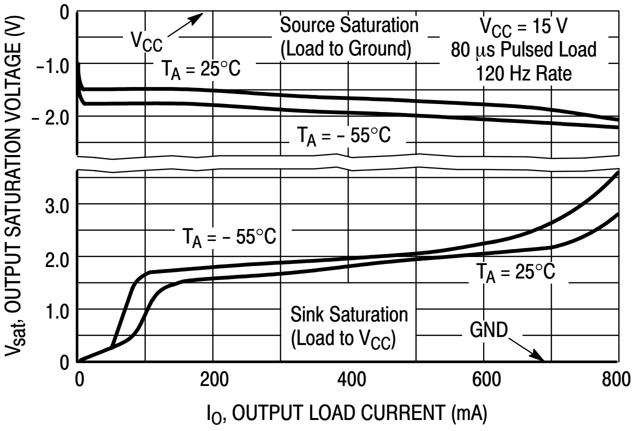


Figure 14. Output Saturation Voltage versus Load Current

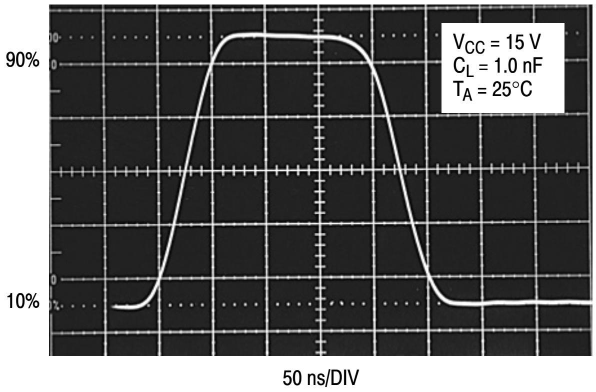


Figure 15. Output Waveform

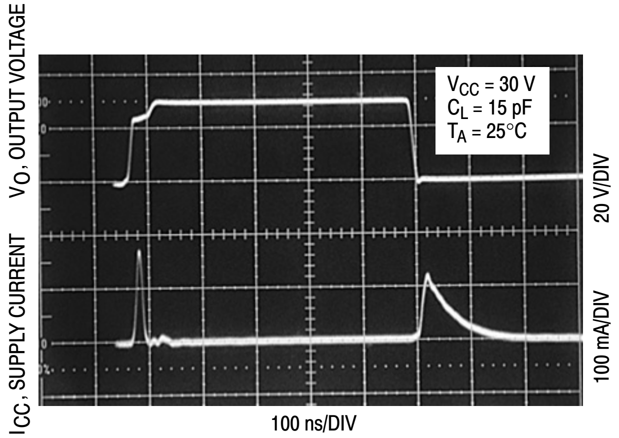


Figure 16. Output Cross Conduction

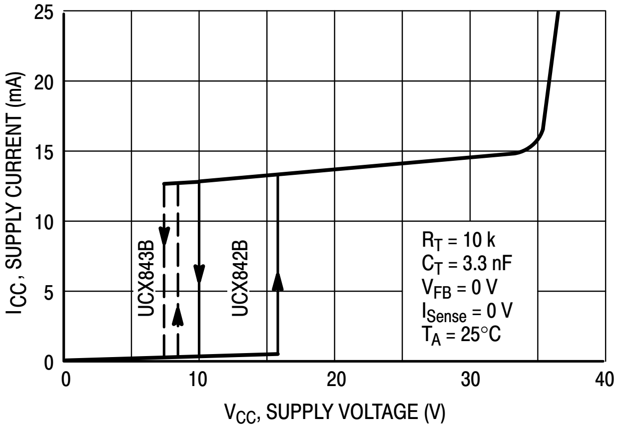


Figure 17. Supply Current versus Supply Voltage

PIN FUNCTION DESCRIPTION

8–Pin	14–Pin	Function	Description
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		GND	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	GND	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842B, UC3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off−Line and DC−to−DC converter applications offering the designer a cost−effective solution with minimal external components. A representative block diagram is shown in Figure 19.

Oscillator

The oscillator frequency is programmed by the values chosen for the timing components R_T and C_T. It must also be noted that the value of R_T uniquely determines the maximum duty ratio of UC384xx. The oscillator configuration depicting the connection of the timing components to the R_T/C_T pin of the controller is shown in Figure 18. Capacitor C_T gets charged from the V_{ref} source, through resistor R_T to its peak threshold $V_{RT/CT(peak)}$, typically 2.8 V. Upon reaching this peak threshold volage, an internal 8.3 mA current source, I_{dischg}, is enabled and the voltage across C_T begins to decrease. Once the voltage across C_T reaches its valley threshold, $V_{RT/CT(valley)}$, typically 1.2 V, I_{dischg} turns off. This allows capacitor C_T to charge up again from V_{ref}. This entire cycle repeats, and the resulting waveform on the R_T/C_T pin has a sawtooth shape. Typical waveforms are shown in Figure 20.

The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Considering the general industry trend of operating switching controllers at higher frequencies, the UC384xx is guaranteed to operate within ±10% at 250 kHz. These internal circuit refinements minimize variations of oscillator frequency and maximum duty ratio.

The charging and discharging times of the timing capacitor C_T are calculated using Equations 1 and 2. These equations do not take into account the propagation delays of the internal comparator. Hence, at higher frequencies, the calculated value of the oscillator frequency differs from the actual value.

$$t_{RT/CT(chg)} = R_T C_T \ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}}\right) \qquad \text{(eq. 1)}$$

$$t_{RT/CT(dischg)} = R_T C_T \ln\left(\frac{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(valley)} - V_{ref}}\right) \qquad \text{(eq. 2)}$$

The maximum duty ratio, D_{max} is given by Equation 3.

$$D_{max} = \frac{t_{RT/CT(chg)}}{t_{RT/CT(chg)} + t_{RT/CT(dischg)}} \qquad \text{(eq. 3)}$$

Substituting Equations 1 and 2 into Equation 3, and after algebraic simplification, we obtain

$$D_{max} = \frac{\ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}}\right)}{\ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}} \cdot \frac{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(valley)} - V_{ref}}\right)} \qquad \text{(eq. 4)}$$

Clearly, the maximum duty ratio is determined by the timing resistor R_T. Therefore, R_T is chosen such as to achieve a desired maximum duty ratio. Once R_T has been selected, C_T can now be chosen to obtain the desired switching frequency as per Equation 5.

$$f = \frac{1}{R_T C_T \ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}} \cdot \frac{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(valley)} - V_{ref}}\right)} \qquad \text{(eq. 5)}$$

Figure 2 shows the frequency and maximum duty ratio variation versus R_T for given values of C_T. Care should be taken to ensure that the absolute minimum value of R_T should not be less than 542 Ω. However, considering a 10% tolerance for the timing resistor, the nearest available standard resistor of 680 Ω is the absolute minimum that can be used to guarantee normal oscillator operation. If a timing resistor smaller than this value is used, then the charging current through the R_T, C_T path will exceed the pulldown (discharge) current and the oscillator will get permanently locked/latched to an undefined state.

In many noise-sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 22. For reliable synchronization, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi-unit synchronization is shown in Figure 23. By tailoring the clock waveform, accurate Output duty ratio clamping can be achieved.

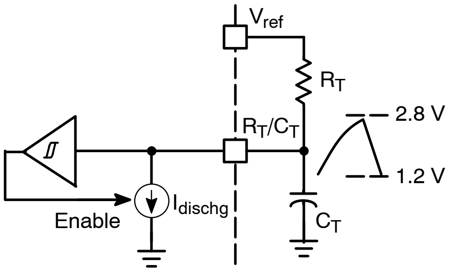


Figure 18. Oscillator Configuration

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 8). The non−inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is −2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 33). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non−inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft−start interval (Figures 25, 26). The Error Amp minimum feedback resistance is limited by the amplifier’s source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator’s 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842B, UC3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle−by−cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground−referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

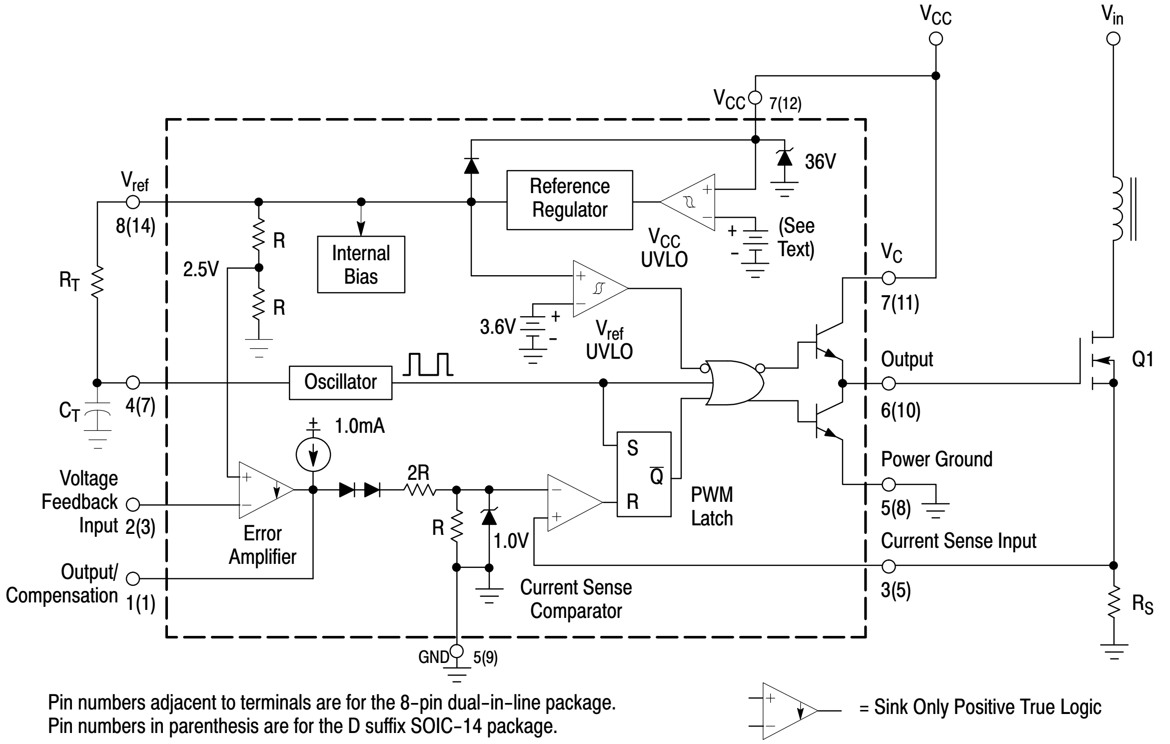
$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 24. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 28).



Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SOIC-14 package.

Figure 19. Representative Block Diagram

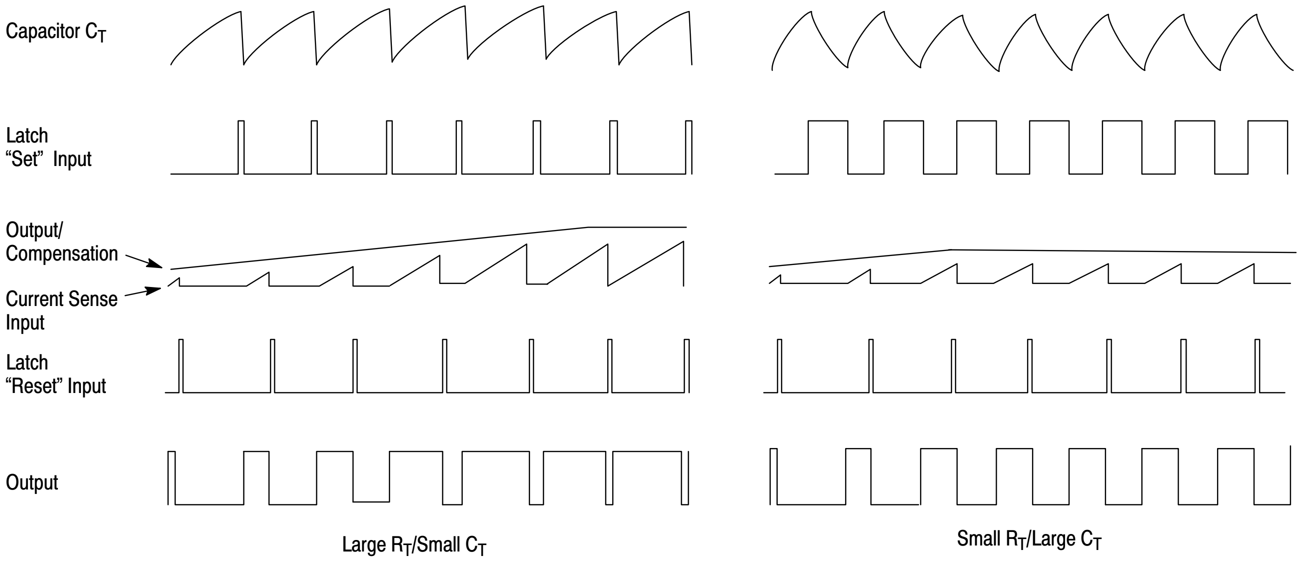


Figure 20. Timing Diagram

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built−in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842B, and 8.4 V/7.6 V for the UCX843B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX842B makes it ideally suited in off−line converter applications where efficient bootstrap startup techniques are required (Figure 35). The UCX843B is intended for lower voltage DC−to−DC converter applications. A 36 V Zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage (V_{CC}) for the UCX842B is 11 V and 8.2 V for the UCX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull−down resistor.

The SOIC−14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A Zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 27 shows proper power and control ground connections in a current−sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at $T_J = 25°C$ on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short−circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire−wrap or plug−in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse−width jitter. This is usually caused by excessive noise pick−up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low−current signal and high−current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise−generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 21A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn−on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)\,(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn−on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 21B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 34).

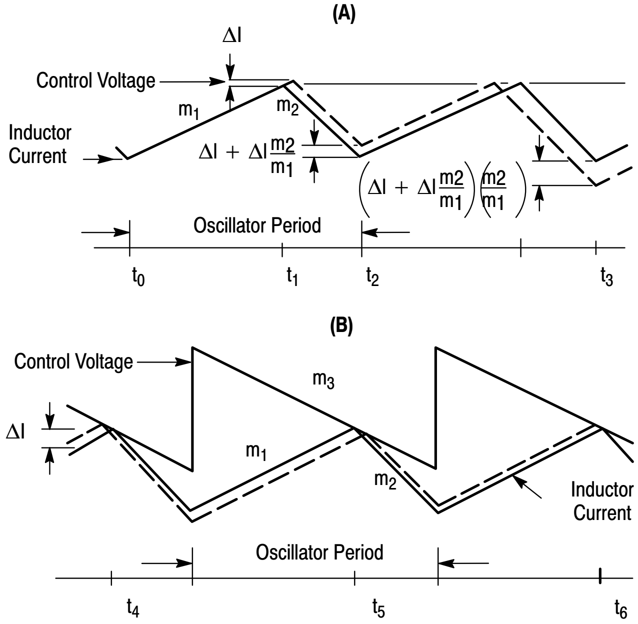
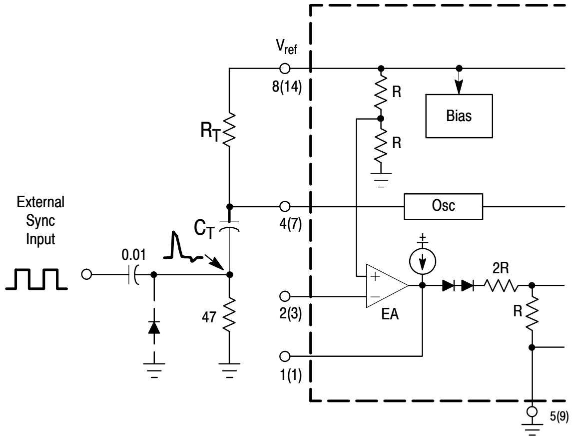
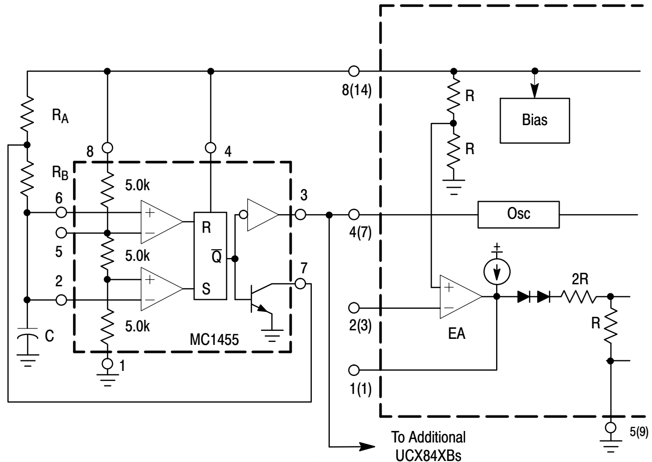


Figure 21. Continuous Current Waveforms



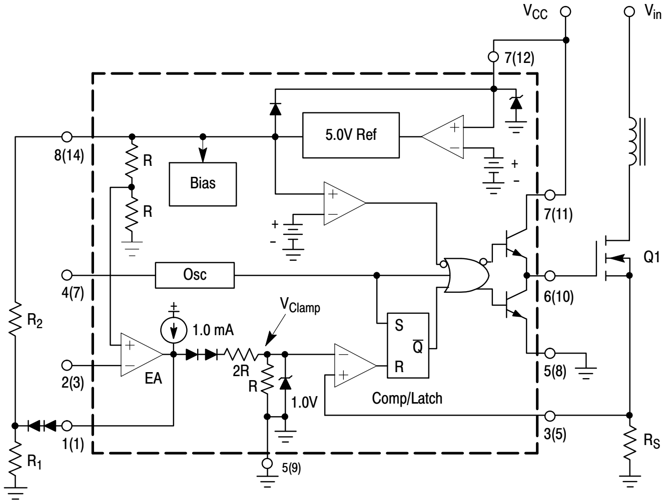
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 22. External Clock Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{(max)} = \frac{R_B}{R_A + 2R_B}$$

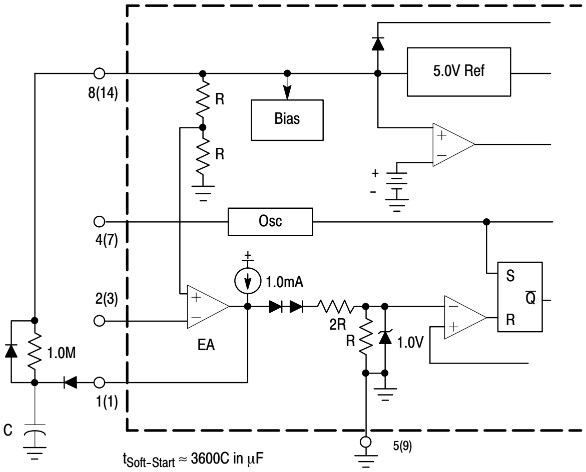
Figure 23. External Duty Cycle Clamp and Multi−Unit Synchronization



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33\text{x}10^{-3}\left(\frac{R_1R_2}{R_1 + R_2}\right) \qquad \text{Where: } 0 \le V_{Clamp} \le 1.0\text{ V}$$

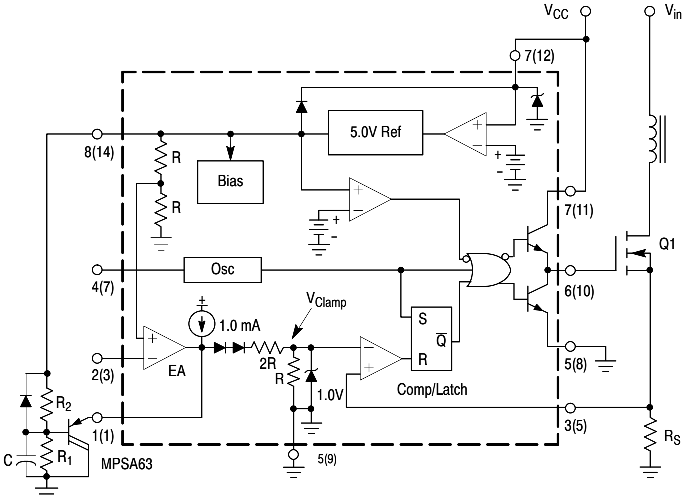
$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 24. Adjustable Reduction of Clamp Level



$t_{Soft\text{-}Start} \approx 3600C$ in μF

Figure 25. Soft−Start Circuit



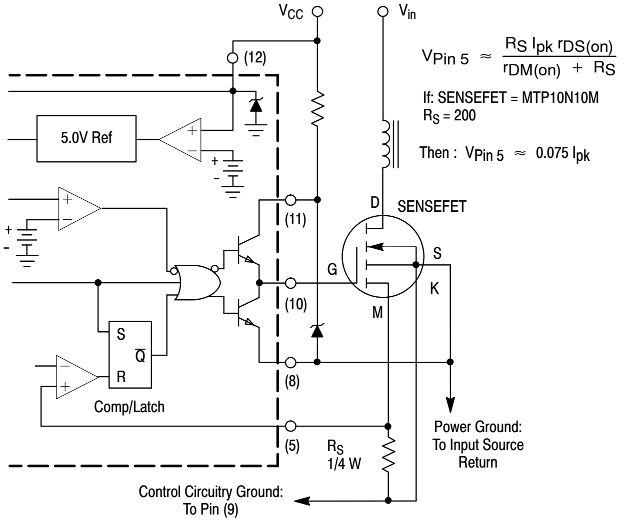
$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)}$$

Where: $0 \le V_{Clamp} \le 1.0$ V

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3\,V_{Clamp}}\right] C \frac{R1\,R2}{R_1 + R_2}$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 26. Adjustable Buffered Reduction of Clamp Level with Soft−Start



$$V_{Pin\,5} \approx \frac{R_S\,I_{pk}\,r_{DS(on)}}{r_{DM(on)} + R_S}$$

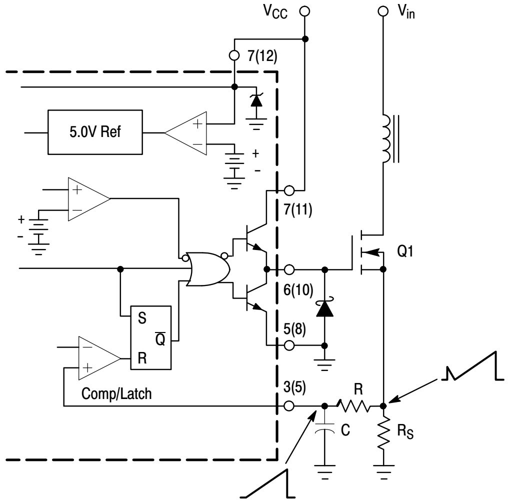
If: SENSEFET = MTP10N10M

$R_S = 200$

Then : $V_{Pin\,5} \approx 0.075\,I_{pk}$

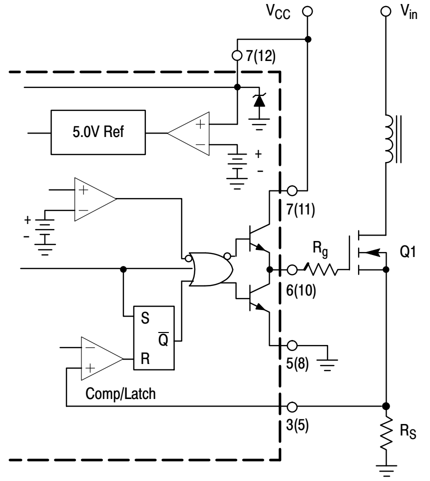
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over-current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 24 and 26.

Figure 27. Current Sensing Power MOSFET



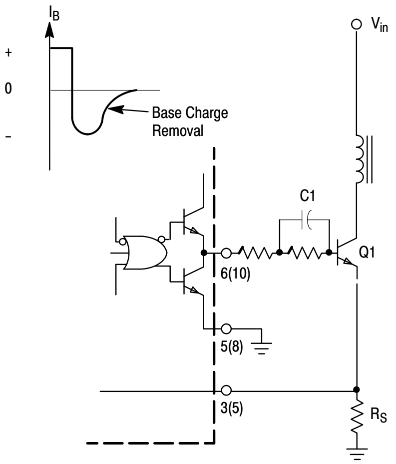
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 28. Current Waveform Spike Suppression



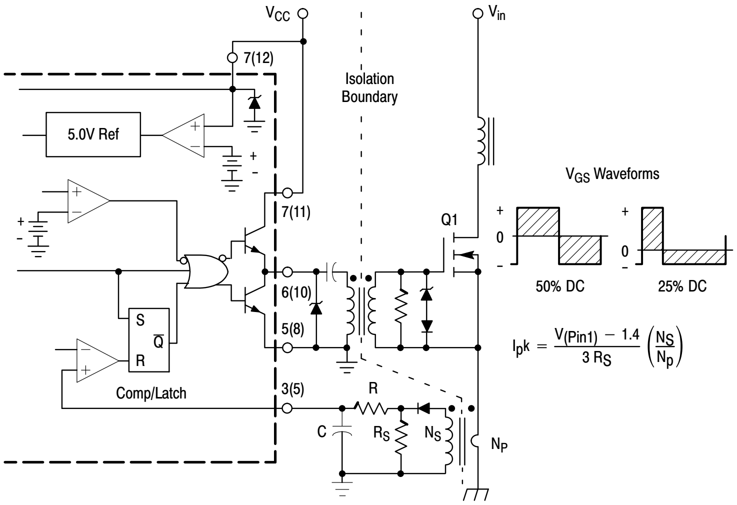
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 29. MOSFET Parasitic Oscillations



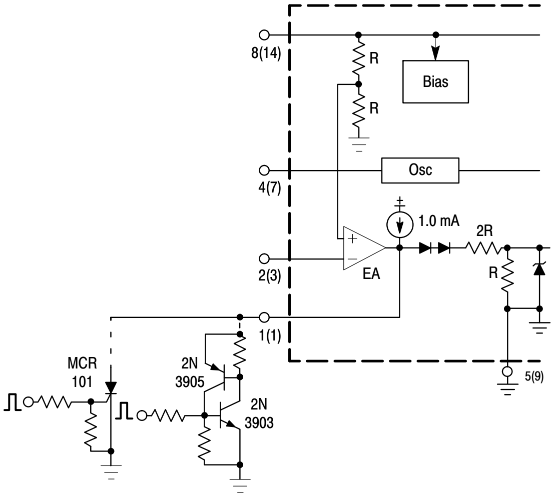
The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 30. Bipolar Transistor Drive



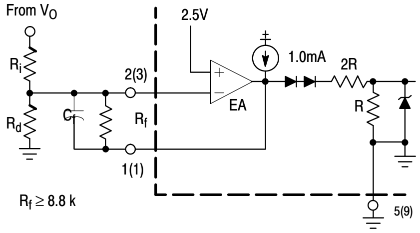
$$I_{pk} = \frac{V_{(Pin1)} - 1.4}{3\,R_S}\left(\frac{N_S}{N_p}\right)$$

Figure 31. Isolated MOSFET Drive

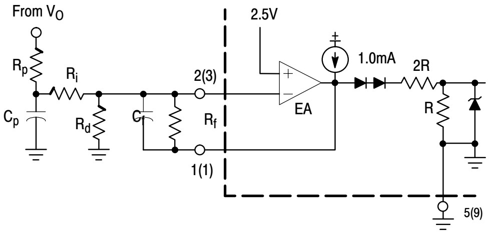


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 32. Latched Shutdown

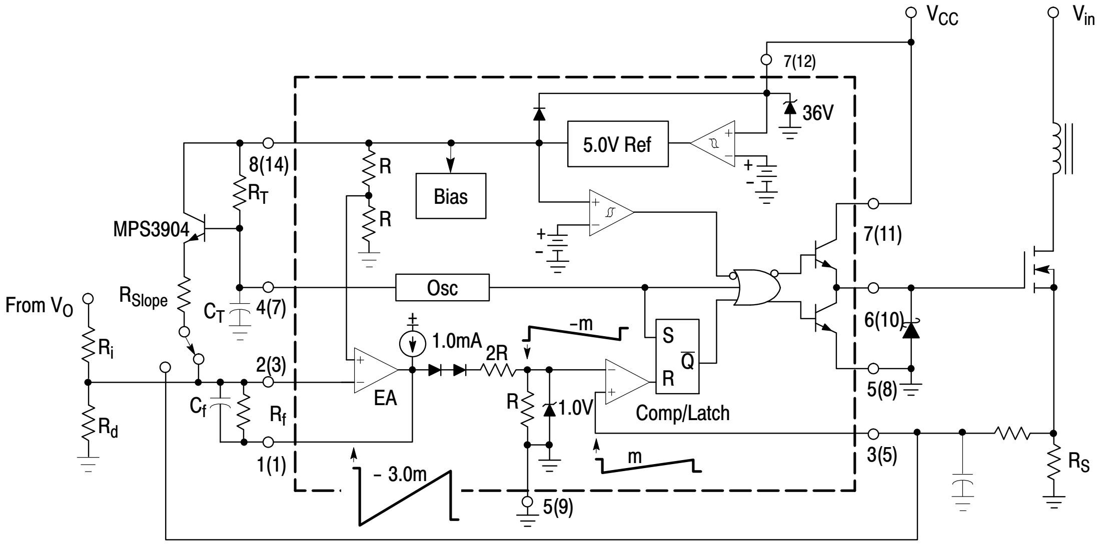


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



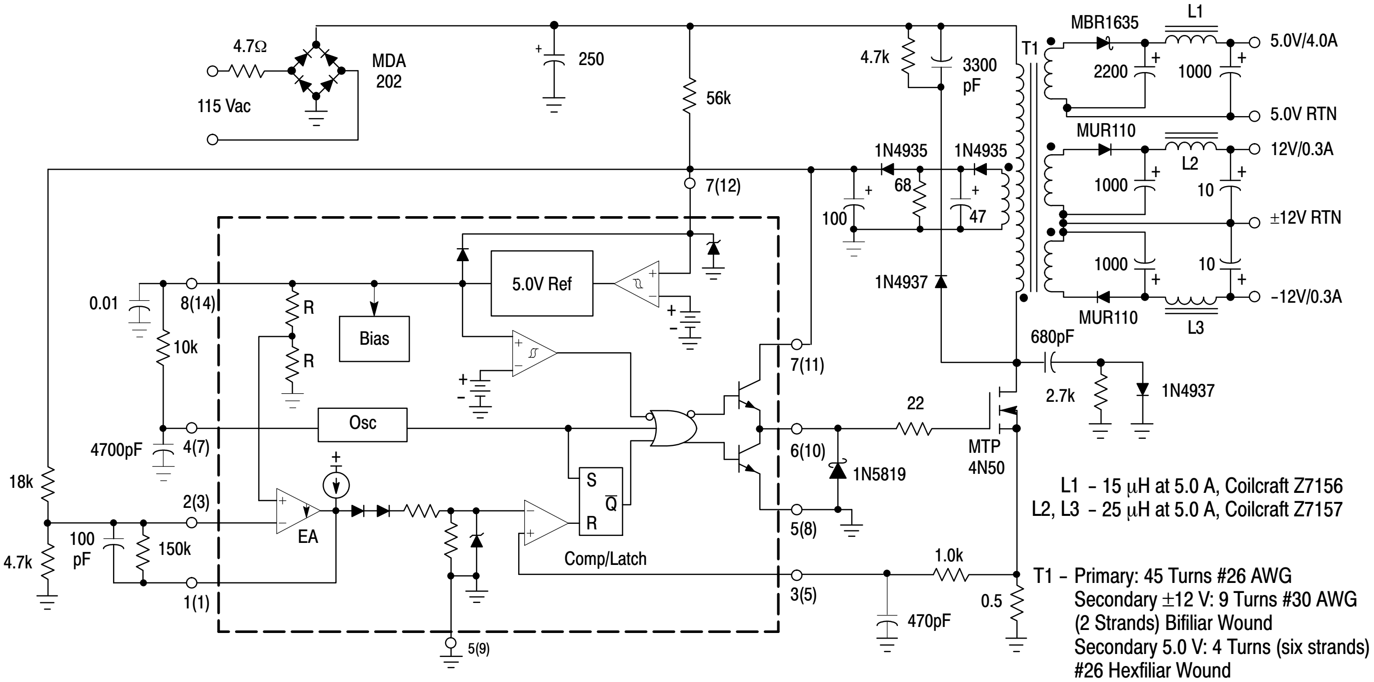
Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 33. Error Amplifier Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 34. Slope Compensation



L1 - 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 - 25 μH at 5.0 A, Coilcraft Z7157

T1 - Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG
(2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns
#30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance
of 1.0 mH

Figure 35. 27 W Off−Line Flyback Regulator

Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation: 5.0 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A	Δ = 300 mV or ± 3.0%
±12 V	V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
UC2842BDG	T_A = −25° to +85°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC2842BD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC2842BD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC2842BNG		PDIP−8 (Pb−Free)	1000 Units/Rail
UC3842BNG	T_A = 0° to +70°C	PDIP−8 (Pb−Free)	1000 Units/Rail
UC3842BDG		SOIC−14 (Pb−Free)	55 Units/Rail
UC3842BDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC3842BD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC3842BD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC3842BVDR2G	T_A = −40° to +105°C	SOIC−14 (Pb−Free)	2500 Tape & Reel
UC3842BVD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC3842BVD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC2843BDG	T_A = −25° to +85°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC2843BDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC2843BD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC2843BD1R2G	T_A = −25° to +85°C	SOIC−8 (Pb−Free)	2500 Tape & Reel
UC2843BNG		PDIP−8 (Pb−Free)	1000 Units/Rail
UC2843DD1R2G	T_A = −40° to +85°C	SOIC−8 (Pb−Free)	2500 Tape & Reel
UC2843DDR2G		SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

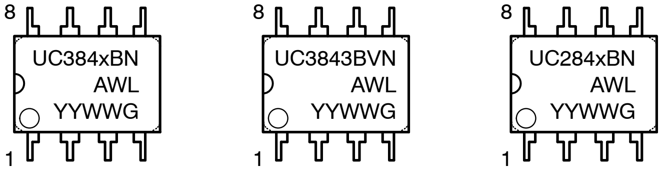
ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
UC3843BDG	T_A = 0° to +70°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC3843BDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC3843BD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC3843BD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC3843BDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC3843BNG		PDIP−8 (Pb−Free)	1000 Units/Rail
UC3843BVDG	T_A = −40° to +105°C	SOIC−14 (Pb−Free)	55 Units/Rail
UC3843BVDR2G		SOIC−14 (Pb−Free)	2500 Tape & Reel
UC3843BVD1G		SOIC−8 (Pb−Free)	98 Units/Rail
UC3843BVD1R2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
UC3843BVNG		PDIP−8 (Pb−Free)	1000 Units/Rail

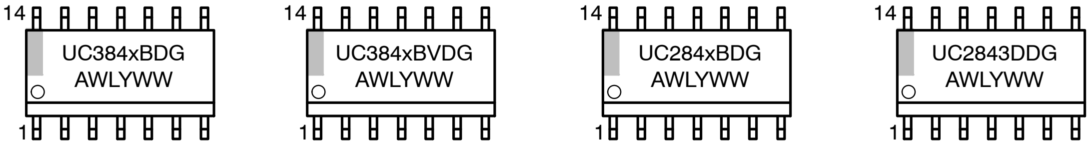
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

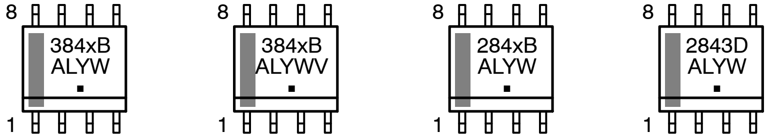
PDIP−8
N SUFFIX
CASE 626



SOIC−14
D SUFFIX
CASE 751A



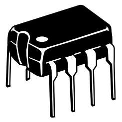
SOIC−8
D1 SUFFIX
CASE 751



x = 2 or 3
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

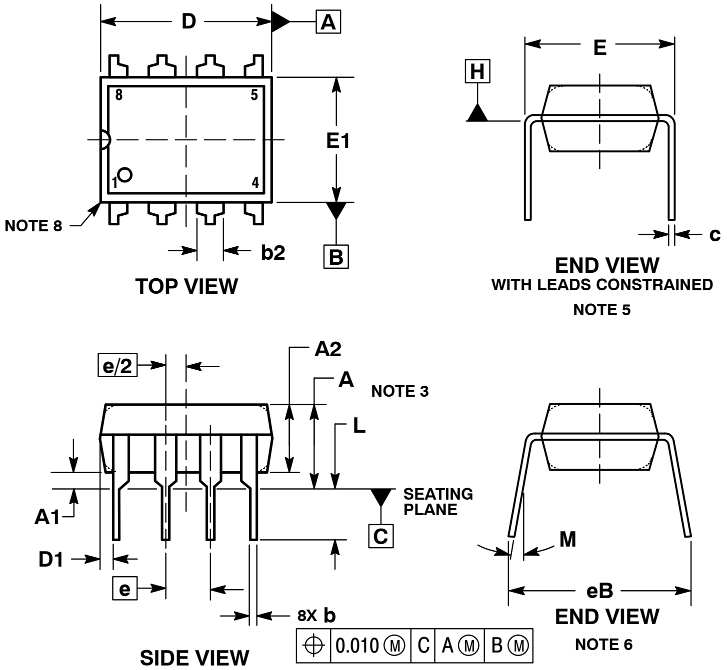
ON Semiconductor®



SCALE 1:1

PDIP−8
CASE 626−05
ISSUE P

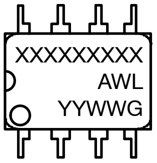
DATE 22 APR 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	−−−−	0.210	−−−	5.33
A1	0.015	−−−−	0.38	−−−
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	−−−−	0.13	−−−
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	−−−−	0.430	−−−	10.92
L	0.115	0.150	2.92	3.81
M	−−−−	10°	−−−	10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**PDIP−8**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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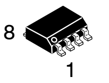
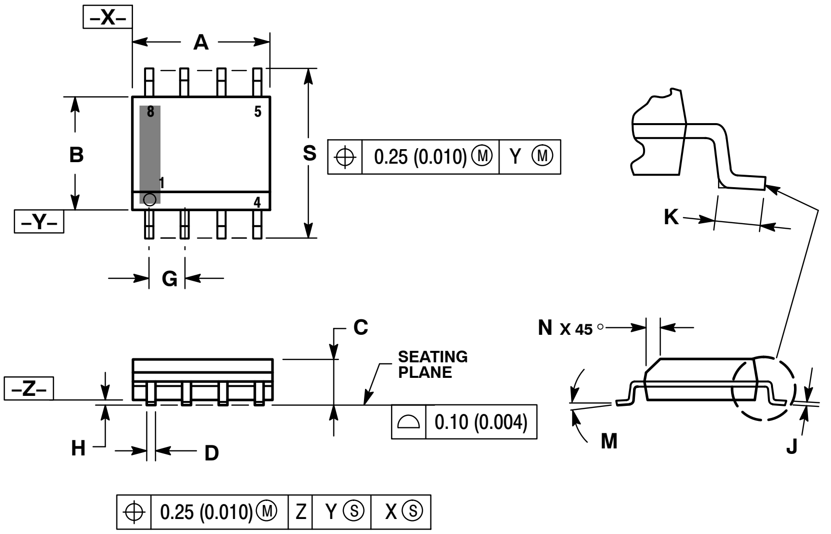


SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

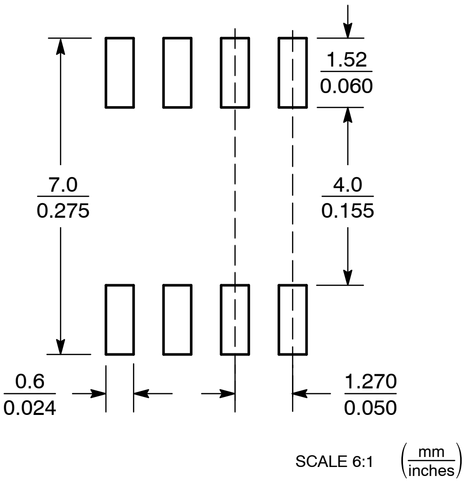
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

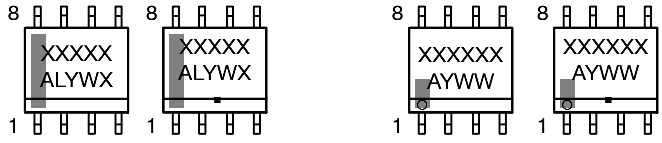
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)** **Discrete** **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

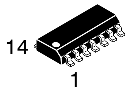
STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

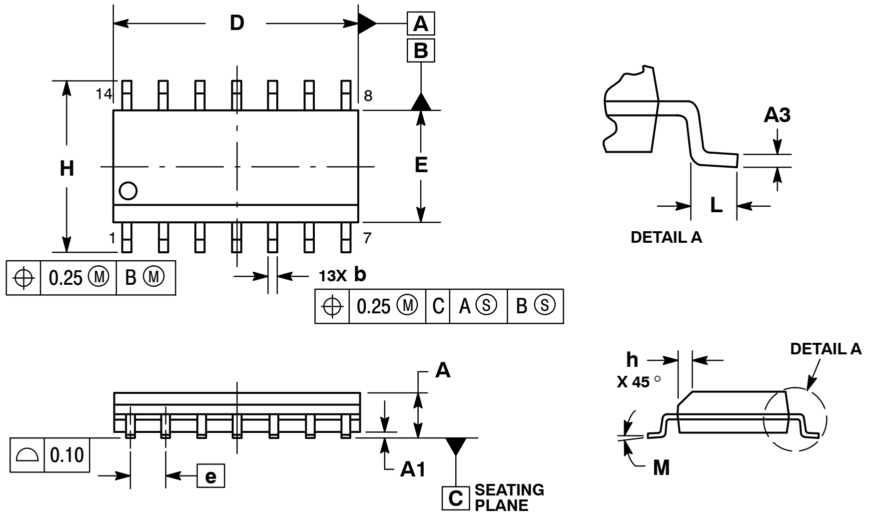
ON Semiconductor®



SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

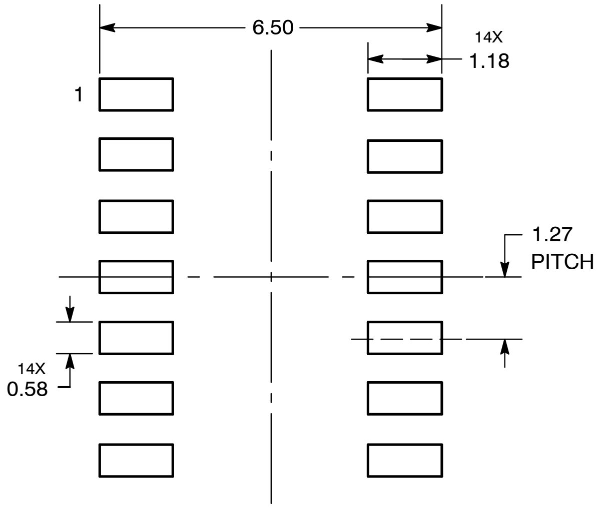
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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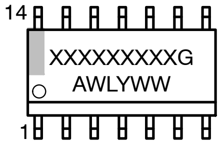
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**	**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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DESCRIPTION:	**SOIC−14 NB**	**PAGE 2 OF 2**

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