1 Pin description

Figure 1. **Pin connection (top view)**

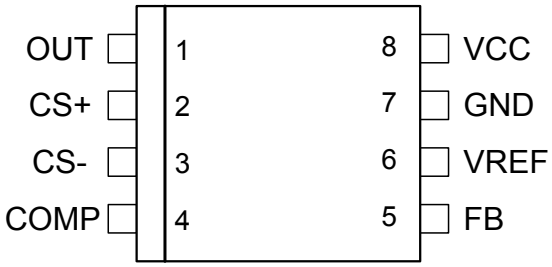


Table 1. **Pin description**

Pin n°	Name	Description
1	OUT	Regulator output.
2	CS+	Current error amplifier input (current sense at higher voltage)
3	CS-	Current error amplifier input (current sense at lower voltage)
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23 V. An extenal resistive divider is required for higher output voltages.
6	VREF	3.3 V reference voltage. No cap is need for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

2 Absolute maximum ratings

Stressing the device above the rating listed in the table below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_8	Input voltage	-0.3	40	V
V_1	OUT pin DC voltage	-1	40	V
	OUT pin peak voltage at Δt = 0.1 µs	-5	40	
I_1	Maximum output current	int. limit.		
V_4, V_5	Analog pins	-0.3	4	V
V_2, V_3	Analog pins	-0.3	V_{CC}	V
P_{TOT}	Power dissipation at $T_A \leq 70$ °C		0.7	W
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-55	150	°C

Table 3. Thermal data

Symbol	Parameter	SO-8	Unit
R_{thJA}	Thermal resistance junction to ambient (device soldered on a standard demonstration board)	110	°C/W

3 Electrical characteristics

T_J = -40 to 125 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating input voltage range	V_0 = 1.235 V; I_0 = 2 A	8		36	V
$R_{DS(on)}$	MOSFET on resistance			0.250	0.5	Ω
I_L	Maximum limiting current	V_{CC} = 8.5 V (1)	1.8	2.5	3.2	A
		V_{CC} = 8.5 V, T_J = 25 °C	2	2.5	3.2	
f_{SW}	Switching frequency		212	250	280	kHz
	Duty cycle		0		100	%
Dynamic characteristics (see test circuit)						
V5	Voltage feedback	8 V < V_{CC} < 36 V; 20 mA < I_0 < 1 A	1.198	1.235	1.272	V
η	Efficiency	V_0 = 5 V, V_{CC} = 12 V		90		%
DC characteristics						
I_{qop}	Total operating quiescent current			3	5	mA
I_q	Quiescent current	Duty cycle = 0; V_{FB} = 1.5 V			2.7	mA
Error amplifier						
V_{OH}	High level output voltage	V_{FB} = 1 V	3.6			V
V_{OL}	Low level output voltage	V_{FB} = 1.5 V			0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9 V; V_{FB} = 1 V	160	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9 V; V_{FB} = 1.5 V	1	1.5		mA
I_b	Source bias current			2.5	4	µA
	DC open loop gain	R_L = ∞	50	58		dB
gm	Transconductance	I_{COMP} = -0.1 mA to 0.1 mA; V_{COMP} = 1.9 V		2.3		mS
V_{OFFS}	Input offset voltage	V_{CS-} = 1.8 V; V_{CS+} = V_{comp}	90	100	110	mV
I_{CS+}	CS+ output current	I_0 =1 A; R_{SENSE}= 100 mΩ; V_{OUT} < V_{CC} - 2 V		1.5	3	µA
I_{CS-}	CS- output current	I_0 = 1 A; R_{SENSE} = 100 mΩ; V_{OUT} < V_{CC} - 2 V		1.5	3	µA
Reference section						
	Reference voltage	I_{REF} = 0 to 5 mA; V_{CC} = 8 V to 36 V	3.2	3.3	3.399	V
	Line regulation	I_{REF} = 0 mA; V_{CC} = 8 V to 36 V		5	10	mV
	Load regulation	I_{REF} = 0 to 5 mA		8	15	mV
	Short circuit current		5	18	35	mA

1. *With T_J = 85 °C, I_{lim_min} = 2 A, assured by design, characterization and statistical correlation.*

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C; +25 °C, +125 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C; +125 °C).

The device operation is so guaranteed when the junction temperature is inside the (-40 °C; +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation (please refer to the Section 8.4 Thermal considerations).

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+150 °C ± 10 °C) temperature.

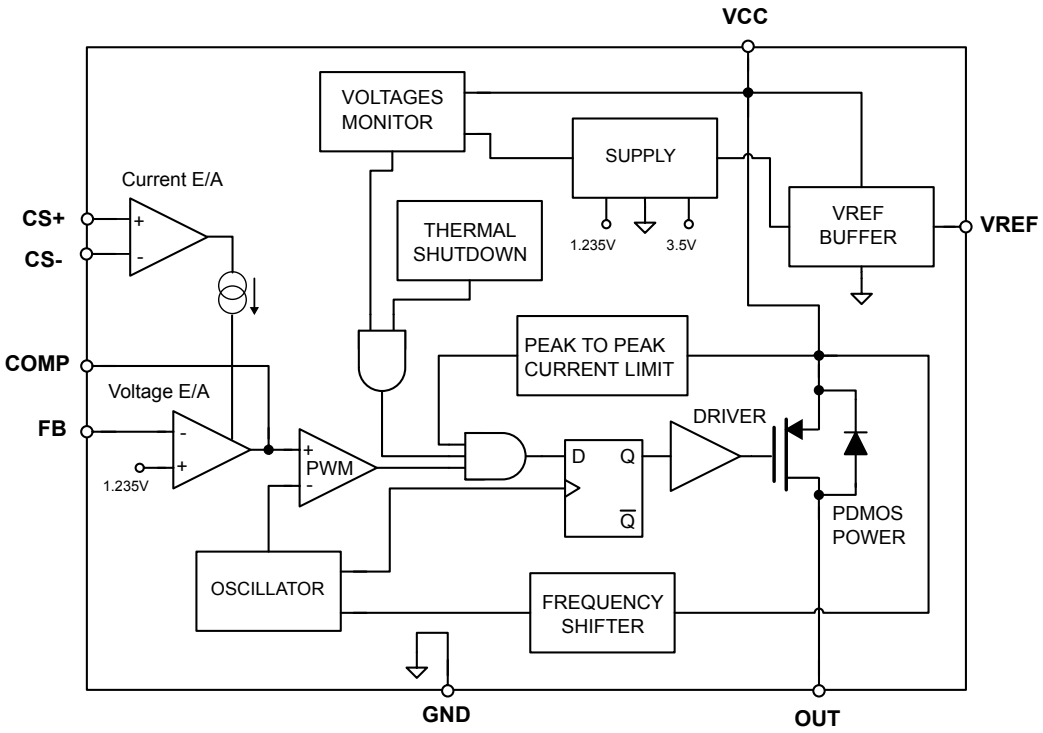
All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

5 Functional description

The main internal blocks are shown in the device block diagram in figure below.

- A voltage regulator supplying the internal circuitry.
- A voltage monitor circuit checks the input and the internal voltages.
- A fully integrated sawtooth oscillator with a frequency of 250 kHz ± 15 %, including also the voltage feed forward function.
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle.
- A transconductance error amplifier for output voltage regulation.
- A transconductance error amplifier for adjustable constant current operation.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high side driver for the internal P-MOS switch.
- An inhibit block for stand-by operation.
- A circuit to implement the thermal protection function.

Figure 2. Block diagram



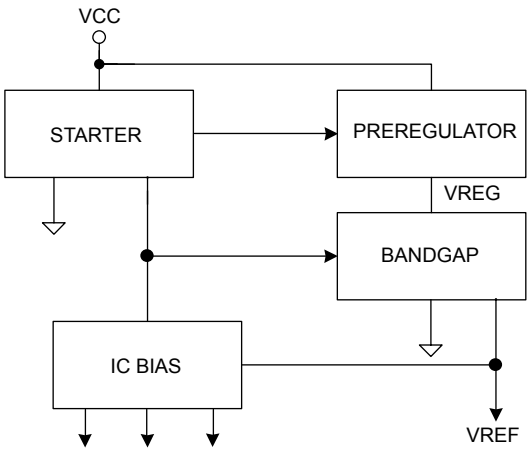
5.1 Power supply and voltage reference

The internal regulator circuit (shown in Figure 3. Internal circuit) consists of a start-up circuit, an internal voltage pre-regulator, the Bandgap voltage reference and the Bias block that provides current to all the blocks. The pre-regulator block supplies the Bandgap cell with a pre-regulated voltage VREG that has a very low supply voltage noise sensitivity.

5.2 Voltage monitors

An internal block continuously senses the VCC, VREF and VBG. If the voltages go higher than their thresholds, the regulator begins operating. There is also an hysteresis on the VCC (UVLO).

Figure 3. Internal circuit

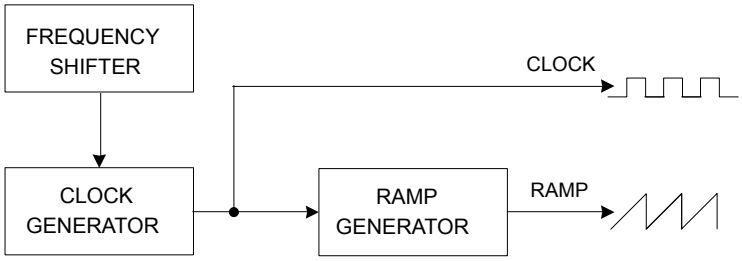


5.3 Oscillator

Figure below shows the block diagram of the oscillator circuit. The clock generator provides the switching frequency of the device, which is internally fixed at 250 kHz. The frequency shifter block acts to reduce the switching frequency in case of strong overcurrent or short circuit. The clock signal is then used in the internal logic circuitry and is the input of the ramp generator.

The ramp generator circuit provides the sawtooth signal, used for PWM control and the internal voltage feed-forward.

Figure 4. Oscillator circuit block diagram



5.4 Current protection

The A6902D features different current protections:

- An inner current loop, composed by the transconductance current error amplifier and the sensing resistor, that implements a precise switching current source regulating an adjustable real average current. This operation regulates 100 mV across the sensing resistor and it requires a small signal stability analysis to design the system bandwidth / phase margin (see Section 7 Closing the loop). The maximum bandwidth is f_{SW} / 5 = 50 kHz for a valid small analysis so the minimum time to react to an external load transient is about five switching cycles.
- A second level “pulse by pulse” current protection, sensing the current flowing in the embedded power element. This protection is faster than the previous as it can disable the power element with negligible delay when the over current comparator is triggered during the power element conduction time. However, due to the noise created by the switching activity of the power MOSFETs, the current sense is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is

generally known as “masking time” or “blanking time” (270 ns typ.). The current threshold of the over-current comparator is given in Table 4. Electrical characteristics.

Both of the protections implement a constant current strategy as the device limits the output current.

The Constant Current Loop, called CCL (see Section 7.2.2 Constant current loop), is adjustable and precise but slower than the embedded Over Current Protection called “OCP” (see Section 6.2 OCP protection), which is very fast but with fixed and spreaded current threshold over the population.

The OCP protects the device and external load in case of fast and unexpected line / load transient like a short circuit event.

5.5 Error amplifiers

The current outputs of the two internal error amplifiers are ORed and compared to the oscillator saw tooth to perform PWM control (voltage mode structure). A compensation network valid for both voltage and current loop is shared in the COMP pin to achieve adequate phase margin.

5.5.1 Voltage loop

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235 V) and the inverting input (FB) is connected to the external divider or directly to the output voltage. The uncompensated error amplifier has the following characteristics:

Table 5. Uncompensated voltage error amplifier characteristics

Description	Value
Transconductance	2300 µS
Low frequency gain	70 dB
Minimum sink/source current	1500 µA / 300 µA
Output voltage swing	0.4 V / 3.65 V
Input bias current	2.5 µA

5.5.2 Constant current loop

The current error amplifier is a transconductance operational amplifier with a typical offset equal to 100 mV which directly senses the voltage across the sensing resistor. The uncompensated current error amplifier has the following characteristics.

Table 6. Uncompensated voltage error amplifier characteristics

Description	Value
Transconductance	1900 µS
Low frequency gain	60 dB
Minimum sink/source current	1500 µA / 300 µA
Output voltage swing	0.4 V / 3.65 V

5.6 PWM comparator and power stage

This block compares the oscillator saw tooth and the error amplifier output signals to generate the PWM signal for the driving stage.

The power stage is a highly critical block, as it functions to guarantee a correct turn ON and turn OFF of the PDMOS. The turn ON of the power element, or more accurately, the rise time of the current at turn ON, is a very critical parameter. At a first approach, it appears that the faster the rise time, the lower the turn ON losses.

However, there is a limit introduced by the recovery time of the recirculation diode.

In fact, when the current of the power element is equal to the inductor current, the diode turns OFF and the drain of the PDMOS is able to go high. But during its recovery time, the diode can be considered a high value capacitor and this produces a very high peak current, responsible for numerous problems:

- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasites.
- Turn ON overcurrent leads to a decrease in the efficiency and system reliability.
- Major EMI problems.
- Shorter freewheeling diode life.

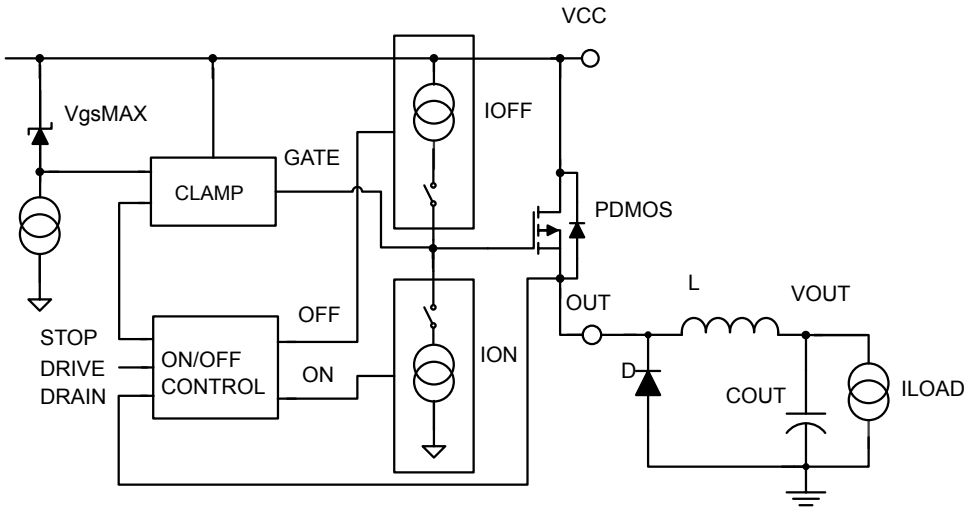
The fall time of the current during turn OFF is also critical, as it produces voltage spikes (due to the parasites elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize these problems, a new driving circuit topology has been used and the block diagram is shown in figure below. The basic idea is to change the current levels used to turn the power switch ON and OFF, based on the PDMOS and the gate clamp status.

This circuitry allows the power switch to be turned OFF and ON quickly and addresses the freewheeling diode recovery time problem. The gate clamp is necessary to ensure that VGS of the internal switch does not go higher than VGSmax.

The ON/OFF Control block protects against any cross conduction between the supply line and ground.

Figure 5. Driving circuitry



5.7 Thermal shutdown

The shutdown block generates a signal that turns OFF the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 ± 10 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C keeps the device from turning ON and OFF continuously.

6 Additional features and protection

6.1 Feedback disconnection

If the feedback is disconnected, the duty cycle increases towards the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this hazardous condition, the device is turned OFF if the feedback pin is left floating.

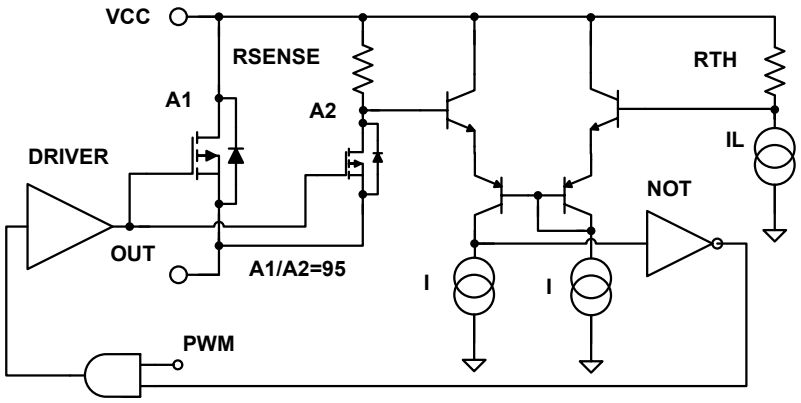
6.2 OCP protection

The OCP features two types of current limit protections: pulse-by-pulse and frequency foldback.

The schematic of the current limitation circuitry for the pulse-by-pulse protection is shown in figure below.

The output power PDMOS transistor is split into two parallel PDMOS transistors. The smallest one includes a resistor in series, RSENSE. The current is sensed through RSENSE and if it reaches the threshold, the mirror becomes unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse. Due to this reduction of the ON time, the output voltage decreases. The frequency shifter function is enabled by the overcurrent event and it skips up to three switching pulses depending on the feedback voltage. In strong overcurrent conditions the device can reduce the switching frequency down to 1/3 of the nominal 250 kHz to keep the switch current limited.

Figure 6. Current limit circuitry



In overcurrent protection mode, when the peak current reaches the current limit, the device reduces the TON down to its minimum value (approximately 250 ns) and the switching frequency to approximately one third of its nominal value even when synchronized to an external signal. In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to ILIM. In any event, in case of heavy shortcircuit at the output (VOUT = 0 V) and depending on the application conditions (Vcc value and parasitic effect of external components) the current peak could reach values higher than ILIM. This can be understood considering the inductor current ripple during the ON and OFF phases:

- ON phase

$$\Delta I_{L,TON} = \frac{V_{IN} - V_{OUT} - (DCR_L + R_{DSON}) \cdot I_L}{L} \cdot T_{ON} \quad (1)$$

- OFF phase

$$\Delta I_{L,TOFF} = \frac{V_D + V_{OUT} - DCR_L \cdot I_L}{L} \cdot T_{OFF} \quad (2)$$

where V_D is the voltage drop across the diode, DCR_L is the series resistance of the Inductor. In short-circuit conditions V_{OUT} is negligible so during T_{OFF} the voltage across the inductor is very small as equal to the voltage drop across parasitic components (typically the DCR of the inductor and the forward voltage of the freewheeling diode) while during TON the voltage applied to the inductor is maximized as approximately equal to V_{IN}.

In case a short circuit at the output is applied and VIN = 12 V the inductor current is controlled in most of the applications. When the application must sustain the short-circuit condition for an extended period, the external components (mainly the inductor and diode) must be selected based on this value.

In case the VIN is very high, it could occur that the ripple current during T_{OFF} (Eq. (2)) does not compensate the current increase during T_{ON} (Eq. (1)). In this case $\Delta IL_{TON} > \Delta IL_{TOFF}$ so the current escalates and the balance between Eq. (1) and Eq. (2) occurs at a current slightly higher than the current limit.

This must be taken into account in particular to avoid the risk of an abrupt inductor saturation.

6.3 Output overvoltage protection

Overvoltage protection, or OVP, is achieved by using an internal comparator connected to the feedback, which turns OFF the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

6.4 Zero load operation

Due to the fact that the internal power is a PDMOS, no bootstrap capacitor is required and so the device works properly even with no load at the output. In this case it works in burst mode, with a random burst repetition rate.

7 Closing the loop

7.1 Error amplifier and compensation network

The output L-C filter of a step-down converter contributes with 180 degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added.

The simplest compensation network together with the equivalent circuit of the error amplifier are shown in figure below. R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise of the COMP pin.

The transfer function of the error amplifier and its compensation network is:

$$A_0(s) = A_{V0} \cdot \frac{(1 + s \cdot R_C \cdot C_C)}{s^2 \cdot R_0 \cdot (C_0 + C_P) \cdot R_C \cdot C_C + s \cdot (R_0 \cdot C_C + R_0 \cdot (C_0 + C_P) + R_C \cdot C_C) + 1} \quad (3)$$

Where

$$A_{V0} = G_m \cdot R_0 \quad (4)$$

Figure 7. Error amplifier and compensation network

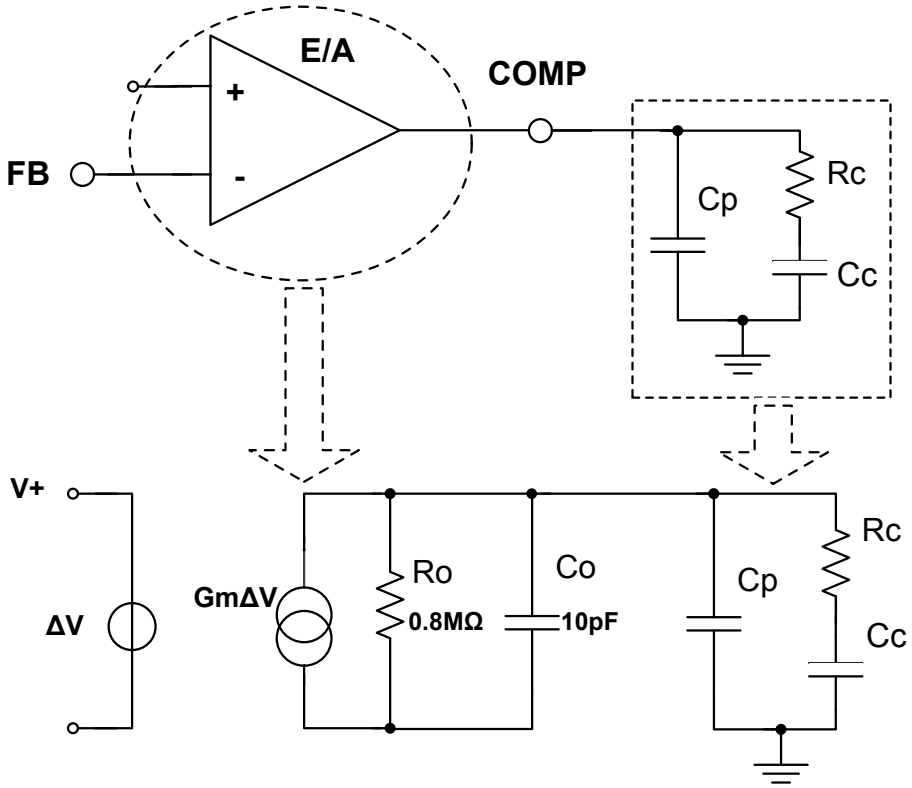


Figure 8. **Voltage loop block diagram**

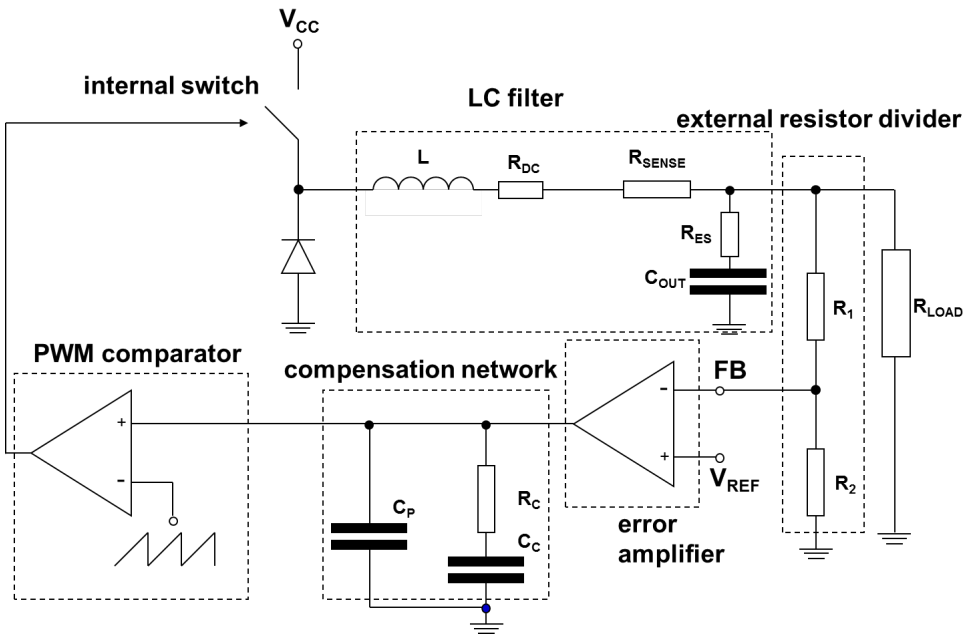
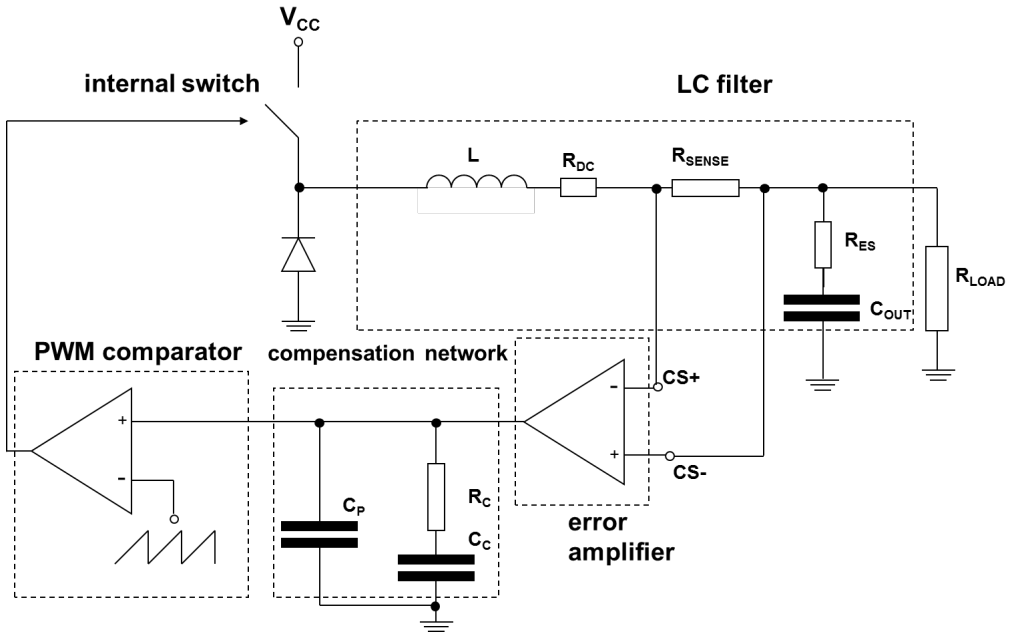


Figure 9. **Constant current loop block diagramConstant current loop block diagram**



The poles of this transfer function are (assuming Cc >> C_0 + C_P):

(5)

$$F_{P1} = \frac{1}{2\pi R_0 C_C}$$

(6)

$$F_{P2} = \frac{1}{2\pi R_C (C_0 + C_P)}$$

whereas the zero is defined as:

(7)

$$F_{Z1} = \frac{1}{2\pi R_C C_C}$$

F_{P1} is the low frequency pole which sets the bandwidth, while the zero F_{Z1} is usually put near to the frequency of the double pole of the L-C filter (see below). F_{P2} is usually at a very high frequency.

7.2 LC filter

The L-C filter has different contributions depending on the active loop so the design of the compensation network must guarantee a proper bandwidth / phase margin for both operations.

7.2.1 Voltage loop

The transfer function of the power stage is given by:

(8)

$$G_{PWR\_VM}(s) = \frac{\frac{1}{\frac{1}{R_{LOAD}} + \frac{1}{R_{ES} + \frac{1}{s \cdot C_{OUT}}}}}{s \cdot L_{IND} + R_{DC} + R_{SENSE} + \frac{1}{\frac{1}{R_{LOAD}} + \frac{1}{R_{ES} + \frac{1}{s \cdot C_{OUT}}}}} \cdot \frac{R_1}{R_1 + R_2}$$

R_1, R_2 represents the output voltage divider.

The previous equation can be rewritten and simplified, assuming R_{ES} and R_{DC} negligible compared to R_{LOAD}:

(9)

$$G_{PWR\_VM}(s) = G_{LC0} \frac{1 + \frac{s}{2\pi \cdot F_{Z\_ESR\_VM}}}{1 + \frac{s}{2\pi \cdot Q \cdot F_{LC}} + \left(\frac{s}{2\pi \cdot F_{LC}}\right)^2} \cdot \frac{R_1}{R_1 + R_2}$$

$$G_{LC0} = \frac{R_{LOAD}}{R_{LOAD} + R_{DC} + R_{SENSE}} \cong 1$$

$$F_{Z\_ESR\_VM} = \frac{1}{2\pi R_{ES} C_{OUT}}$$

$$F_{P\_LC} = \frac{1}{2\pi\sqrt{L_{IND} \cdot C_{OUT}} \cdot \sqrt{\frac{R_{LOAD} + R_{ES}}{R_{LOAD} + R_{DC} + R_{SENSE}}}} \approx \frac{1}{2\pi\sqrt{L_{IND} \cdot C_{OUT}}}$$

$$Q \approx \frac{\sqrt{L_{IND} \cdot C_{OUT}}}{\frac{L_{IND}}{R_{LOAD}} + C_{OUT} \cdot R_{SENSE}}$$

The singularity introduced by the ESR of the output capacitor, $F_{Z\_ESR\_VM}$, is essential to increase the phase margin of the loop.

7.2.2 Constant current loop

The transfer function of the output filter is given by:

(10)

$$G_{PWR\_CM}(s) = \frac{R_{SENSE}}{s \cdot L_{IND} + R_{DC} + R_{SENSE} + \frac{1}{\frac{1}{R_{LOAD}} + \frac{1}{R_{ES} + \frac{1}{s \cdot C_{OUT}}}}}$$

The previous equation can be rewritten and simplified, assuming R_{ES} and R_{DC} negligible compared to R_{LOAD}:

$$G_{PWR\_CM}(s) = \frac{1 + \frac{s}{2\pi \cdot F_{Z\_ESR\_CM}}}{1 + \frac{s}{2\pi \cdot Q \cdot F_{LC}} + \left(\frac{s}{2\pi \cdot F_{LC}}\right)^2} \cdot R_{SENSE}$$

$$F_{Z\_ESR\_CM} = \frac{1}{2\pi C_{OUT} \cdot (R_{LOAD} + R_{ES})} \approx \frac{1}{2\pi C_{OUT} \cdot R_{LOAD}}$$

$$F_{P\_LC} = \frac{1}{2\pi\sqrt{L_{IND} \cdot C_{OUT}} \cdot \sqrt{\frac{R_{LOAD} + R_{ES}}{R_{LOAD} + R_{DC} + R_{SENSE}}}} \approx \frac{1}{2\pi\sqrt{L_{IND} \cdot C_{OUT}}}$$

$$Q \approx \frac{\sqrt{L_{IND} \cdot C_{OUT}}}{\frac{L_{IND}}{R_{LOAD}} + C_{OUT} \cdot R_{SENSE}}$$

As a consequence, the frequency of the zero in current loop operation depends on the loading conditions, whereas the current and voltage power loop transfer functions have the same denominator.

In terms of principle it is possible to compensate the current loop with ceramic capacitor at the output, placing $f_{Z\_ESR\_CM}$ inside the system bandwidth to guarantee enough phase margin for a given loading range.

Negligible ESR means $f_{Z\_ESR\_VM} >> f_{P\_LC}$ and so the voltage loop results stable only in discontinuous conduction mode / no load operation but unstable working in continuous conduction mode.

An application that fits this operation is when the voltage loop implements just an OVP protection for load disconnection or end of charge detection in battery charging application.

7.2.3 PWM comparator

In voltage mode control loop the PWM comparator in Figure 2. Block diagram generates a PWM control signal for the driving circuitry comparing the internal saw tooth waveform and the output of the error amplifier.

The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the switching net (OUT pin) results in an almost constant gain, due to the voltage feed-forward which generates the saw tooth signal with amplitude proportional to the input voltage:

(11)

$$G_{PWM}(s) = \frac{V_{IN}}{\Delta V_{OSC}} = \frac{V_{IN}}{K \cdot V_{IN}} = \frac{1}{0.076}$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, thus ensuring a better line regulation and faster line transient response.

In summary, the open loop gain can be expressed as:

(12)

$$G_{TOT}(s) = \begin{cases} G_{PWM}(s) \cdot G_{PWR\_VM}(s) \cdot A_0(s) \\ G_{PWM}(s) \cdot G_{PWR\_CM}(s) \cdot A_0(s) \end{cases}$$

For constant current or constant voltage operation, respectively.

8 Application information

8.1 Input capacitor selection

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current. For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The input capacitor critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The RMS input current (flowing through the input capacitor) is estimated by:

(13)

$$I_{CIN,RMS} \cong I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The maximum input RMS current is achieved when D = 50%.

Based on above requirements of current rating and low ESR, a typical choice is a ceramic capacitor 50 V rated, in the range of 4.7 to 10 µF.

Alternative solutions, like low ESR aluminum or polymer capacitors, can also fit if the above requirements are satisfied.

High dv/dt voltage spikes on the input side can be critical for DC/DC converters. A good power layout and input voltage filtering help to minimize this issue.

In addition to the above considerations, a 1 µF/50 V ceramic capacitor as close as possible to the VCC and GND pins is always suggested to adequately filter VCC spikes.

The amount of input voltage ripple can be roughly estimated by:

(14)

$$V_{IN,PP} \cong I_{OUT} \cdot \frac{D \cdot (1 - D)}{C_{IN} \cdot F_{SW}} + I_{OUT} \cdot R_{ES}$$

In case of MLCC ceramic input capacitors, the equivalent series resistance (R_{ES}) is almost negligible.

8.2 Output capacitor selection

The output capacitor is very important in order to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system.

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to meet the voltage ripple requirements.

The amount of the voltage ripple can be estimated starting from the current ripple obtained by the inductor selection. Assuming ΔIL the inductor current ripple, the output voltage ripple is roughly estimated by:

(15)

$$\Delta V_{OUT,PP} \cong \Delta I_L \cdot \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}} + \Delta I_L \cdot R_{ES,OUT}$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi-layer ceramic capacitor (MLCC) with very low ESR value.

The output capacitor is important also for loop stability: it fixes the double LC filter pole and, above all, the zero due to its ESR.

This component must be selected considering all the above requirements.

8.3 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor.

The minimum inductance value, in order to have the expected current ripple, must be selected.

The target current ripple value is typically in the range of 20% - 40% of the output current.

In the continuous conduction mode (CCM), the required inductance value can be calculated as follow.

(16)

$$L_{IND} = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_L \cdot F_{SW}}$$

In order to guarantee a maximum current ripple in every condition, Eq. (16) must be evaluated in case of maximum input voltage, assuming VOUT fixed.

Increasing the value of the inductance help to reduce the current ripple but, at the same time, strongly impacts the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from the initial to the final value. Until the inductor has finished its charging (or discharging) time, the output current is supplied (or recovered) by the output capacitors.

Further, if the compensation network is properly designed, during a load variation the device is able to properly change the duty cycle so improving the control loop transient response.

When this condition is reached the response time is only limited by the time required to change the inductor current, basically by VIN, VOUT and L.

Minimizing the response time, at the end, can help to decrease the output filter total cost and to reduce the application area.

8.4 Thermal considerations

$R_{thJ\text{-}A}$ is the equivalent static thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient.

For this device the path through the pin leads is the one conducting the largest amount of heat. The static $R_{th\ J\text{-}A}$ measured on the application is about 110 °C/W.

The junction temperature of device will be estimated as follow:

(17)

$$T_J = T_A + R_{thJA} \cdot P_{TOT}$$

The dissipated power of the device is tied to three different sources:

(18)

$$P_{ON} = R_{DSON} \cdot (I_{OUT})^2 \cdot D$$

Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the switching losses related to the R_{DSON} increases compared to an ideal case.

R_{DSON} has a typical value of 0.25 Ω @ 25 °C and increases up to a maximum value of 0.5 Ω @ 125 °C. We can consider a value of 0.4 Ω.

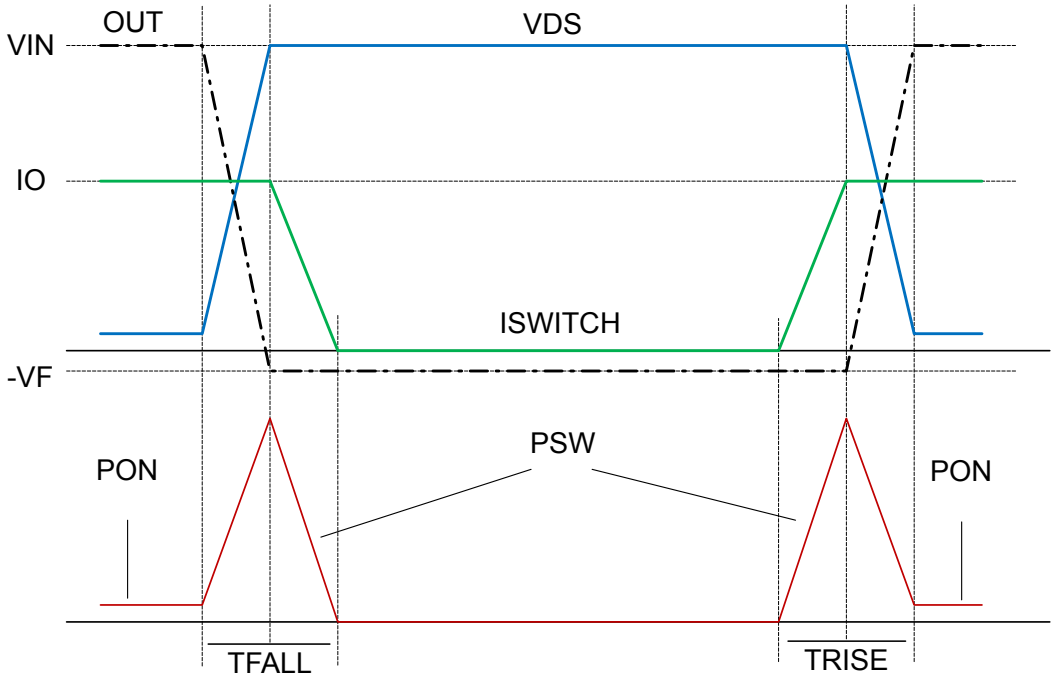
- Switching losses due to turning ON and OFF. These are derived using the following equation:

(19)

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{T_{RISE} + T_{FALL}}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{TRAN} \cdot F_{SW}$$

Where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see figure below). T_{TRAN} is the equivalent switching time, approximately 70 ns.

Figure 10. **Switching losses**



- Quiescent current losses

(20)

$$P_Q = V_{IN} \cdot I_Q$$

Where I_Q is the quiescent current, with typical value 2.5 mA @ VIN = 12 V.

The resulting power losses are given by:

(21)

$$P_{TOT} = P_{ON} + P_{SW} + P_Q$$

8.5 Maximum output voltage

The current error amplifier inputs require a biasing point at least 2 V below the VCC for proper operation, as written in Table 4. Electrical characteristics.

Adding the expected 100 mV (typical) voltage drop between VCS+ and VCS-, the maximum output voltage that guarantees the proper biasing point of the current sense circuitry is:

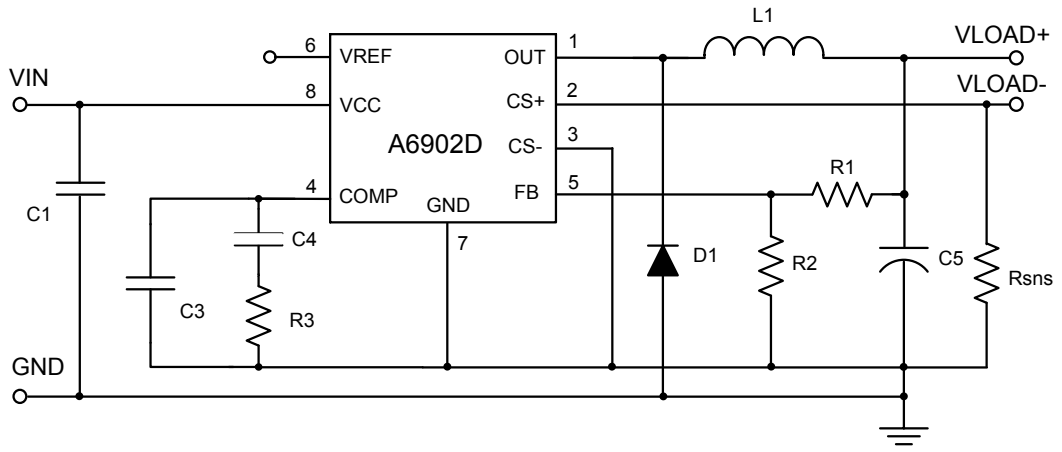
(22)

$$V_{OUT,MAX} = V_{IN,MIN} - 2.1V$$

The accuracy of the trimmed voltage offset (100 mV ± 5%) between the OTA inputs is not guaranteed if the biasing point is out of specification.

To overcome the above described limitation the low-side current sensing schematic can be implemented, as shown in figure below.

Figure 11. **Low-side current sensing implementation**



Here the current error amplifier inputs are biased at the device ground so the duty cycle limitation is no more present. The device can manage 100% duty cycle thanks to the P-CHANNEL embedded power element.

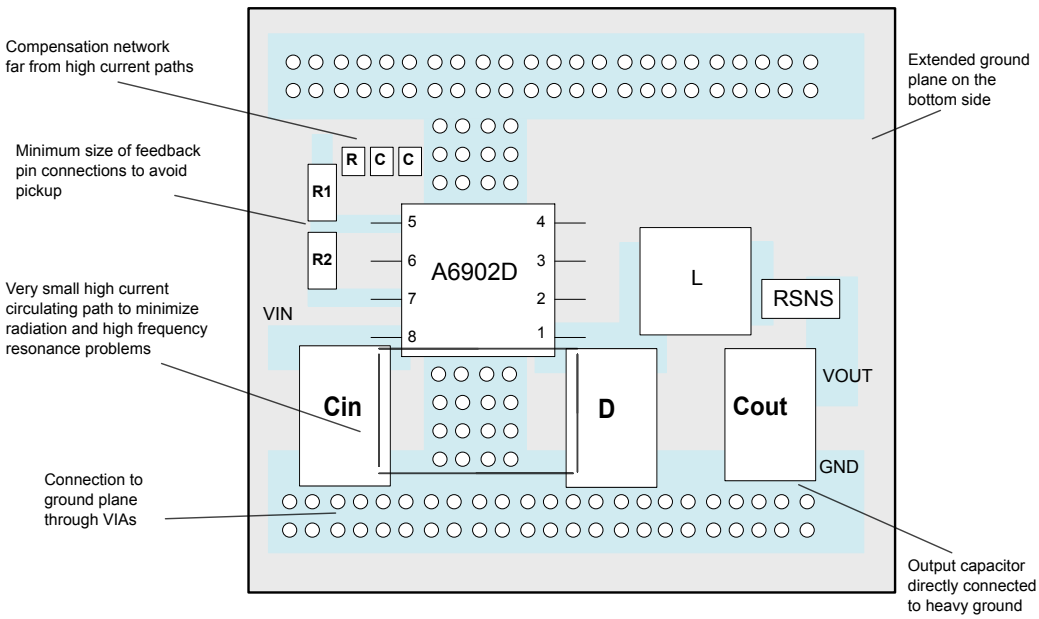
This solution is feasible if the load can be left floating (i.e. no more strictly referred to GND).

8.6 Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be routed as far as possible from the high current paths. A layout example is provided in figure below.

Figure 12. **Layout example**



The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick-up noise. Another

important issue is the ground plane of the board. It is very important to connect TOP to BOTTOM ground to improve the thermal dissipation.

9 Application circuit

Figure below shows the evaluation board application circuit, where the input supply voltage, VCC, can range from 8 V to 36 V and the programmed output voltage is 3.3 V.

Figure 13. Evaluation board application circuit

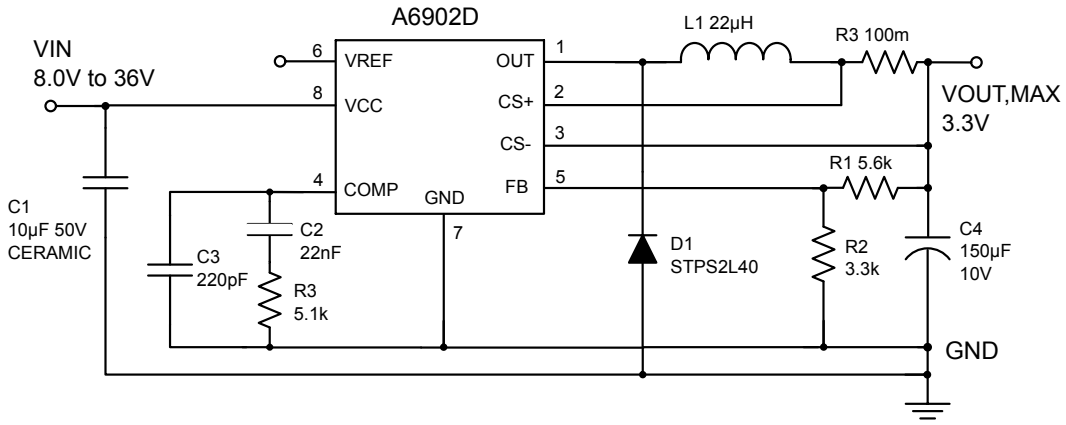


Table 7. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32ER61H106KA12L	10 µF, 50 V	Murata
C2		10 nF, 5%, 0603	
C3		33 pF, 5%, 0603	
C4	POSCAP 10TPB150ML	150 µF, 25 mΩ	Sanyo
R1		5.6 kΩ, 1%, 0.1 W, 0603	
R2		3.3 kΩ, 1%, 0.1 W, 0603	
R3		22 kΩ, 1%, 0.1 W, 0603	
D1	STPS2L40U	2 A, 40 V	STMicroelectronics
L1	DO1813HC-223	22 µH, 1,2 A sat / 0,25 Ω	Coilcraft
U1	A6902D		STMicroelectronics

Figure 14. **PCB layout (component side)**

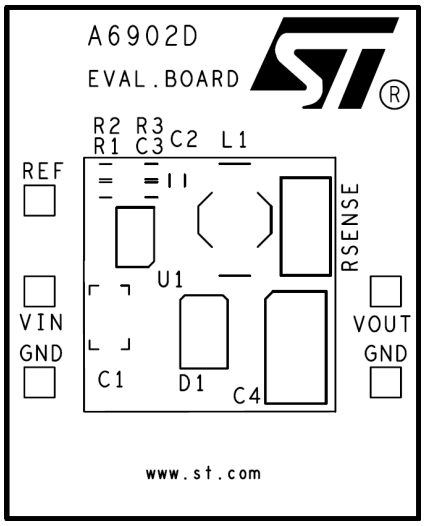


Figure 15. **PCB layout (BOTTOM side)**

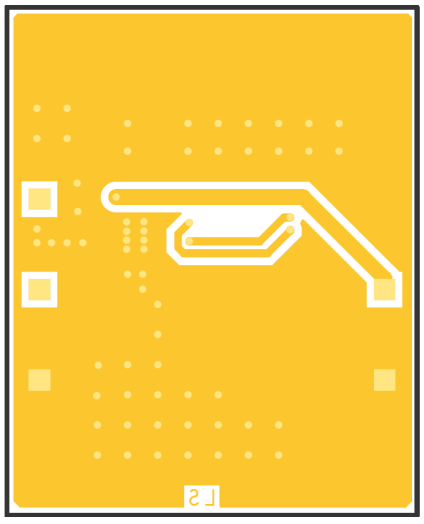
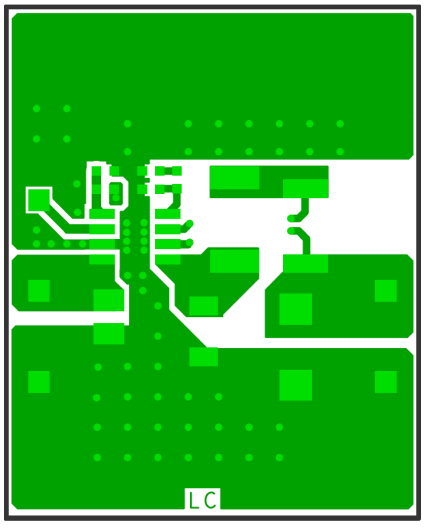


Figure 16. **PCB layout (TOP side)**



10 Typical characteristics

Figure 17. Line regulation

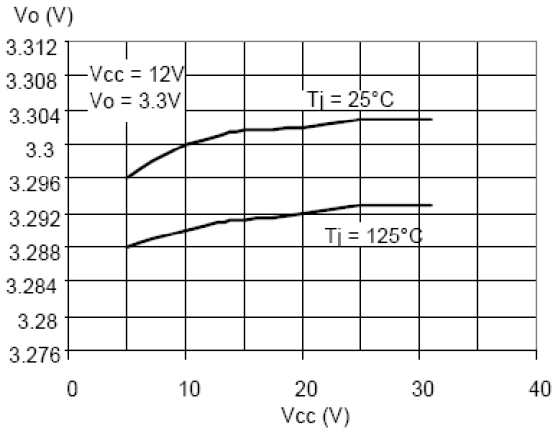


Figure 18. Shutdown current vs. junction temperature

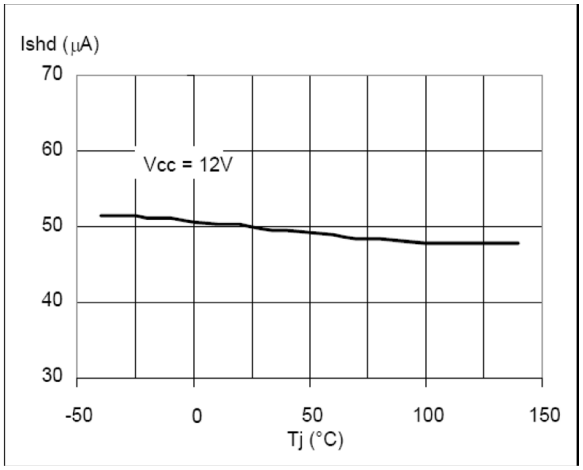


Figure 19. Output voltage vs. junction temperature

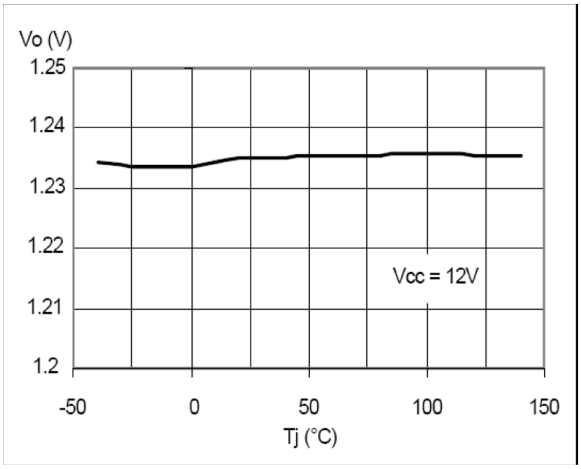


Figure 20. Switching frequency vs. junction temperature

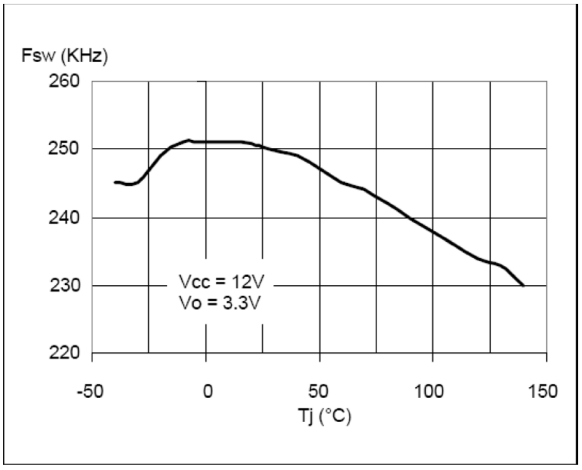


Figure 21. **Quiescent current vs. junction temperature**

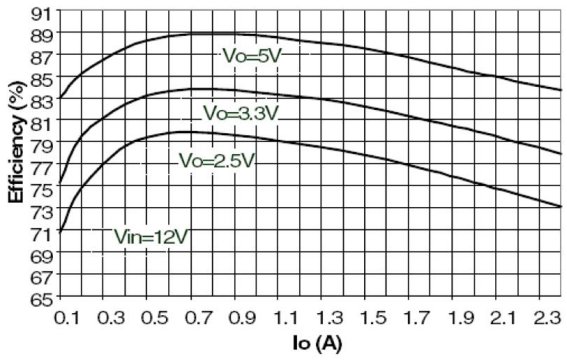
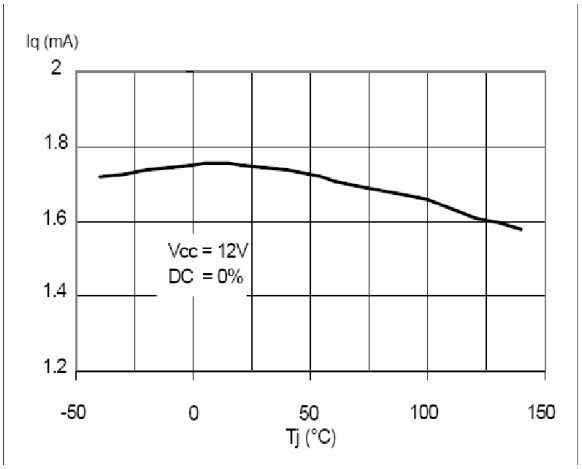


Figure 22. **Efficiency vs. output current**



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 SO8 package information

Figure 23. **SO8 package outline**

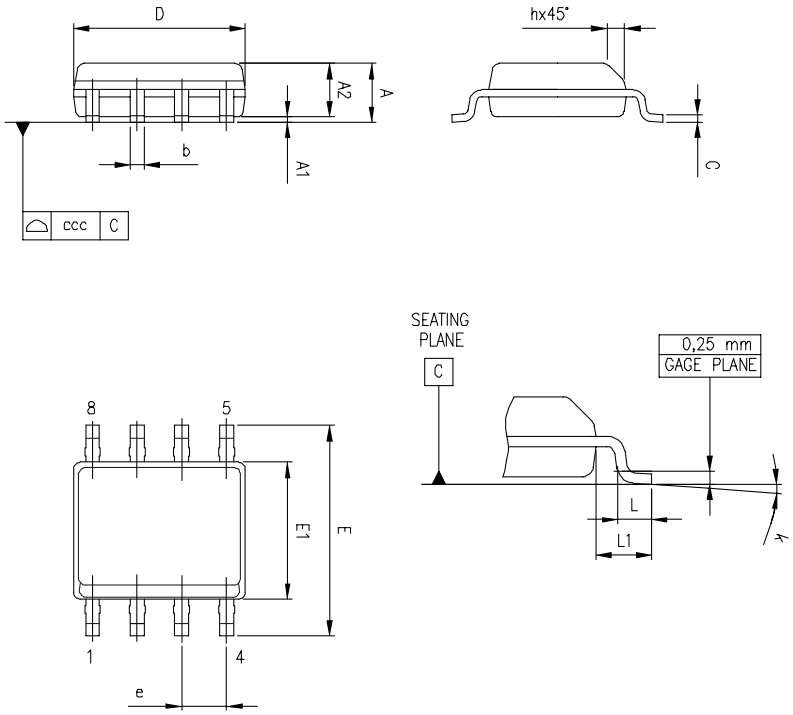


Table 8. **SO-8 mechanical data**

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.01
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		0.127			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min), 8° (max)					
ddd			0.10			0.004

1. *Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 inch) in total (both side)*

12 Ordering information

Table 9. **Order codes**

Order code	Package	Packing
A6902D	SO8	Tube
A6902D13TR		Tape and reel

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
02-Oct-2007	1	First release
5-Nov-2007	2	Updated: Electrical characteristics table
2-May-2008	3	Updated: Electrical characteristics table
28-Aug-2008	4	Updated: Coverpage and Electrical characteristics table
23-Apr-2009	5	Updated: first feature in coverpage
24-Oct-2018	6	Added: Functional description Section 5 Functional description

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