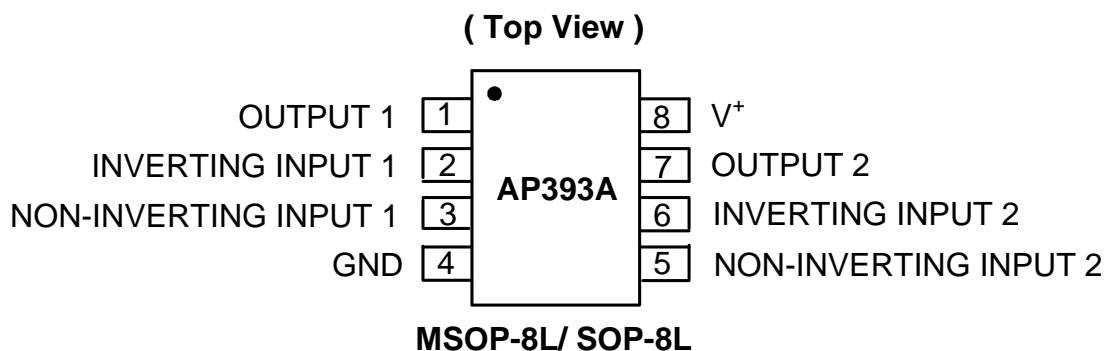


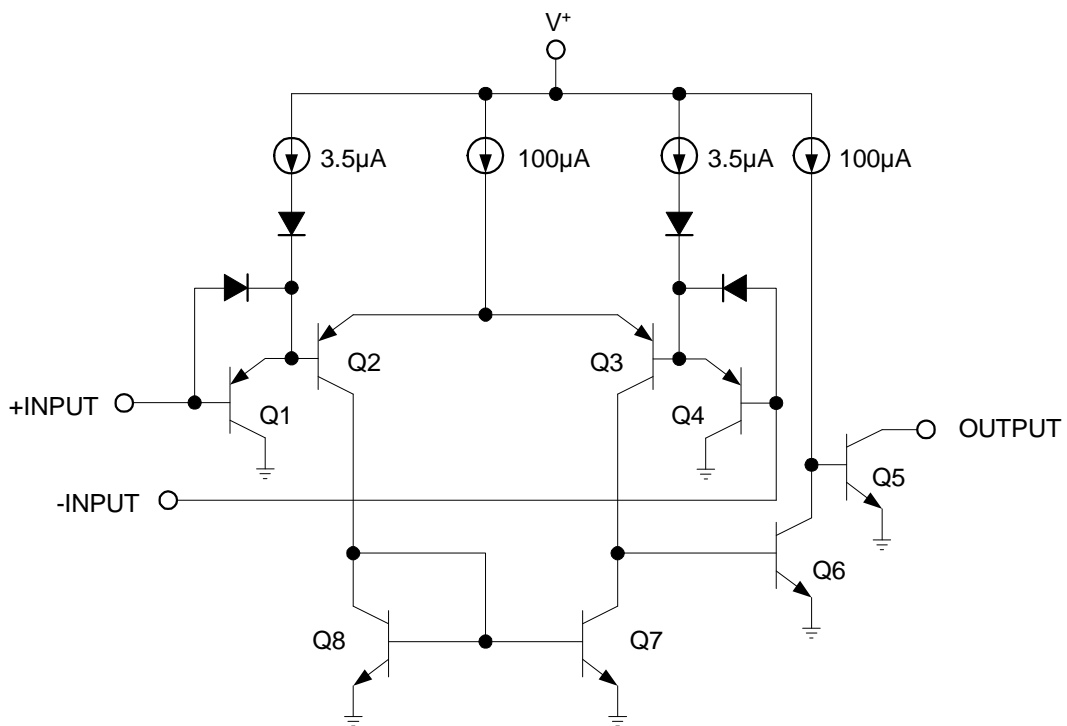
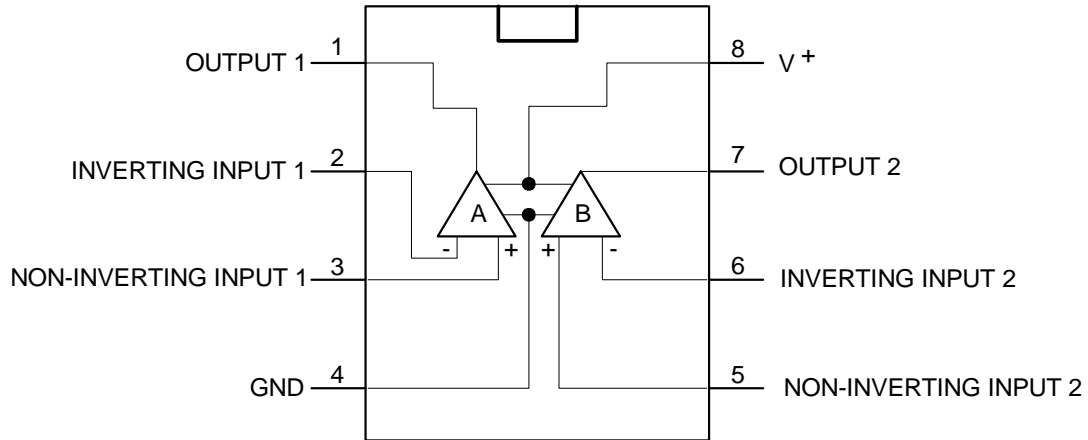
### Pin Assignments



### Pin Descriptions

Pin Name	Pin No.	Description
OUTPUT 1	1	Channel 1 Output
INVERTING INPUT 1	2	Channel 1 Negative Input
NON-INVERTING INPUT 1	3	Channel 1 Positive Input
GND	4	Ground
NON-INVERTING INPUT 2	5	Channel 2 Positive Input
INVERTING INPUT 2	6	Channel 2 Negative Input
OUTPUT 2	7	Channel 2 Output
V <sup>+</sup>	8	V <sub>CC</sub>

**Block Diagram**



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	
$V_{CC}$	Supply Voltage	40	V	
$V_{IN}$	Differential Input Voltage (Note 10)	40	V	
$V_{IN}$	Input Voltage	-0.3 to +40	V	
$I_{CC}$	Input Current ( $V_{IN}=0.3V$ ) (Note 5)	50	mA	
$P_D$	Power Dissipation (Note 3)	MSOP-8L	670	mW
		SOP-8L	510	
	Output Short-Circuit to Ground (Note 4)	Continuous		
$T_{OP}$	Operating Junction Temperature Range	0 to +70	°C	
$T_{ST}$	Storage Temperature Range	-65 to +150	°C	

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage (Single)	+2	+36	V
$V_{CC}$	Supply Voltage (Dual Supplies, $V^+$ VS GND)	$\pm 1$	$\pm 18$	V
$V_{IN}$	Differential Input Voltage (Single) (Note 10)	0	$\pm 36$	V
$V_{IN}$	Differential Input Voltage (Dual Supplies) (Note 10)	-18	+18	V
$T_A$	Operating Ambient Temperature	0	70	°C

### Electrical Characteristics

( $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ , unless otherwise stated)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$V_{OFFSET}$	Input Offset Voltage	(Note 11)	-	4.0	8.0	mV
$I_{OFFSET}$	Input Offset Current	$I_{IN(+)} - I_{IN(-)}$ , $V_{CM} = 0V$	-	70	150	nA
$I_{BIAS}$	Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output In Linear Range, $V_{CM} = 0V$ (Note 7)	-	150	400	nA
	Input Common Mode Voltage Range	$V^+ = 30V$ (Note 8)	0	-	$V^+ - 1.5$	V
$I_{CC}$	Supply Current	$R_L = \infty$ , $V^+ = 5V$	-	0.4	1	mA
		$V^+ = 36V$	-	1	2.5	
	Voltage Gain	$R_L \geq 15k\Omega$ , $V^+ = 15V$ , $V_O = 1V$ to $11V$	50	200	-	V/mV
	Large Signal Response Time	$V_{IN} =$ TTL Logic Swing, $V_{REF} = 1.4V$ , $V_{RL} = 5V$ , $R_L = 5.1k\Omega$	-	300	-	ns
	Response Time	$V_{RL} = 5V$ , $R_L = 5.1k\Omega$ (Note 9)	-	1.3	-	$\mu s$
$I_{O(SINK)}$	Output Sink Current	$V_{IN(-)} = 1V$ , $V_{IN(+)} = 0$ , $V_O \leq 1.5V$	6.0	16	-	mA
$V_{SAT}$	Saturation Voltage	$V_{IN(-)} = 1V$ , $V_{IN(+)} = 0$ , $I_{SINK} \leq 4mA$	-	250	400	mV
$I_{O(Leak)}$	Output Leakage Current	$V_{IN(-)} = 0$ , $V_{IN(+)} = 1V$ , $V_O = 5V$	-	0.1	-	nA

### Electrical Characteristics (Continued)

( $V_{CC} = 5V$ ) (Note 6)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$V_{OFFSET}$	Input Offset Voltage	(Note 11)	-	-	9	mV
$I_{OFFSET}$	Input Offset Current	$I_{IN(+)} - I_{IN(-)}$ , $V_{CM} = 0V$	-	-	180	nA
$I_{BIAS}$	Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output In Linear Range, $V_{CM} = 0V$ (Note 7)	-	-	500	nA
	Input Common Mode Voltage Range	$V^+ = 30V$ (Note 8)	0	-	$V^+ - 2.0$	V
$V_{SAT}$	Saturation Voltage	$V_{IN(-)} = 1V$ , $V_{IN(+)} = 0$ , $I_{SINK} \leq 4mA$	-	-	700	mV
$I_{O(Leak)}$	Output Leakage Current	$V_{IN(-)} = 0$ , $V_{IN(+)} = 1V$ , $V_O = 30V$	-	-	1.0	$\mu A$
	Differential Input Voltage	Keep All $V_{IN}$ 's $\geq 0V$ (or $V^+$ , if Used), (Note 10)	-	-	36	V
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	MSOP-8L (Note 12)		208		$^{\circ}C/W$
		SOP-8L (Note 12)		165		
$\theta_{JC}$	Thermal Resistance Junction-to-Case	MSOP-8L (Note 12)		39		$^{\circ}C/W$
		SOP-8L (Note 12)		26		

- Notes:
- For operating at high temperatures, the AP393A must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ( $P_D \leq 100mW$ ), provided the output transistors are allowed to saturate.
  - Short circuits from the output to  $V^+$  can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of  $V^+$ .
  - This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the  $V^+$  voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than -0.3V.
  - The AP393A temperature specifications are limited to  $0^{\circ}C \leq T_{OP} \leq +70^{\circ}C$ .
  - The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
  - The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is  $V^+ - 1.5V$  at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of  $V^+$ .
  - The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained, see typical performance characteristics section.
  - Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
  - At output switch point,  $V_O \approx 1.4V$ ,  $R_S = 0\Omega$  with  $V^+$  from 5V to 30V; and over the full input common-mode range (0V to  $V^+ - 1.5V$ ), at 25°C.
  - Test condition for MSOP-8L and SOP-8L: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

### Application Information

The AP393A is high gain, wide bandwidth devices, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to  $< 10\text{k}\Omega$  reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required. All input pins of any unused comparators should be tied to the negative supply.

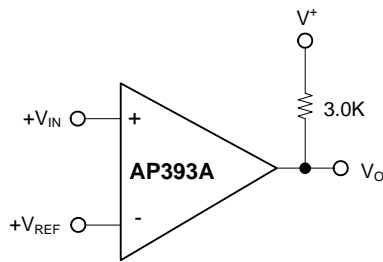
The bias network of the AP393A establishes a drain current independent of the magnitude of the power supply voltage over the range of from  $2.0 V_{DC}$  to  $30 V_{DC}$ . It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than  $V+$  without damaging the device (Note 10). Protection should be provided to prevent the input voltages from going negative more than  $-0.3 V_{DC}$  (at  $25^\circ\text{C}$ ). An input clamp diode can be used as shown in the applications section.

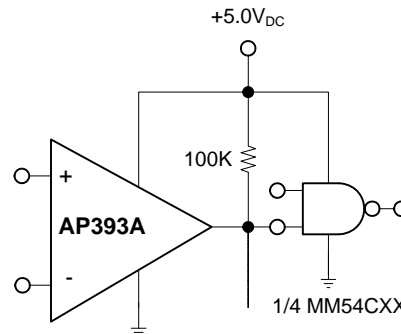
The output of the AP393A is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage applied to the  $V+$  terminal of the AP393A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current the output device can sink is limited by the drive available (which is independent of  $V+$ ) and the  $\beta$  of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately  $60\Omega r_{SAT}$  of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

### Typical Circuit

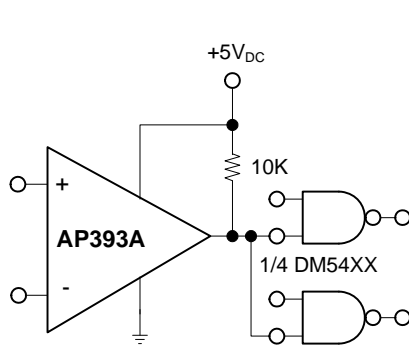
(  $V_{CC} = 5.0V_{DC}$  )



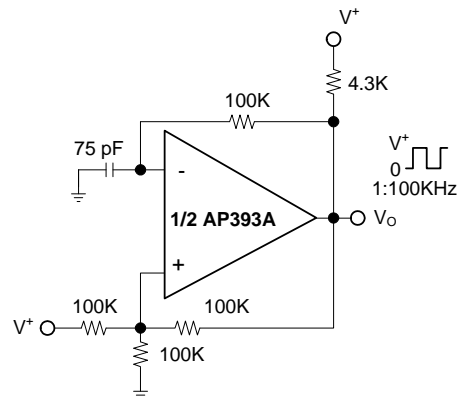
**Basic Comparator**



**Driving CMOS**



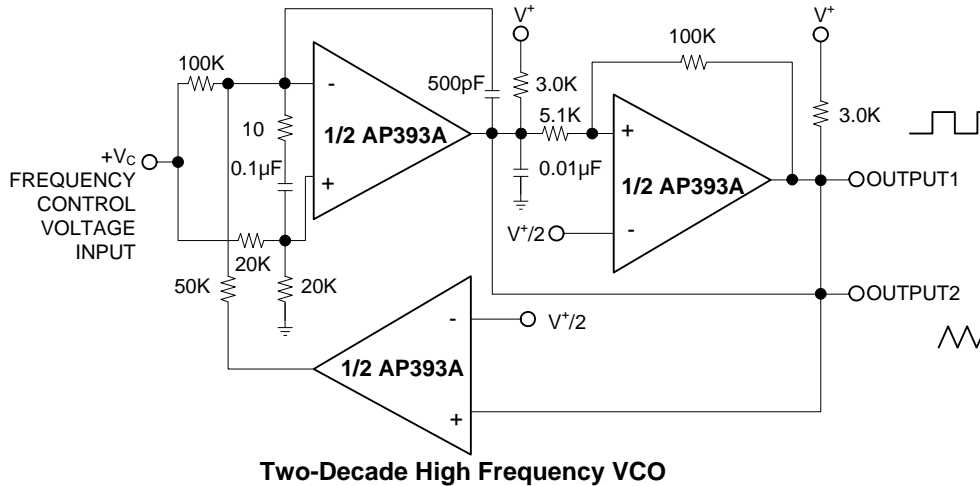
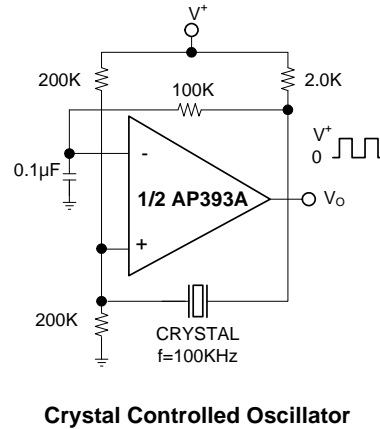
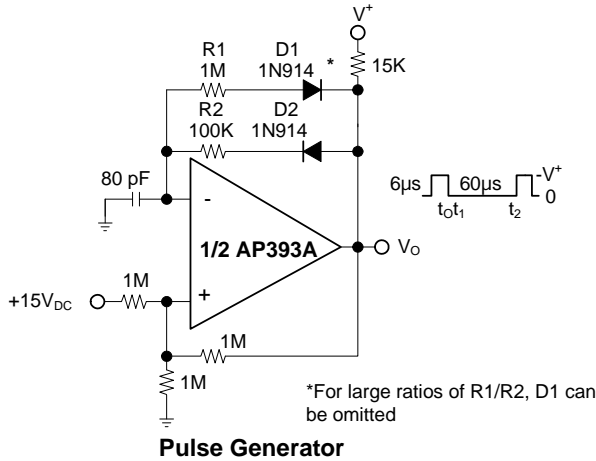
**Driving TTL**



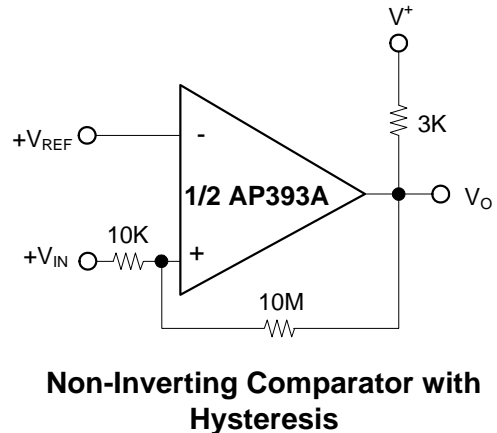
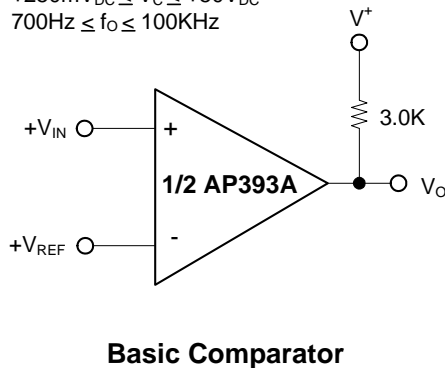
**Squarewave Oscillator**

**Typical Circuit (Continued)**

( $V_{CC} = 5.0V_{DC}$ )

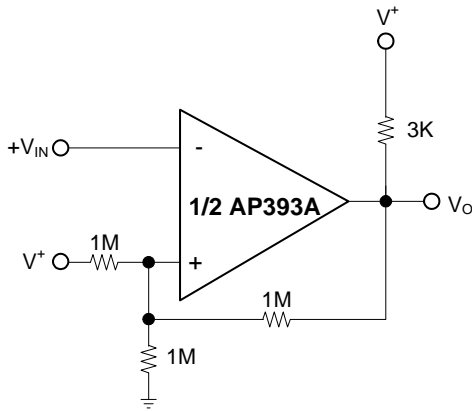


$V^* = +30V_{DC}$   
 $+250mV_{DC} \leq V_C \leq +50V_{DC}$   
 $700Hz \leq f_o \leq 100KHz$

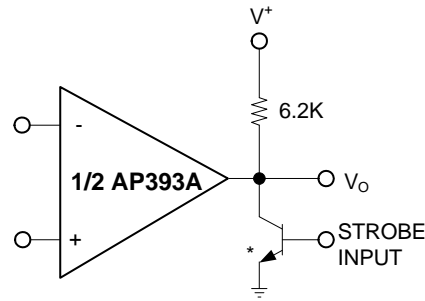


**Typical Circuit (Continued)**

( $V_{CC} = 5.0V_{DC}$ )

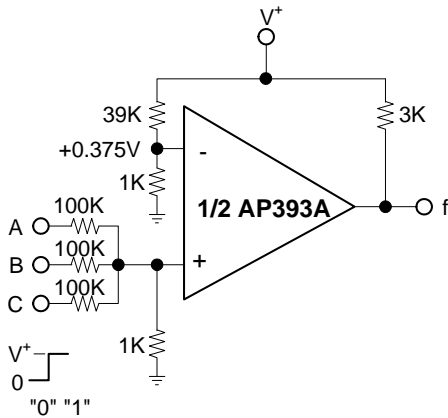


**Inverting Comparator with Hysteresis**

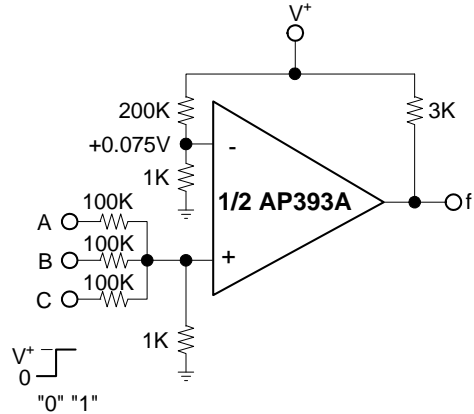


\* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

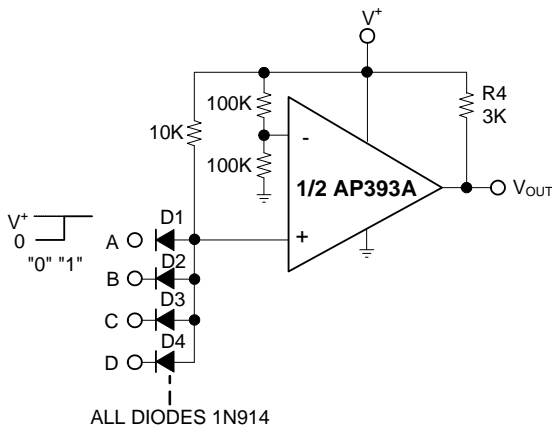
**Output Strobing**



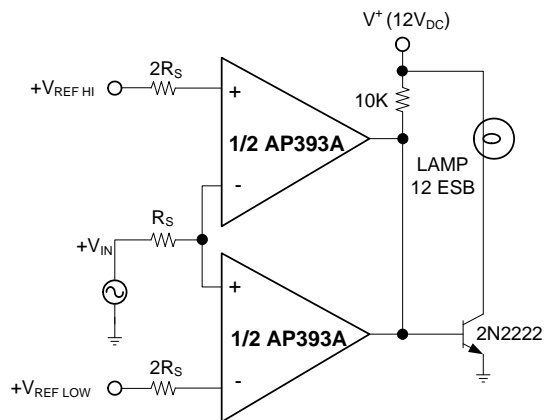
**AND Gate**



**Or Gate**



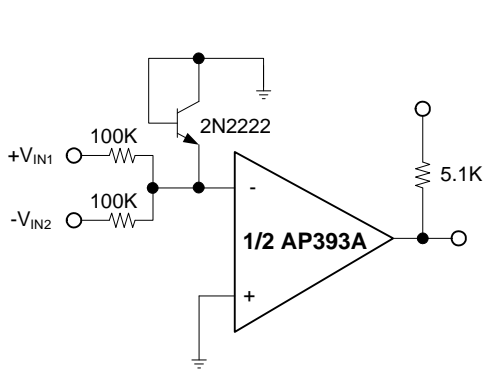
**Large Fan-in AND Gate**



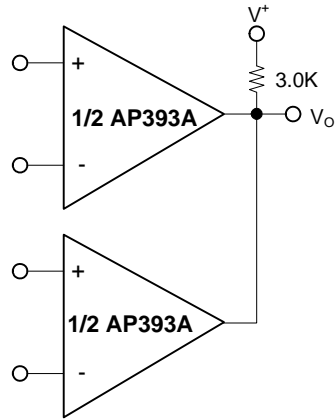
**Limit Comparator**

**Typical Circuit (Continued)**

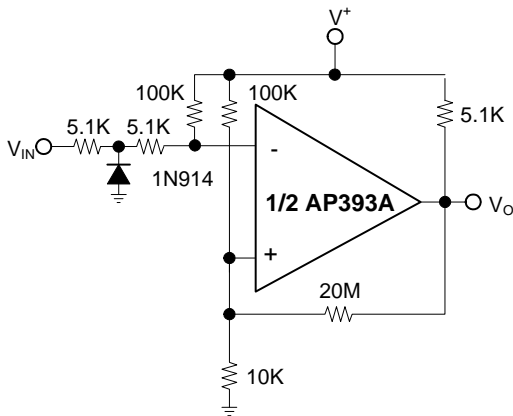
( $V_{CC} = 5.0V_{DC}$ )



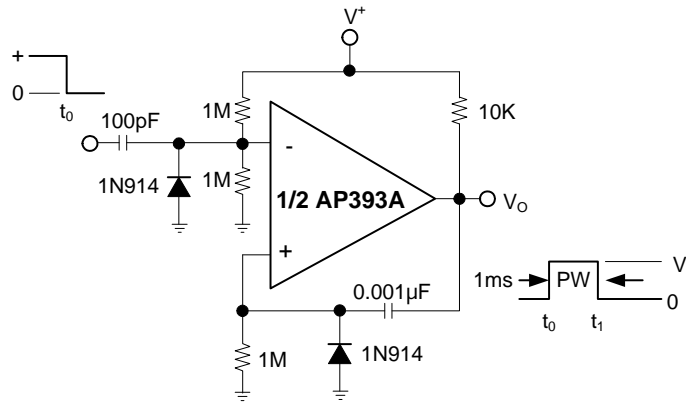
**Comparing Input Voltages of Opposite Polarity**



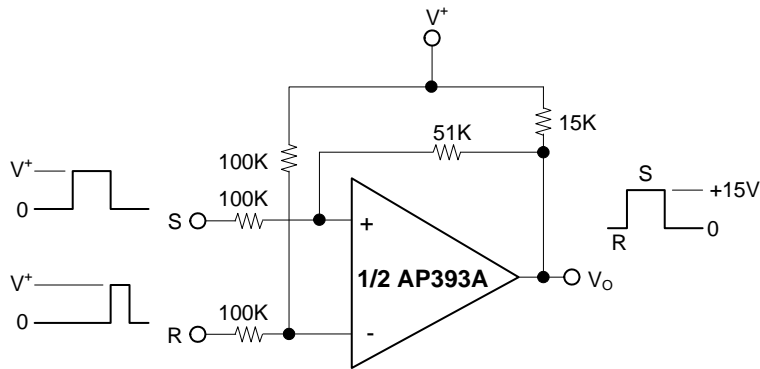
**ORing the Outputs**



**Zero Crossing Detector (Single Power Supply)**



**One-Shot Multivibrator**

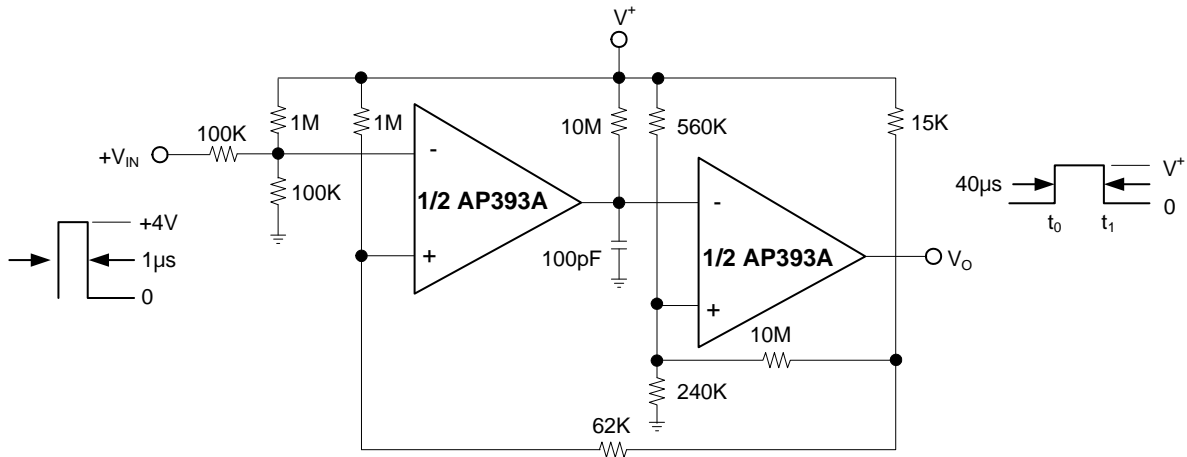


**Bi-Stable Multivibrator**

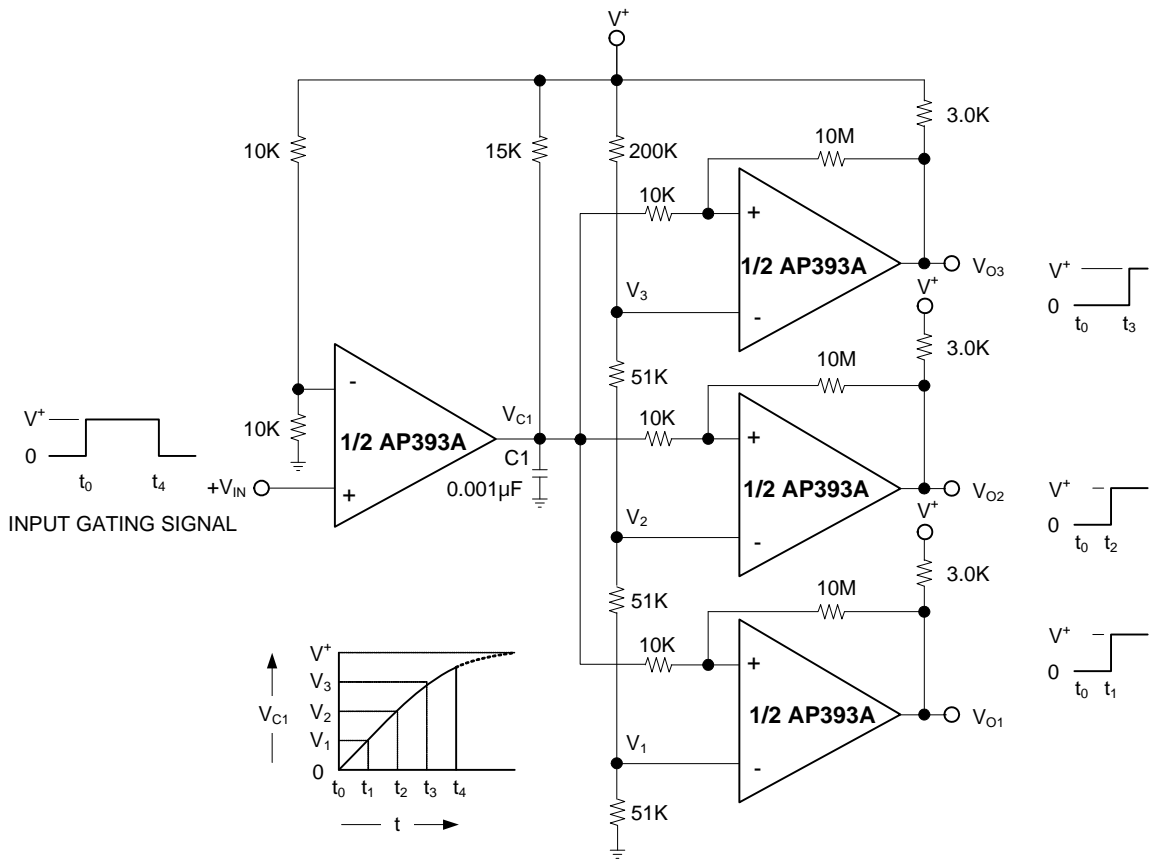


**Typical Circuit (Continued)**

( $V_{CC} = 5.0V_{DC}$ )



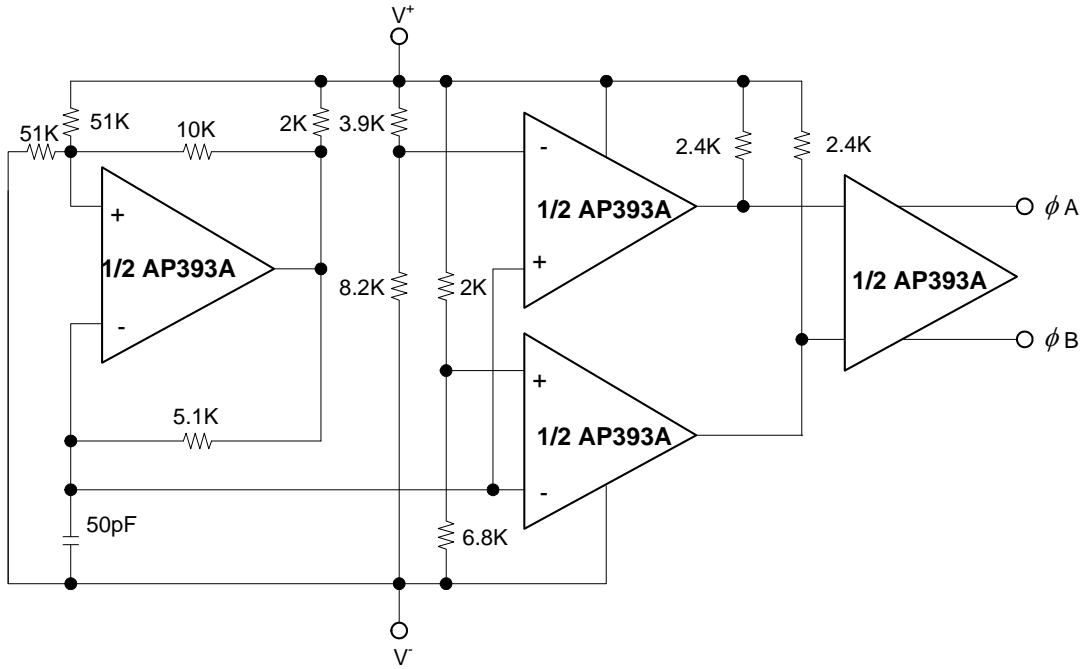
**One-Shot Multivibrator with Input Lock Out**



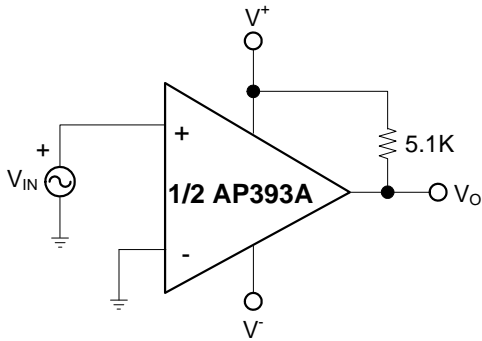
**Time Delay Generator**

**Split-Supply Applications**

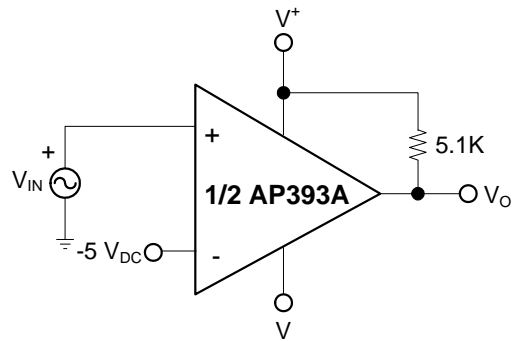
(  $V^+$  = +15V<sub>DC</sub> and  $V^-$  = -15 V<sub>DC</sub> )



**MOS Clock Driver**



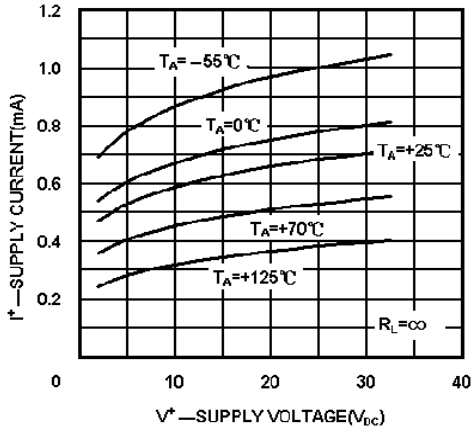
**Zero Crossing Detector**



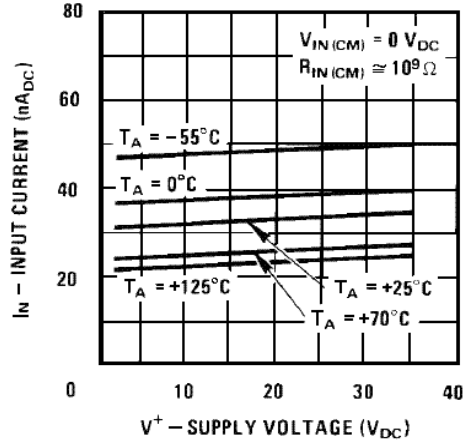
**Comparator With a  
Negative Reference**

**Typical Characteristics**

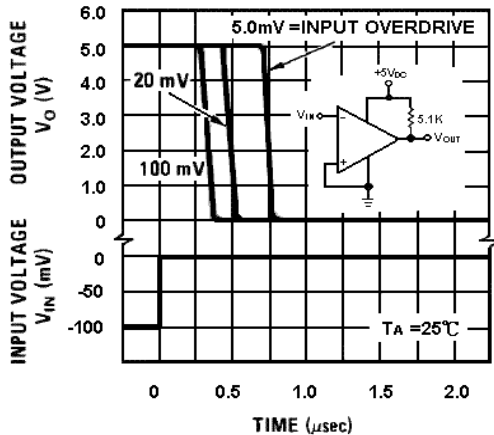
**Supply Current**



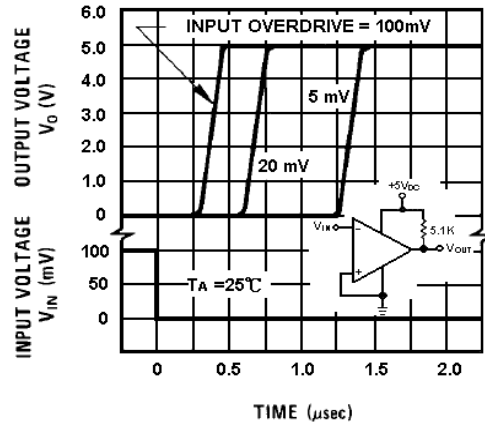
**Input Current**



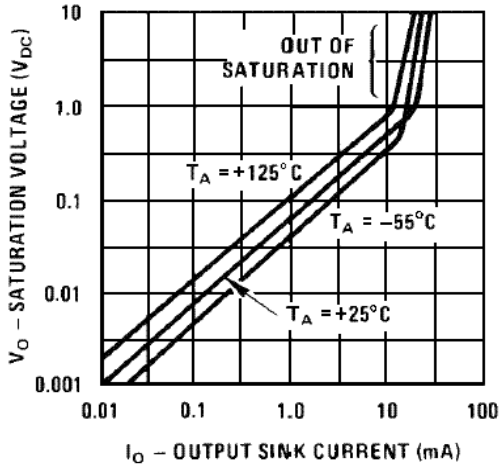
**Response Time for Various Input Overdrives—Negative Transition**



**Response Time for Various Input Overdrives—Positive Transition**

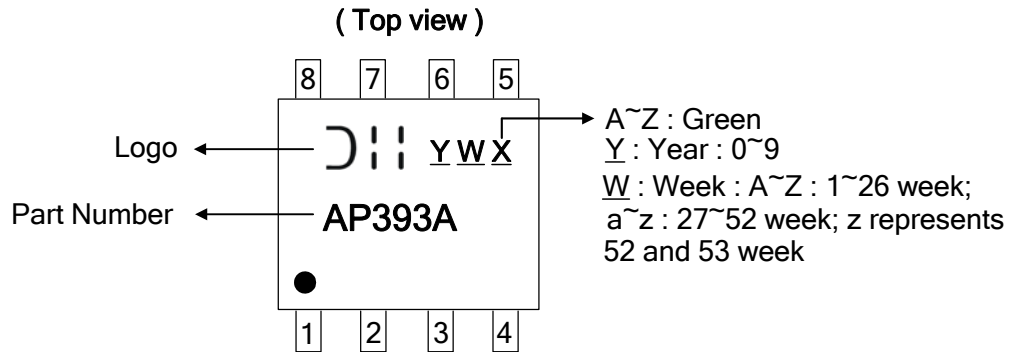


**Output Saturation Voltage**

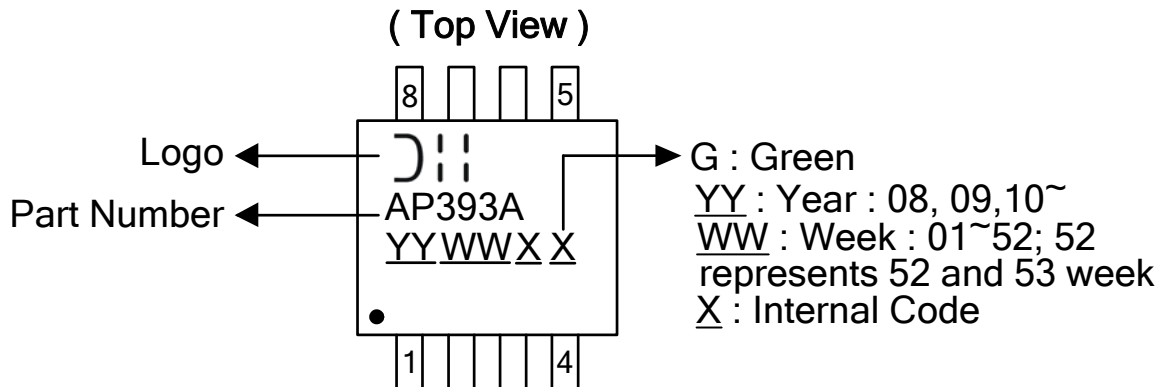


**Marking Information**

(1) MSOP-8L

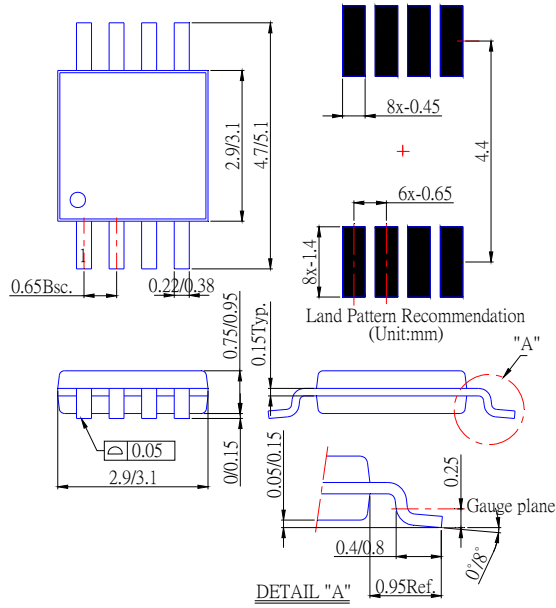


(2) SOP-8L

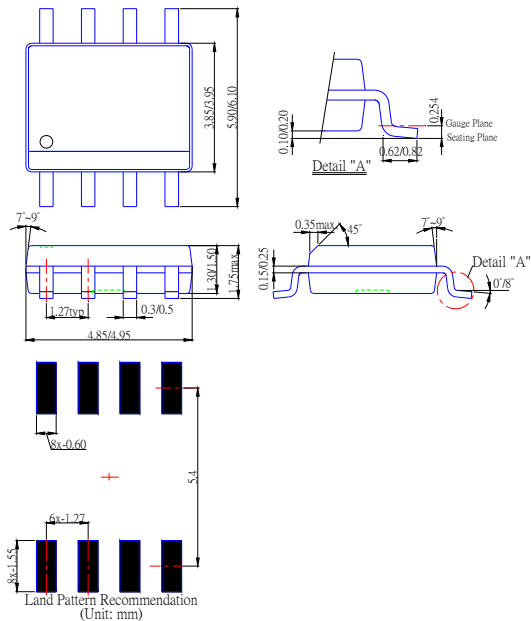


**Package Information (All Dimensions in mm)**

**(1) Package Type: MSOP-8L**



**(2) Package Type: SOP-8L**



**IMPORTANT NOTICE**

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to any product herein. Diodes Incorporated does not assume any liability arising out of the application or use of any product described herein; neither does it convey any license under its patent rights, nor the rights of others. The user of products in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on our website, harmless against all damages.

**LIFE SUPPORT**

Diodes Incorporated products are not authorized for use as critical components in life support devices or systems without the expressed written approval of the President of Diodes Incorporated.