1 Characteristics

Symbol		Value	Unit		
V _{PP}	Peak pulse voltage	IEC 61000-4-2 contact dis IEC 61000-4-2 air dischar	±30	kV	
P _{PP} ⁽¹⁾	Peak pulse power dis	150	W		
I _{PP}	Peak pulse current (8	9	А		
Тj	Junction temperature	-55 to +150	°C		
T _{stg}	Storage temperature	-65 to +150	°C		
ΤL	Maximum lead tempe	260	°C		

Table 1. Absolute maximum ratings ($T_{amb} = 25 \ ^{\circ}C$)

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

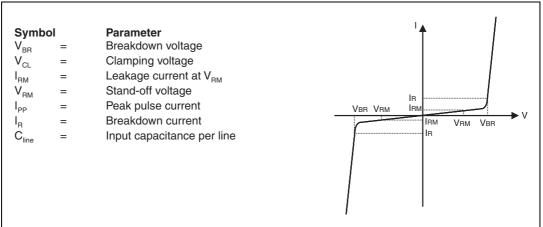
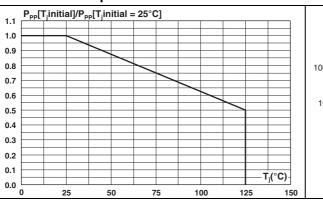


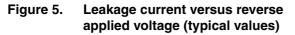
Table 2.Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test condition	Min.	Тур.	Max.	Unit	
V	From pin1 to pin2, I _R = 1 mA		13		V	
V _{BR}	From pin2 to pin1, I _R = 1 mA 5 8			v		
	V _{RM} = 3 V			10	nA	
IRM	V _{RM} = 1 V			1	ПА	
R _d	Square pulse, $I_{PP} = 1 \text{ A}$, $t_p = 2.5 \ \mu s$		650		mΩ	
C _{line}	$F = 1 \text{ MHz}, V_{R} = 0 \text{ V}$		26	30	pF	



Figure 3. Relative variation of peak pulse power versus initial junction temperature





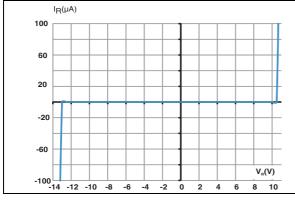
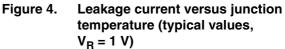
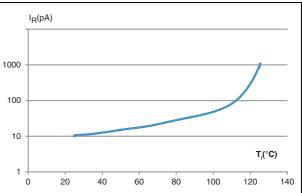
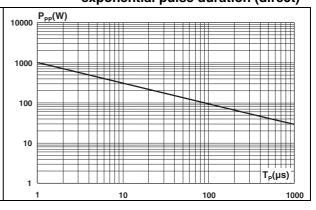


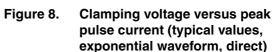
Figure 7. Peak pulse power versus exponential pulse duration (reverse)





Peak pulse power versus exponential pulse duration (direct)





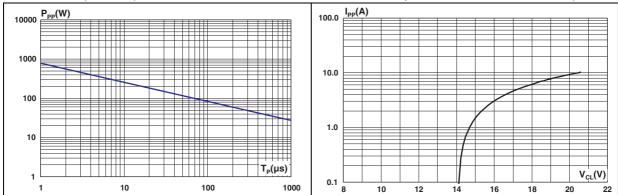
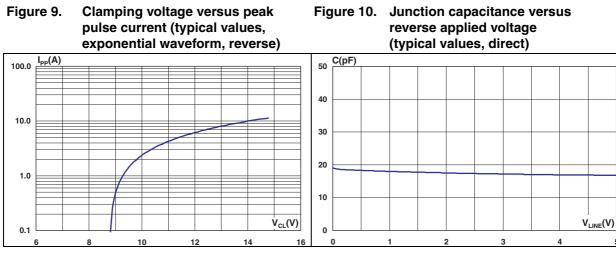
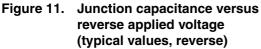
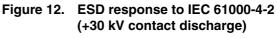


Figure 6.







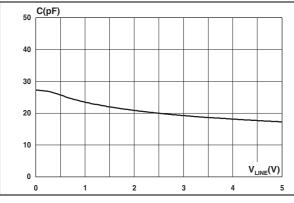


Figure 13. ESD response to IEC 61000-4-2 (-30 kV contact discharge)

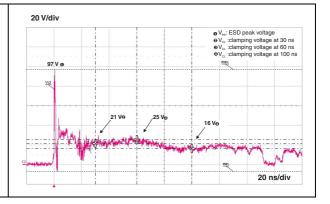
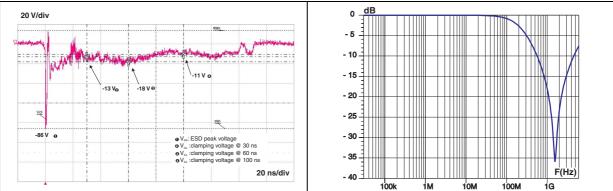
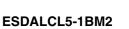


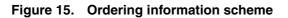
Figure 14. S21 attenuation measurement result







2 Ordering information scheme



ESD array	
Low capacitance	
Low leakage	
Breakdown voltage	
5 = 5 Volts minimum	
Number of lines	
1 = 1 line protected	
Directional	
B = Bi-directional	
Package	
M2 = SOD882	



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK[®] is an ST trademark.

Figure 16. SOD882 dimension definitions

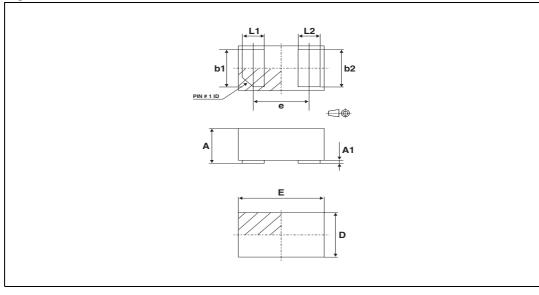
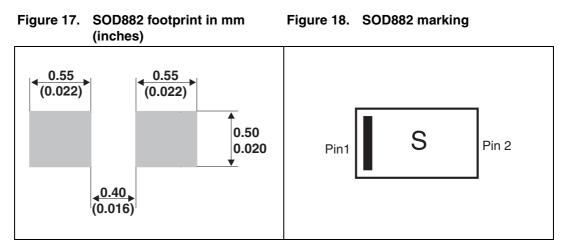


Table 3.SOD882 dimension values

	Dimensions							
Ref.	Millimeters			Inches				
	Min.	Тур.	Max.	Min.	Тур.	Max.		
А	0.40	0.47	0.50	0.016	0.019	0.020		
A1	0.00		0.05	0.000		0.002		
b1	0.45	0.50	0.55	0.018	0.020	0.022		
b2	0.45	0.50	0.55	0.018	0.020	0.022		
D	0.55	0.60	0.65	0.022	0.024	0.026		
E	0.95	1.00	1.05	0.037	0.039	0.041		
е	0.60	0.65	0.70	0.024	0.026	0.028		
L1	0.20	0.25	0.30	0.008	0.010	0.012		
L2	0.20	0.25	0.30	0.008	0.010	0.012		





Note:

Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

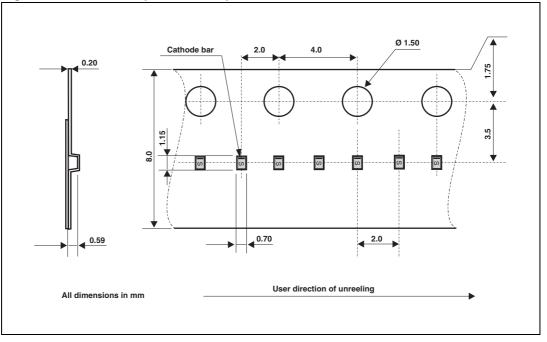


Figure 19. SOD882 tape and reel specifications

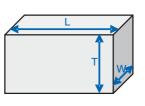


4 **Recommendations on PCB assembly**

4.1 Stencil opening design

- 1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 20. Stencil opening dimensions



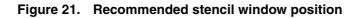
b) General design rule

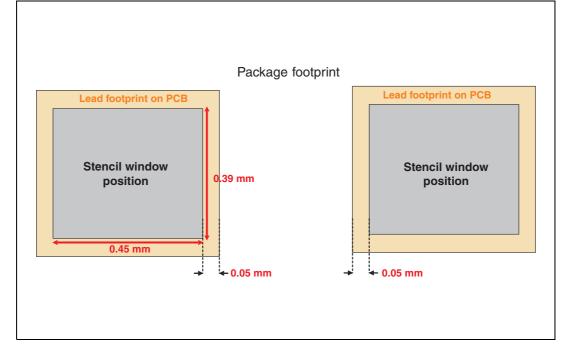
Stencil thickness (T) = 75 ~ 125 μ m

Aspect Ratio =
$$\frac{W}{T} \ge 1.5$$

Aspect Area =
$$\frac{L \times W}{2T(L+W)} \ge 0.66$$

- 2. Reference design
 - a) Stencil opening thickness: 100 µm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.





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4.2 Solder paste

- 1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
- 2. "No clean" solder paste is recommended.
- 3. Offers a high tack force to resist component movement during high speed.
- 4. Solder paste with fine particles: powder particle size is 20-45 $\mu m.$

4.3 Placement

- 1. Manual positioning is not recommended.
- 2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- 3. Standard tolerance of \pm 0.05 mm is recommended.
- 4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
- 5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
- 6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

- 1. To control the solder paste amount, the closed via is recommended instead of open vias.
- 2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.



4.5 Reflow profile

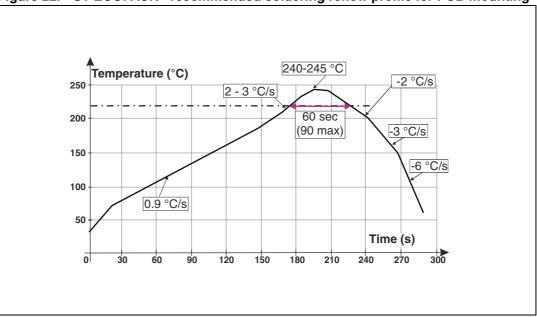


Figure 22. ST ECOPACK[®] recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement.



5 Ordering information

Table 4. Ordering information

Order code	Marking ⁽¹⁾	Package	Weight	Base qty	Delivery mode
ESDALCL5-1BM2	S	SOD882	0.92 mg	12,000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location

6 Revision history

Table 5.Document revision history

Date	Revision	Changes
31-Oct-2012	1	Initial release.



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