High-Bandwidth, Quad DPDT Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+ .....-0.3V to +6V
IN_, $\overline{EN}$ (MAX4761) .....-0.3V to +6V
IN_, $\overline{EN}$ (MAX4761A).....-0.3V to (V+ + 0.3V)
COM_, NO_, NC_ (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current
NO_, NC_, COM_ .....±100mA
Peak Current
(pulsed at 1ms, 10% duty cycle).....±200mA
(pulsed at 1ms, 50% duty cycle)..... ±300mA

Continuous Power Dissipation (T_A = +70°C)
36-Bump UCSP (derate 15.3mW/°C above +70°C).... 1221mW
36-Pin TQFN (derate 26.3mW/°C above +70°C)..... 2105mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Bump Temperature (soldering)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			T_{MIN} to T_{MAX}	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NC\_}$ or $V_{NO\_}$ = 0V or V+ (Note 4)		+25°C		2.0	3.5	Ω
				T_{MIN} to T_{MAX}			4	
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V (Notes 4, 5)		+25°C		0.2	0.4	Ω
				T_{MIN} to T_{MAX}			0.55	
On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$= 10mA, $V_{NC\_}$ or $V_{NO\_}$ = 0V or V+ (Note 6)		+25°C		0.8	1.5	Ω
				T_{MIN} to T_{MAX}			1.8	
NO_, NC_ Off-Leakage Current	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V		+25°C	-5		+5	nA
				T_{MIN} to T_{MAX}	-25		+25	
COM_ Off-Leakage Current		V+ = 3.6V (MAX4761/MAX4761A); $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V		+25°C	-5	0.1	+5	nA
				T_{MIN} to T_{MAX}	-25		+25	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V or unconnected		+25°C	-5		+5	nA
				T_{MIN} to T_{MAX}	-25		+25	
DYNAMIC								
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 2	MAX4760/ MAX4761	+25°C		45	140	ns
				T_{MIN} to T_{MAX}			150	
			MAX4760A/ MAX4761A	+25°C		400	800	ns
				T_{MIN} to T_{MAX}			800	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	V+ = 2.7V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 2	MAX4760/ MAX4761	+25°C		25	50	ns
				T_{MIN} to T_{MAX}			60	
			MAX4760A/ MAX4761A	+25°C		300	800	ns
				T_{MIN} to T_{MAX}			800	
Break-Before-Make	t_{BBM}	V+ = 2.7V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω, C_L = 35pF, Figure 3 (Note 7)		+25°C		100		ns
				T_{MIN} to T_{MAX}	2			
Skew	t_{SKEW}	R_S = 39Ω, C_L = 50pF, Figure 4 (Note 7)		+25°C		0.2		ns
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0V, C_L = 1.0nF, Figure 5		+25°C		15		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C_L = 5pF, R_L = 50Ω		+25°C		150		MHz
Off-Isolation	V_{ISO}	C_L = 5pF, R_L = 50Ω, $V_{COM\_}$ = $1V_{P-P}$, f = 100kHz, Figure 6 (Note 8)		+25°C		80		dB
Crosstalk	V_{CT}	C_L = 5pF, R_L = 50Ω, $V_{COM\_}$ = $1V_{P-P}$, f = 100kHz, Figure 6 (Note 9)		+25°C		95		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz , $V_{COM\_}$ = $1V_{P-P}$, DC bias = V+/2, R_L = R_S = 600Ω		+25°C		0.03		%
NO_, NC_ Off-Capacitance	$C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$	$V_{NO\_}$, $V_{NC\_}$ = GND, f = 1MHz, Figure 7		+25°C		25		pF
COM_ On-Capacitance	$C_{COM(ON)}$	$V_{NO\_}$, $V_{NC\_}$ = GND, f = 1MHz, Figure 7		+25°C		54		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	$V_{COM\_}$ = GND, f = 1MHz (MAX4761/ MAX4761A), Figure 7		+25°C		25		pF
DIGITAL I/O (IN_, $\overline{EN}$)								
Input-Logic High	V_{IH}	V+ = 2.7V to 3.6V		T_{MIN} to T_{MAX}	1.4			V
		V+ = 3.6V to 5.5V (MAX4760A/MAX4761A)		T_{MIN} to T_{MAX}	1.6			
		V+ = 3.6V to 5.25V (MAX4760/MAX4761)		T_{MIN} to T_{MAX}	2.0			
Input-Logic Low	V_{IL}	V+ = 2.7V to 3.6V		T_{MIN} to T_{MAX}			0.5	V
		V+ = 3.6V to 5.5V (MAX4760A/MAX4761A)		T_{MIN} to T_{MAX}			0.5	
		V+ = 3.6V to 5.25V (MAX4760/MAX4761)		T_{MIN} to T_{MAX}			0.6	
Input Leakage Current	I_{IN}, I_{EN}	V_{IN} = 0V or V+		T_{MIN} to T_{MAX}			1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Power Supply Current	I+	V+ = 4.3V, $V_{IN\_}$ = 0V or V+ (MAX4760/MAX4761)	+25°C		0.01		µA
			T_{MIN} to T_{MAX}			1.0	
		V+ = 5.5V, $V_{IN\_}$ = 0V or V+ (MAX4760A/MAX4761A)	+25°C		0.01		
			T_{MIN} to T_{MAX}			1.0	
		V+ = 5.5V, $V_{IN\_}$ = 1.8V (MAX4760A/MAX4761A)	+25°C		5.5		
			T_{MIN} to T_{MAX}			12	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: UCSP packages are 100% tested at +25°C and limits across the full temperature range are guaranteed by correlation and design. TQFN packages are 100% tested at +85°C and limits across the full temperature range are guaranteed by correlation and design.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design, not production tested.

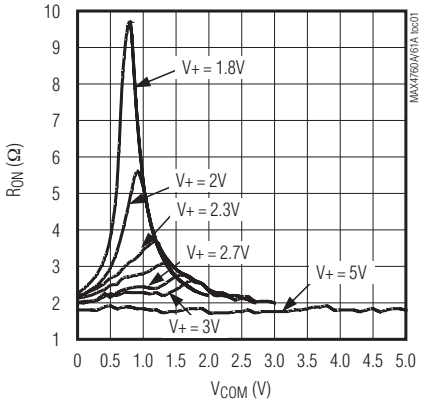
Note 8: Off-isolation = $20\log_{10}$ [$V_{COM\_}$/($V_{NO\_}$ or $V_{NC\_}$)], $V_{COM\_}$ = output, $V_{NO\_}$ or $V_{NC\_}$ = input to off switch.

Note 9: Between any two switches.

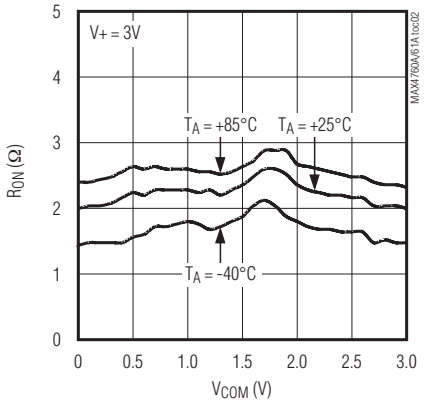
Typical Operating Characteristics

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

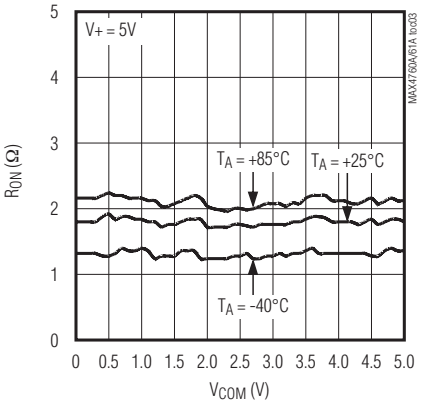
ON-RESISTANCE vs. V_{COM} (MAX4760/MAX4761)



ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (MAX4760/MAX4761)



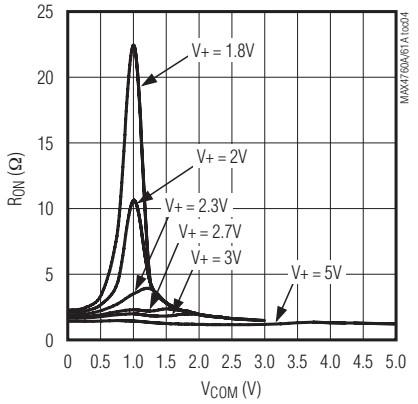
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (MAX4760/MAX4761)



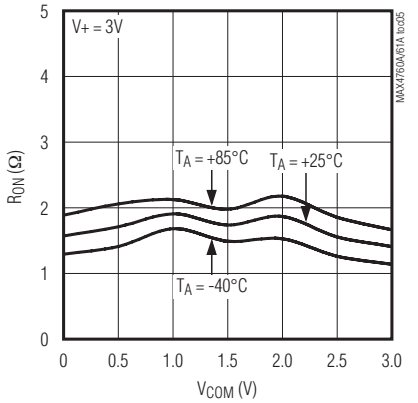
Typical Operating Characteristics (continued)

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

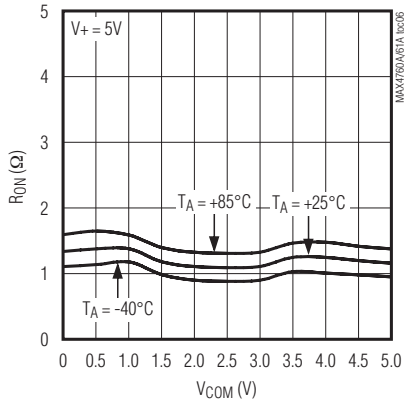
ON-RESISTANCE vs. V_{COM} (MAX4760A/MAX4761A)



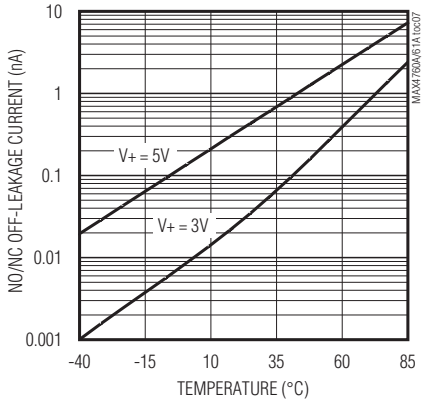
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (MAX4760A/MAX4761A)



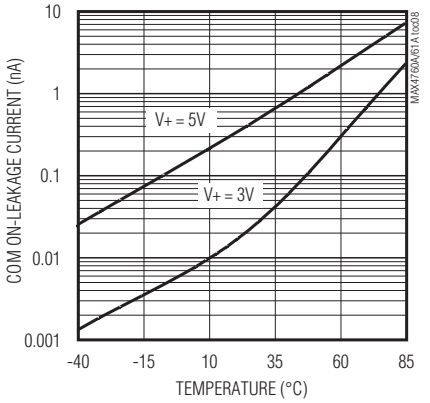
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (MAX4760A/MAX4761A)



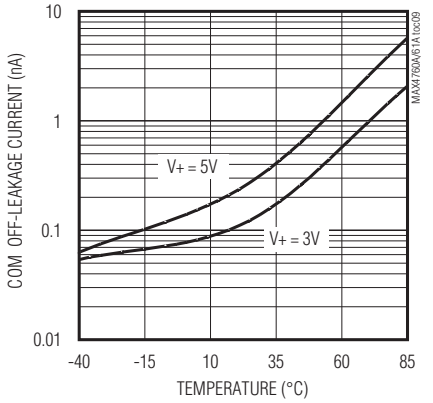
NO/NC OFF-LEAKAGE CURRENT vs. TEMPERATURE



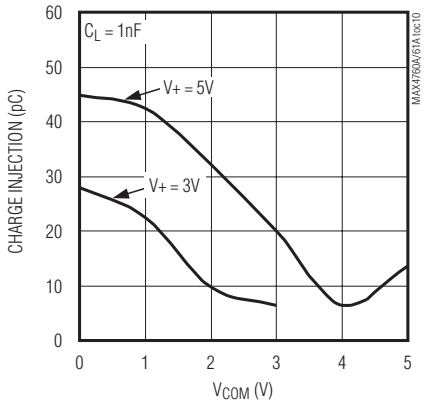
COM ON-LEAKAGE CURRENT vs. TEMPERATURE



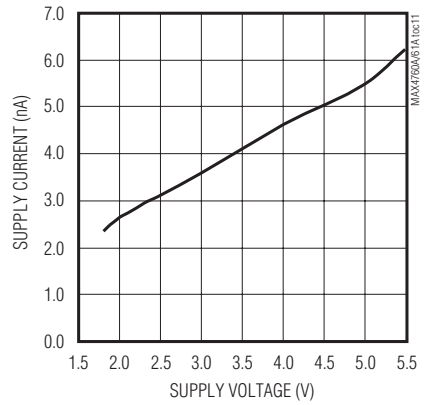
COM OFF-LEAKAGE CURRENT vs. TEMPERATURE



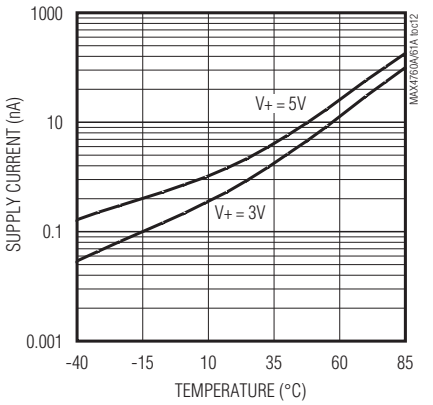
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

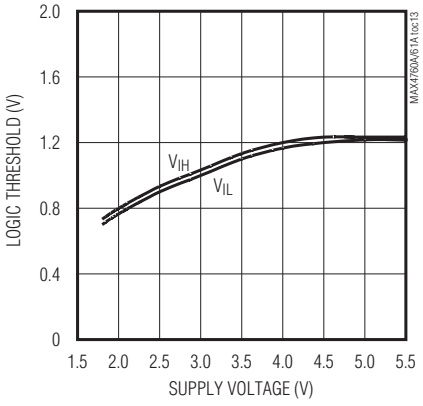


High-Bandwidth, Quad DPDT Switches

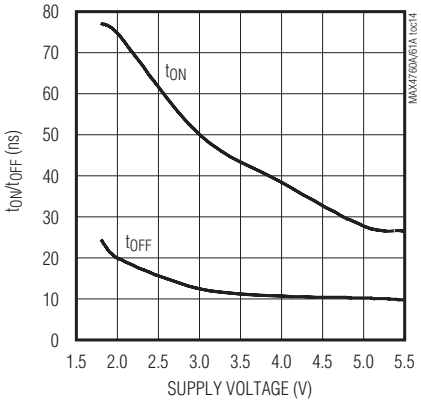
Typical Operating Characteristics (continued)

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

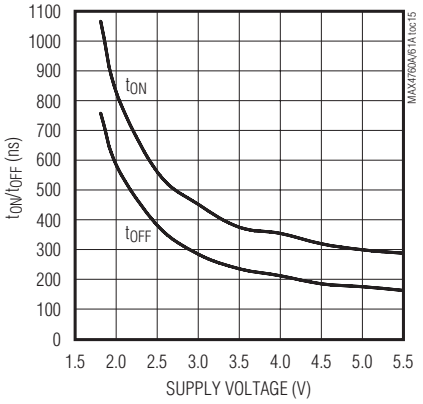
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



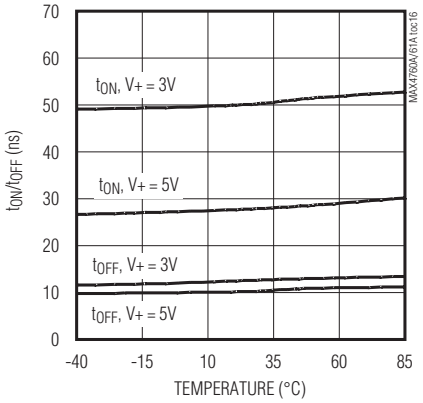
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE (MAX4760/MAX4761)



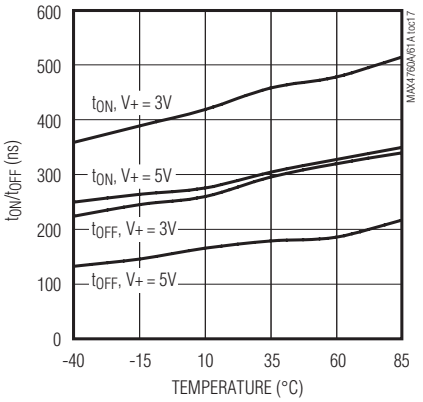
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE (MAX4760A/MAX4761A)



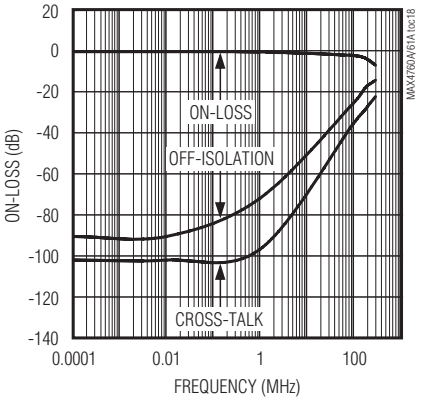
TURN-ON/OFF TIMES vs. TEMPERATURE (MAX4760/MAX4761)



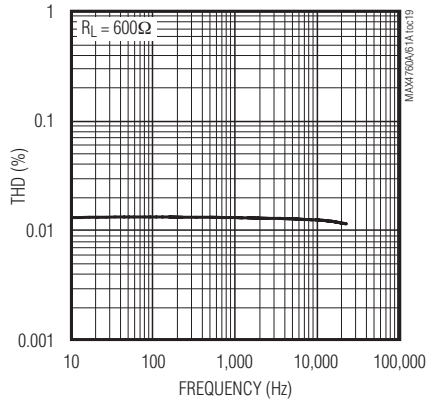
TURN-ON/OFF TIMES vs. TEMPERATURE (MAX4760A/MAX4761A)



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN				NAME	FUNCTION
MAX4760/MAX4760A		MAX4761/MAX4761A			
TQFN-EP	UCSP	TQFN-EP	UCSP		
1	A1	1	A1	NC1	Analog Switch 1, Normally Closed Terminal 1
2	B2	2	B2	COM2	Analog Switch 2, Common Terminal 2
3	A2	3	A2	NC2	Analog Switch 2, Normally Closed Terminal 2
4	A3	4	A3	INA	Logic Control Digital Input for the MAX4760/MAX4760A Switch 1 and Switch 2. Digital control input for all MAX4761/MAX4761A switches.
5	C3, D4	5	C3, D4	V+	Positive Supply Voltage
6	A4	—	—	INB	Logic Control Digital Input for Switches 3 and 4
7	A5	7	A5	NC3	Analog Switch 3, Normally Closed Terminal 3
8	B5	8	B5	COM3	Analog Switch 3, Common Terminal 3
9	A6	9	A6	NC4	Analog Switch 4, Normally Closed Terminal 4
10	B6	10	B6	COM4	Analog Switch 4, Common Terminal 4
11, 14, 17, 29, 32, 35	—	6, 11, 14, 17, 24, 29, 32, 35	A4, F3	N.C.	No Connection. Leave N.C. unconnected.
12	C5	12	C5	NO3	Analog Switch 3, Normally Open Terminal 3
13	C6	13	C6	NO4	Analog Switch 4, Normally Open Terminal 4
15	D6	15	D6	NO8	Analog Switch 8, Normally Open Terminal 8
16	D5	16	D5	NO7	Analog Switch 7, Normally Open Terminal 7
18	E6	18	E6	COM8	Analog Switch 8, Common Terminal 8
19	F6	19	F6	NC8	Analog Switch 8, Normally Closed Terminal 8
20	E5	20	E5	COM7	Analog Switch 7, Common Terminal 7
21	F5	21	F5	NC7	Analog Switch 7, Normally Closed Terminal 7
22	F4	—	—	IND	Logic Control Digital Input for Switches 7 and 8
23	C4, D3	23	C4, D3	GND	Ground
24	F3	—	—	INC	Logic Control Digital Input for Switches 5 and 6
25	F2	25	F2	NC6	Analog Switch 6, Normally Closed Terminal 6
26	E2	26	E2	COM6	Analog Switch 6, Common Terminal 6
27	F1	27	F1	NC5	Analog Switch 5, Normally Closed Terminal 5
28	E1	28	E1	COM5	Analog Switch 5, Common Terminal 5
30	D2	30	D2	NO6	Analog Switch 6, Normally Open Terminal 6
31	D1	31	D1	NO5	Analog Switch 5, Normally Open Terminal 5
33	C1	33	C1	NO1	Analog Switch 1, Normally Open Terminal 1
34	C2	34	C2	NO2	Analog Switch 2, Normally Open Terminal 2
36	B1	36	B1	COM1	Analog Switch 1, Common Terminal 1
—	—	22	F4	$\overline{EN}$	Output Enable, Active Low
—	—	—	—	EP	Exposed Pad (TQFN Only). Connect EP to GND.

High-Bandwidth, Quad DPDT Switches

Detailed Description

The MAX4760/MAX4760A quad double-pole/double-throw (DPDT) and the MAX4761/MAX4761A octal single-pole/double-throw (SPDT) analog switches operate from a single +1.8V to +5.5V supply. These devices are fully specified for +3V applications.

The MAX4760/MAX4760A/MAX4761/MAX4761A have a guaranteed 2.0Ω (typ) on-resistance to switch data or audio signals. The low 54pF (typ) capacitance and 0.2ns change in skew makes them ideal for data switching applications. The MAX4760/MAX4760A have four logic inputs to control two switches in pairs and the MAX4761/MAX4761A have one logic control input and an enable input ($\overline{EN}$) to disable the switches.

Applications Information

Digital Control Inputs

The MAX4760/MAX4760A/MAX4761/MAX4761A logic inputs accept up to +5.5V regardless of the supply voltage. For example, with a +3.3V supply, IN_ can be driven low to GND and high to +5.5V, which allows mixed logic levels in a system. Driving the control logic inputs rail-to-rail also minimizes power consumption.

For the MAX4761/MAX4761A, drive $\overline{EN}$ low to enable. When $\overline{EN}$ is high, COM_ is high impedance.

Analog Signal Levels

Analog signal inputs over the full voltage range (0V to V+) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional so NO_, NC_, and COM_ can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1µF capacitor connected from V+ to GND is adequate for most applications.

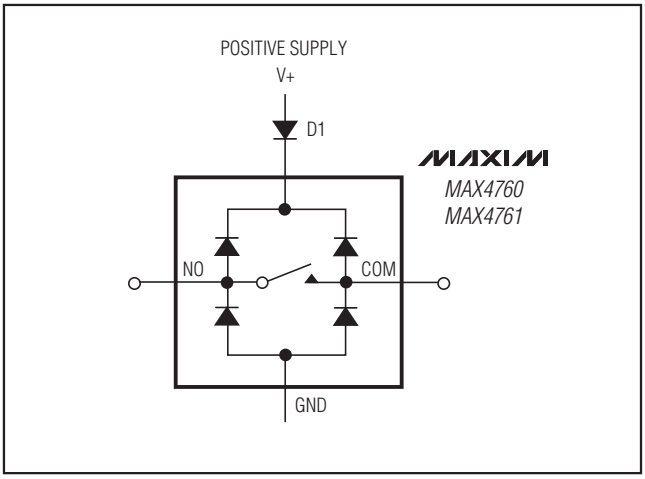


Figure 1. Overvoltage Protection Using an External Blocking Diode

Power-Supply Sequencing

CMOS devices require proper power-supply sequencing. Always apply V+ before the analog signals, especially if the input signal is not current limited. If sequencing is not possible, and the input signal is not current limited to less than 20mA, add a small-signal diode (Figure 1). Adding the diode reduces the analog range to a diode drop (0.7V) below V+ and increases the on-resistance slightly. The maximum supply voltage must not exceed +6V at any time.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications* available on Maxim's website at **www.maxim-ic.com/ucsp**.

Timing Circuits/Timing Diagrams

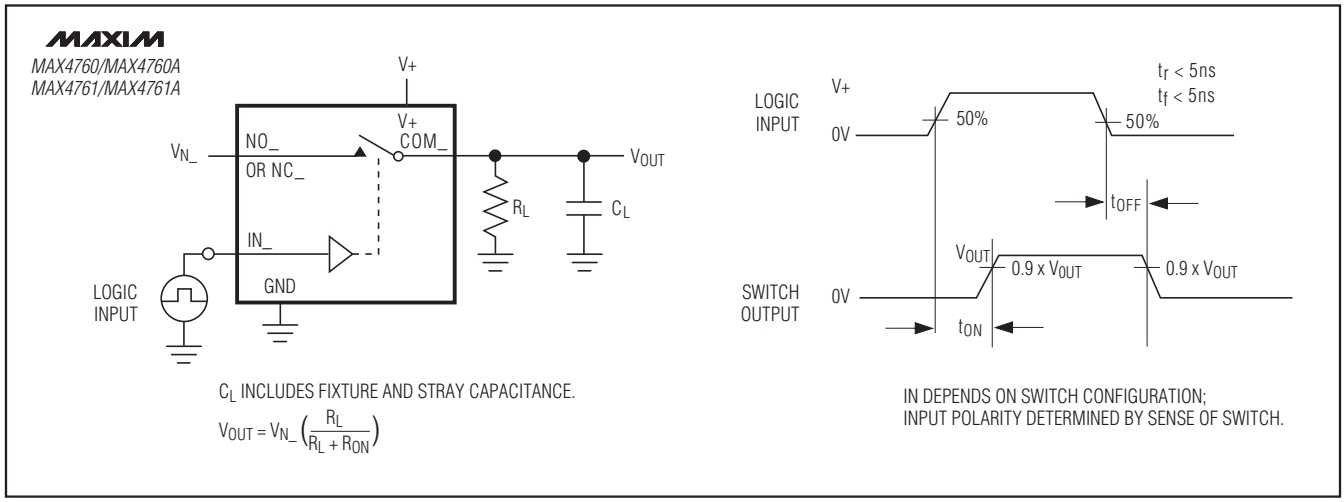


Figure 2. Switching Time

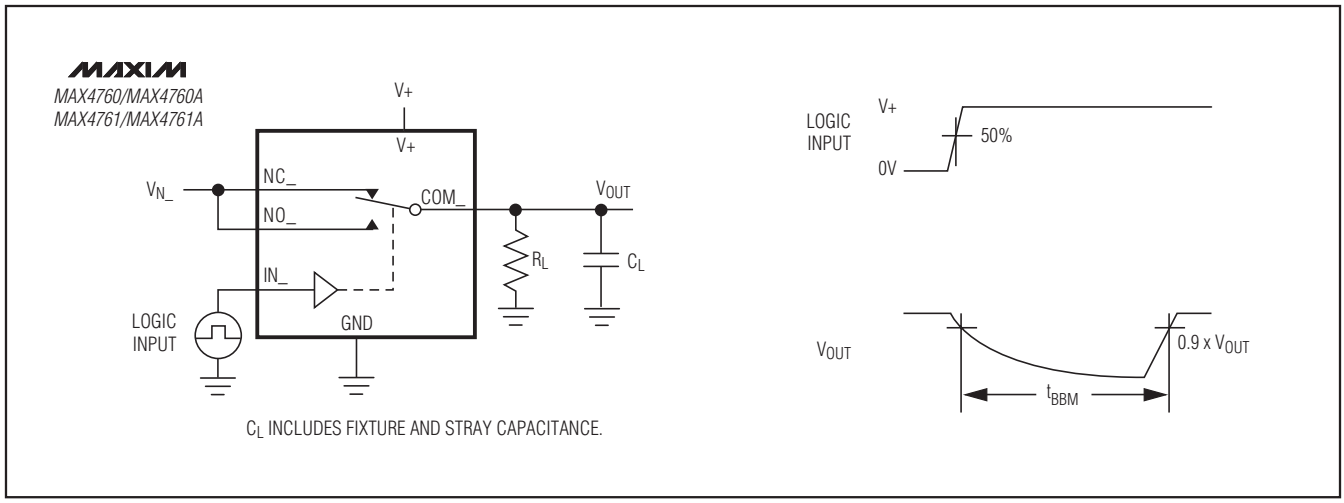
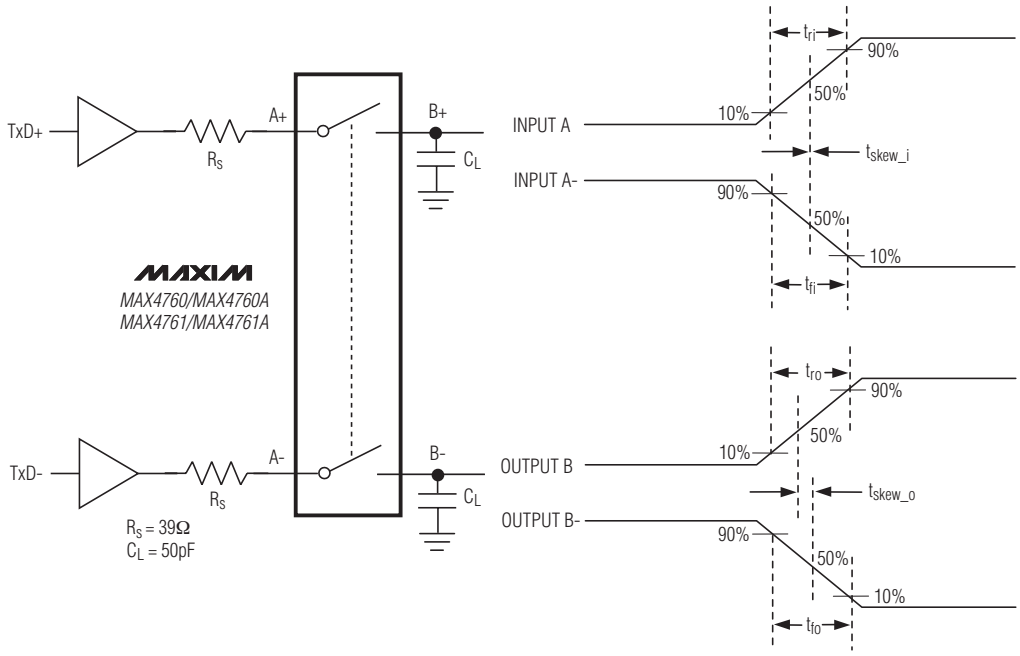


Figure 3. Break-Before-Make Interval

High-Bandwidth, Quad DPDT Switches

Timing Circuits/Timing Diagrams (continued)



$|t_{ro} - t_{ri}|$ DELAY DUE TO SWITCH FOR RISING INPUT AND RISING OUTPUT SIGNALS.

$|t_{fo} - t_{fi}|$ DELAY DUE TO SWITCH FOR FALLING INPUT AND FALLING OUTPUT SIGNALS.

$|t_{skew\_o}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR OUTPUT SIGNALS.

$|t_{skew\_i}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR INPUT SIGNALS.

Figure 4. Input/Output Skew Timing Diagram

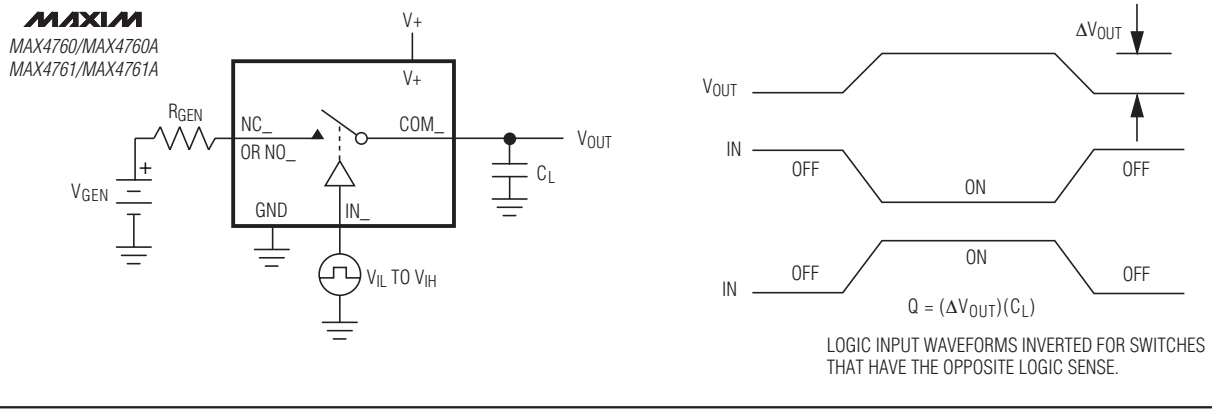


Figure 5. Charge Injection

Timing Circuits/Timing Diagrams (continued)

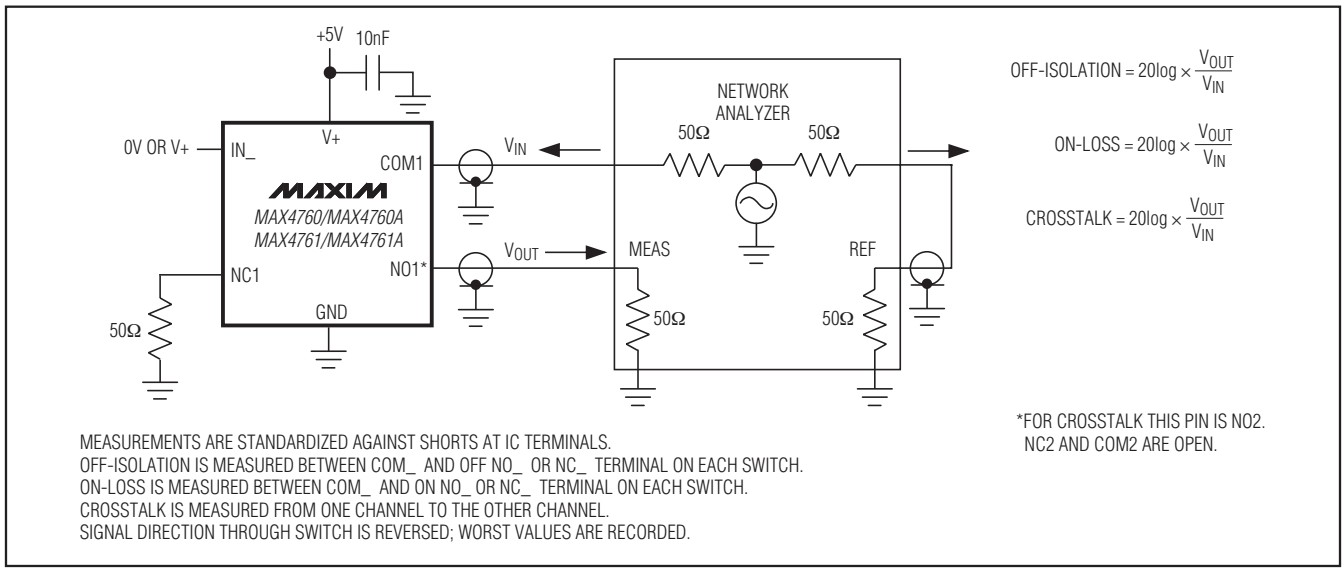


Figure 6. On-Loss, Off-Isolation, and Crosstalk

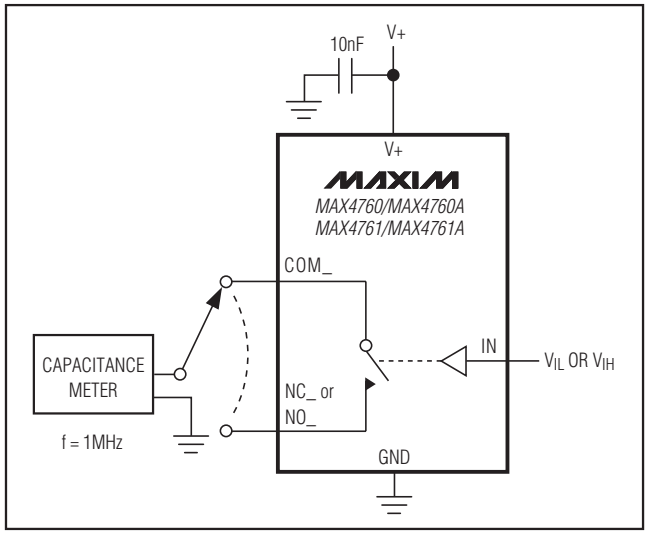
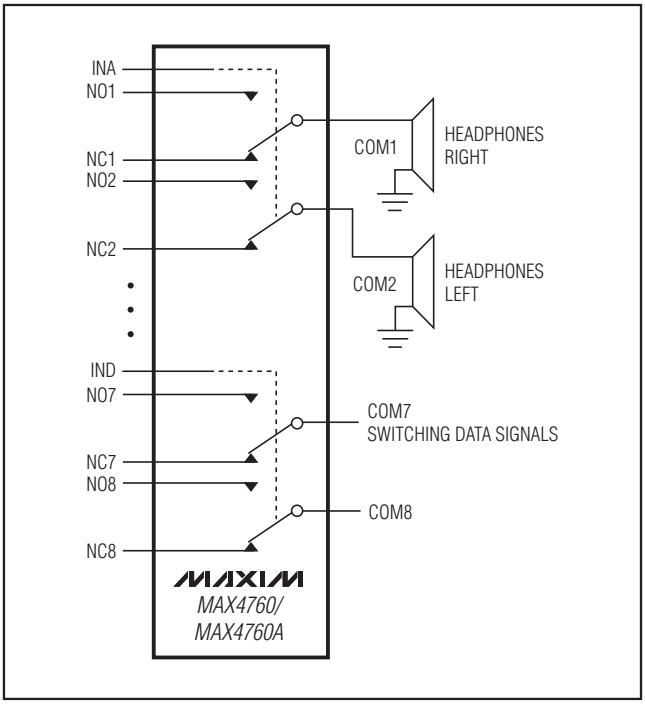


Figure 7. Channel On-/Off-Capacitance

Typical Operating Circuit



High-Bandwidth, Quad DPDT Switches

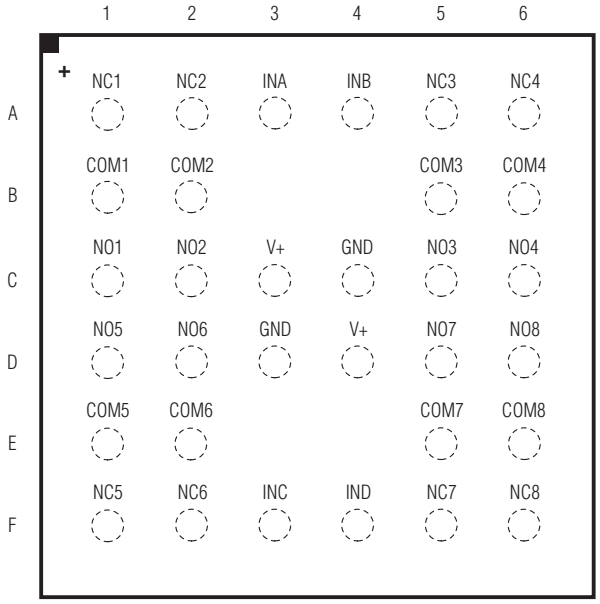
Pin Configurations/Truth Tables

TOP VIEW

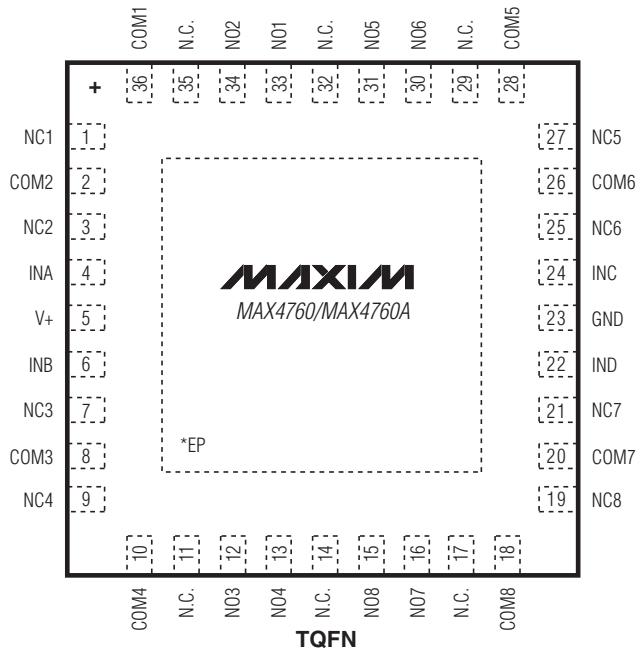
MAXIM

MAX4760/MAX4760A

(BUMP SIDE DOWN)



UCSP



TQFN

*EXPOSED PADDLE CONNECTED TO GND.

MAX4760/MAX4760A

INA	NO1/NO2	NC1/NC2
LOW	OFF	ON
HIGH	ON	OFF
INB	**NO3/NO4**	**NC3/NC4**
LOW	OFF	ON
HIGH	ON	OFF
INC	**NO5/NO6**	**NC5/NC6**
LOW	OFF	ON
HIGH	ON	OFF
IND	**NO7/NO8**	**NC7/NC8**
LOW	OFF	ON
HIGH	ON	OFF

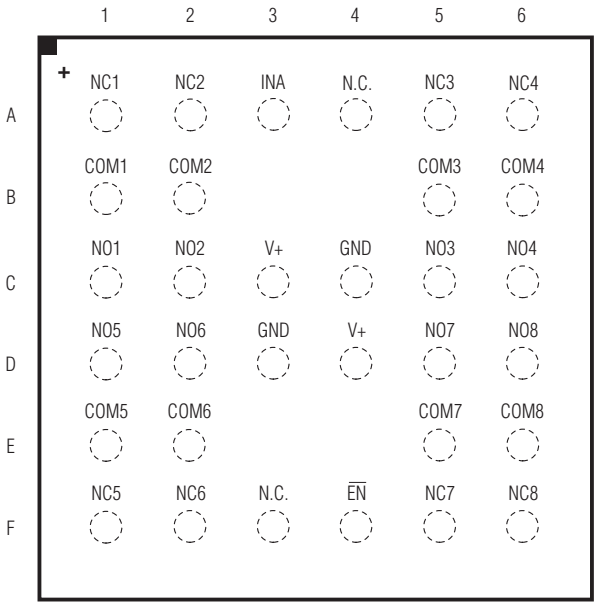
Pin Configurations/Truth Tables (continued)

TOP VIEW

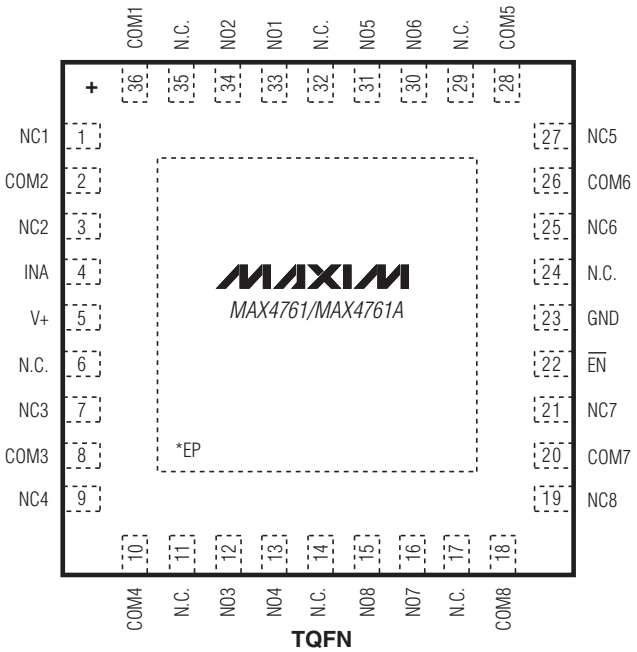
MAXIM

MAX4761/MAX4761A

(BUMP SIDE DOWN)



UCSP



TQFN

*EXPOSED PADDLE CONNECTED TO GND.

MAX4761/MAX4761A

$\overline{EN}$	INA	NO_	NC_
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF
HIGH	X	OFF	OFF

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 UCSP	B36-2	21-0082
36 TQFN-EP	T3666-3	21-0141

High-Bandwidth, Quad DPDT Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	4/07	Addition of MAX4760A/MAX4761A	1–14
5	4/09	Revised *Ordering Information*, *Electrical Characteristics* table, and *Pin Description*.	1, 3, 7

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Maxim Integrated:

MAX4760AEBX+T MAX4760EBX+T MAX4760ETX+ MAX4760ETX+T MAX4760EWX+T MAX4761ETX+ MAX4761ETX+T MAX4760EBX+TW MAX4761EBX-T