

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|--------------|
| Human Body Model (per JESD22-A114) | 1A (Minimum) |
| Machine Model (per EIA/JESD22-A115) | A (Minimum) |
| Charge Device Model (per JESD22-C101) | IV (Minimum) |

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics

| | | | | | |
|---|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 1 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$) | I_{GSS} | — | — | 1 | μAdc |

On Characteristics

| | | | | | |
|--|--------------|---|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 250\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1 | 2 | 3 | Vdc |
| Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 500\ \text{mAdc}$, Measured in Functional Test) | $V_{GS(Q)}$ | 2 | 2.8 | 4 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.2\ \text{Adc}$) | $V_{DS(on)}$ | — | 0.21 | 0.3 | Vdc |

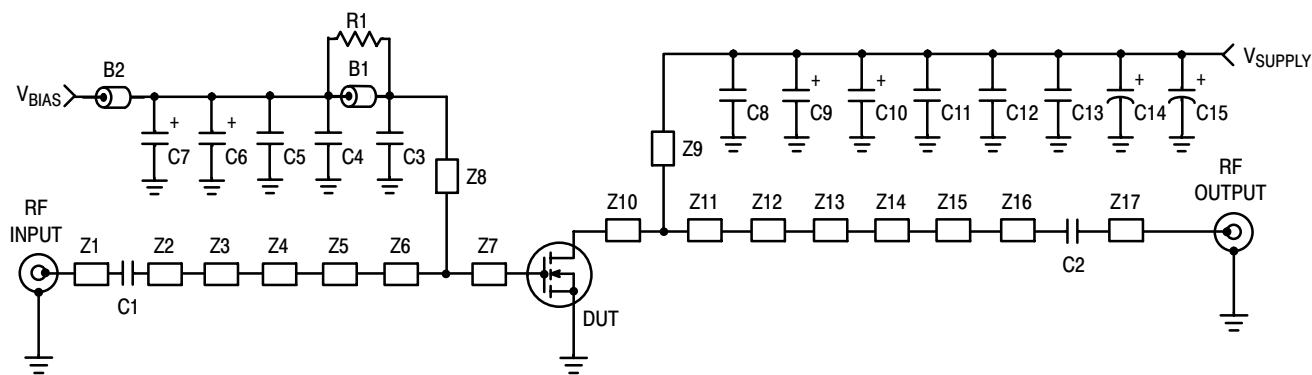
Dynamic Characteristics ⁽¹⁾

| | | | | | |
|--|-----------|---|------|---|----|
| Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$) | C_{rss} | — | 0.83 | — | pF |
| Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$) | C_{oss} | — | 232 | — | pF |

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 500\ \text{mA}$, $P_{out} = 7\ \text{W Avg. W-CDMA}$, $f = 2615\ \text{MHz}$, Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\ \text{MHz}$ Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

| | | | | | |
|------------------------------|----------|------|-------|----|-----|
| Power Gain | G_{ps} | 15 | 16 | 18 | dB |
| Drain Efficiency | η_D | 20.5 | 22.5 | — | % |
| Adjacent Channel Power Ratio | ACPR | -40 | -42.5 | — | dBc |
| Input Return Loss | IRL | — | -10 | — | dB |

1. Part internally matched both on input and output.



| | | | |
|----|----------------------------|-----|--|
| Z1 | 0.748" x 0.081" Microstrip | Z10 | 0.091" x 0.753" Microstrip |
| Z2 | 0.273" x 0.081" Microstrip | Z11 | 0.150" x 0.753" Microstrip |
| Z3 | 0.055" x 0.220" Microstrip | Z12 | 0.153" x 0.543" Microstrip |
| Z4 | 0.090" x 0.440" Microstrip | Z13 | 0.145" x 0.384" Microstrip |
| Z5 | 0.195" x 0.170" Microstrip | Z14 | 0.446" x 0.148" Microstrip |
| Z6 | 0.797" x 0.490" Microstrip | Z15 | 0.130" x 0.425" Microstrip |
| Z7 | 0.082" x 0.490" Microstrip | Z16 | 0.384" x 0.081" Microstrip |
| Z8 | 0.050" x 0.476" Microstrip | Z17 | 0.730" x 0.081" Microstrip |
| Z9 | 0.070" x 0.350" Microstrip | PCB | Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$ |

Figure 1. MRF6S27050HR3(SR3) Test Circuit Schematic

Table 5. MRF6S27050HR3(SR3) Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|----------|--|--------------------|------------------|
| B1 | Ferrite Bead | 2508051107Y0 | Fair-Rite |
| B2 | Ferrite Bead, Short | 2743019447 | Fair-Rite |
| C1, C2 | 4.3 pF Chip Capacitors | ATC100B4R3BT500XT | ATC |
| C3, C8 | 3.6 pF Chip Capacitors | ATC100B3R6BT500XT | ATC |
| C4, C11 | 2.2 μ F, 50 V Chip Capacitors | C1825C225J5RAC | Kemet |
| C5 | 0.01 μ F, 100 V Chip Capacitor | C1825C103J1RAC | Kemet |
| C6 | 22 μ F, 25 V Tantalum Capacitor | T491D226K025AT | Kemet |
| C7 | 47 μ F, 16 V Tantalum Capacitor | T491D476K016AT | Kemet |
| C9, C10 | 10 μ F, 50 V Tantalum Capacitors | T491D106K050AT | Kemet |
| C12, C13 | 1.0 μ F, 50 V Chip Capacitors | GRM32RR71H105KA01B | Murata |
| C14 | 330 μ F, 63 V Electrolytic Capacitor | EMVY630GTR331MMH0S | Nippon Chemi-Con |
| C15 | 47 μ F, 50 V Electrolytic Capacitor | EMVK500ADA470MHA0G | United Chemi-Con |
| R1 | 2.7 Ω , 1/4 W Chip Resistor | CRCW12062R7FKEA | Vishay |

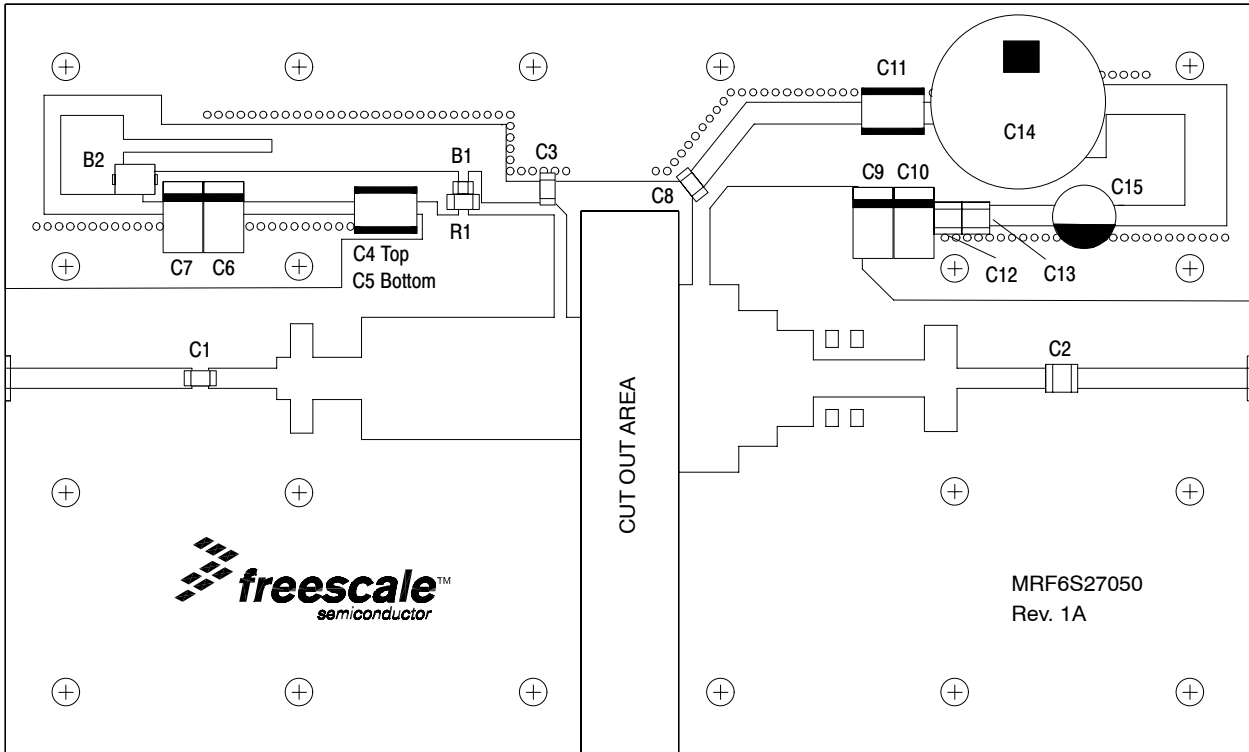


Figure 2. MRF6S27050HR3(SR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

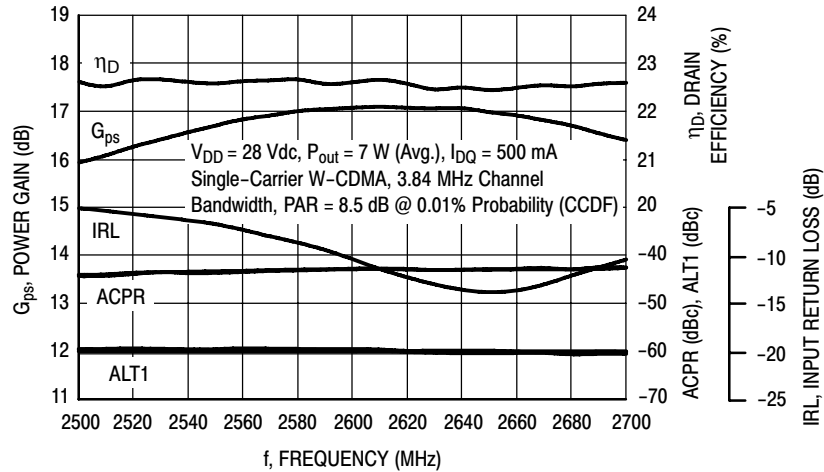


Figure 3. Single-Carrier W-CDMA Broadband Performance @ $P_{out} = 7$ Watts Avg.

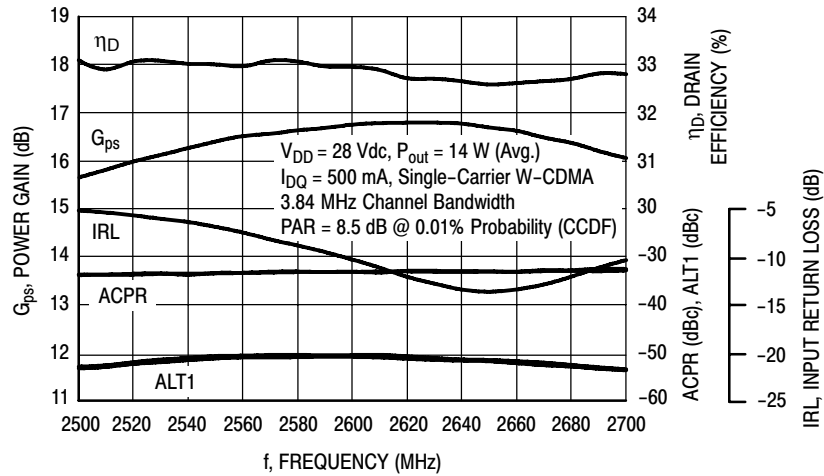


Figure 4. Single-Carrier W-CDMA Broadband Performance @ $P_{out} = 14$ Watts Avg.

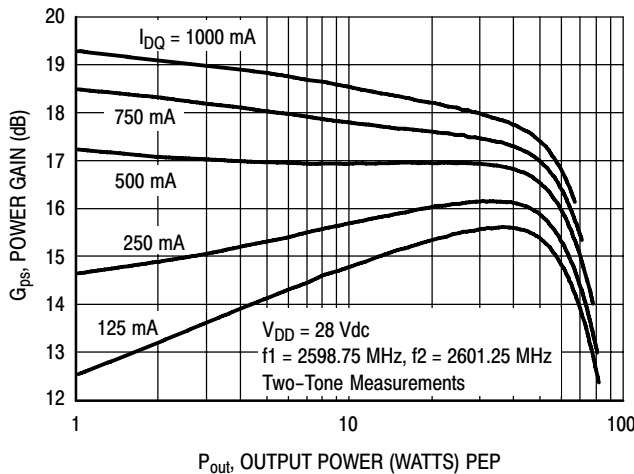


Figure 5. Two-Tone Power Gain versus Output Power

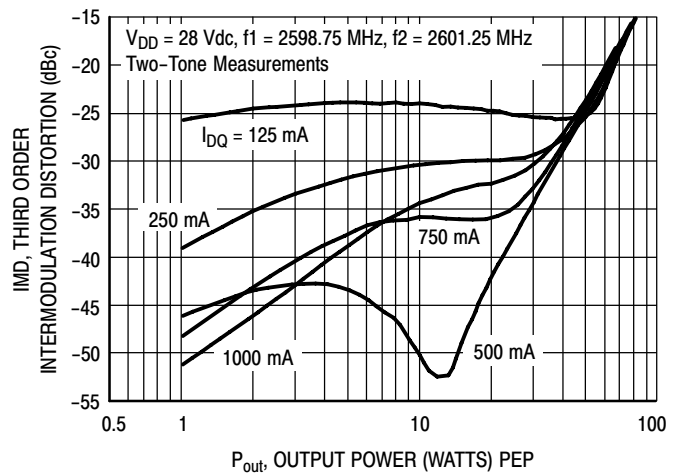


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

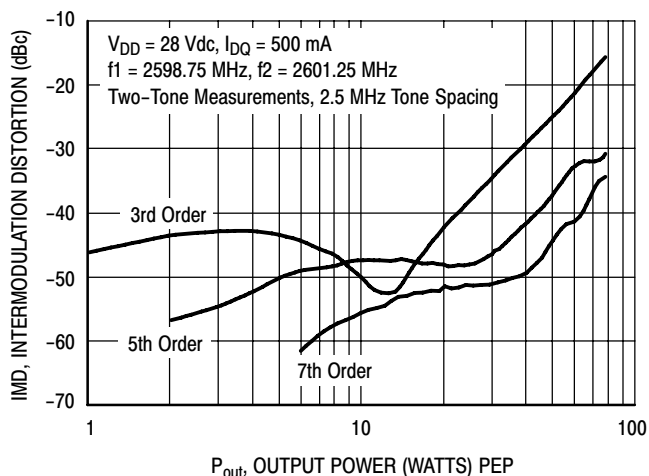


Figure 7. Intermodulation Distortion Products versus Output Power

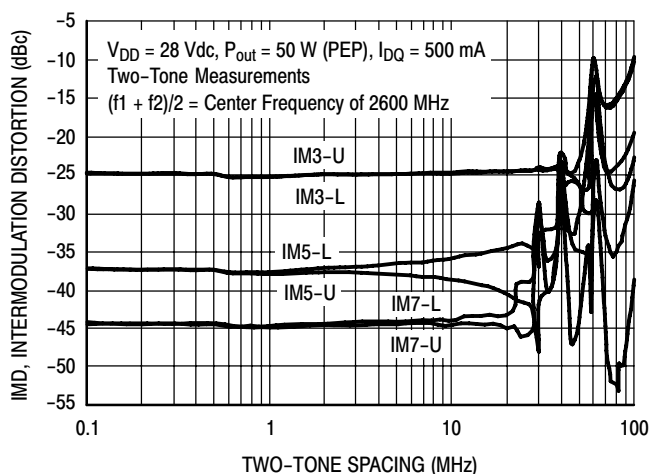


Figure 8. Intermodulation Distortion Products versus Tone Spacing

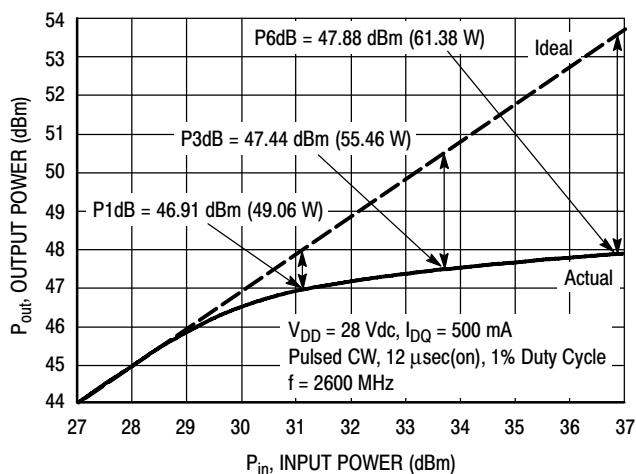


Figure 9. Pulsed CW Output Power versus Input Power

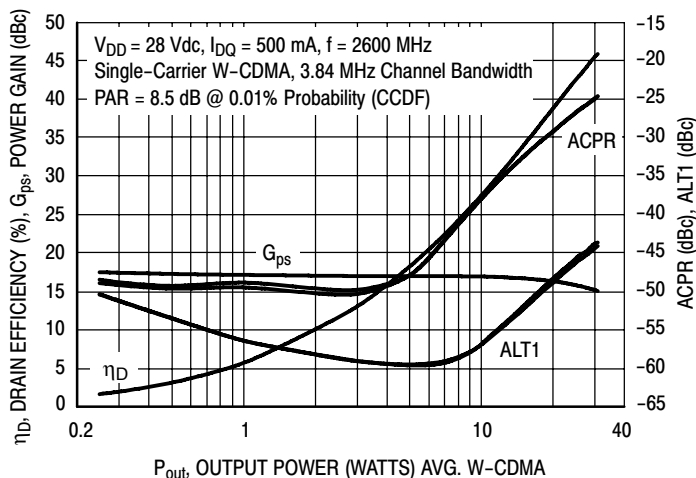


Figure 10. Single-Carrier W-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

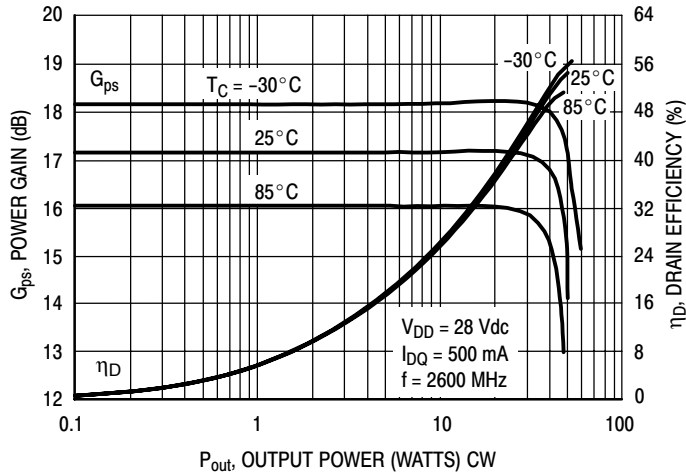


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

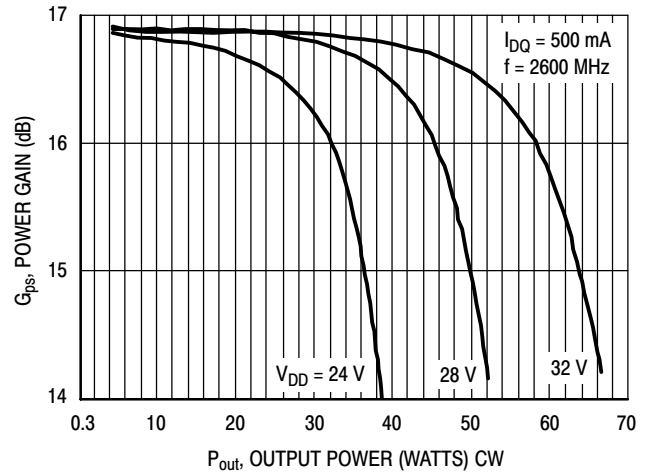


Figure 12. Power Gain versus Output Power

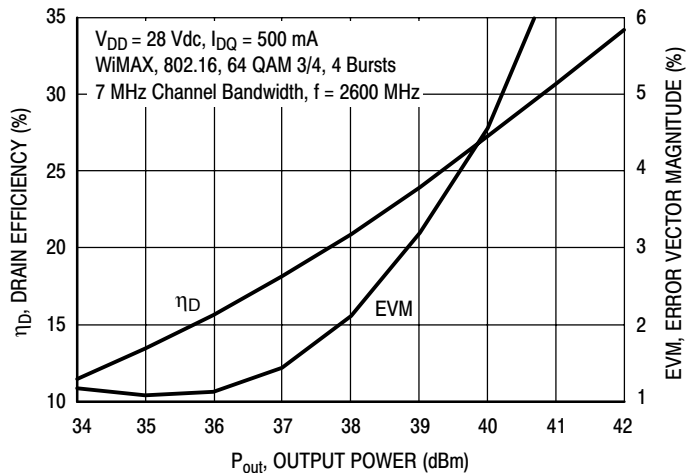
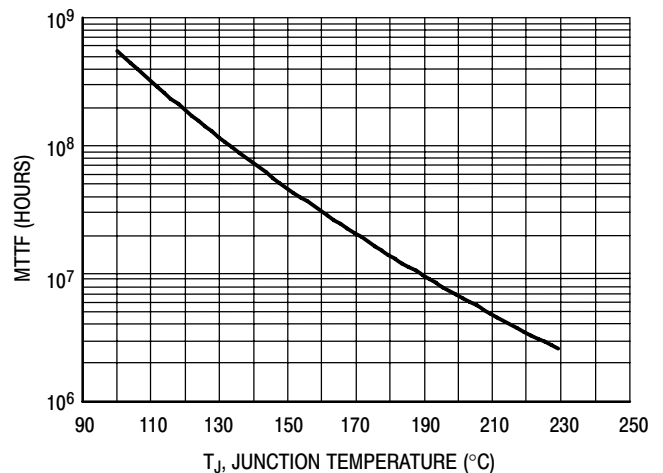


Figure 13. Drain Efficiency and Error Vector Magnitude versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28$ Vdc, $P_{out} = 7$ W Avg., and $\eta_D = 22.5\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 14. MTTF Factor versus Junction Temperature

W-CDMA TEST SIGNAL

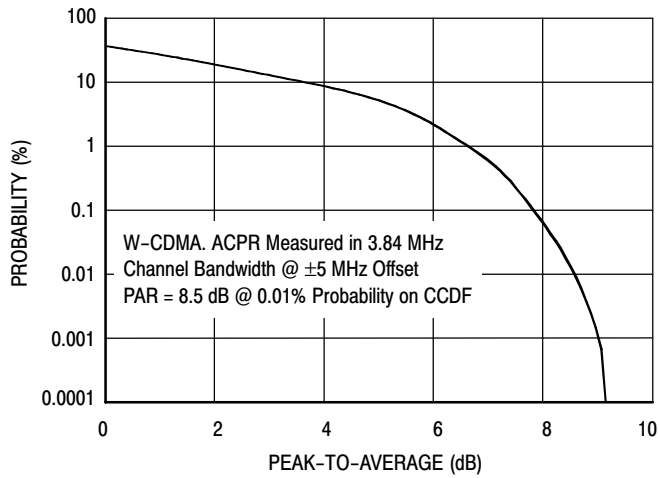


Figure 15. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal

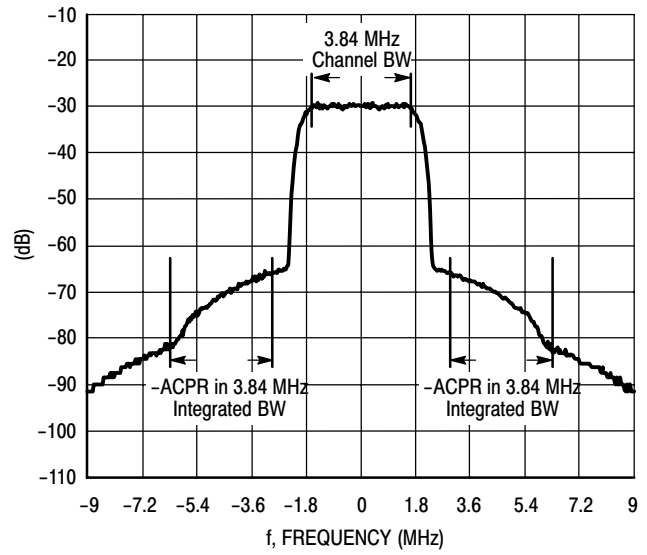
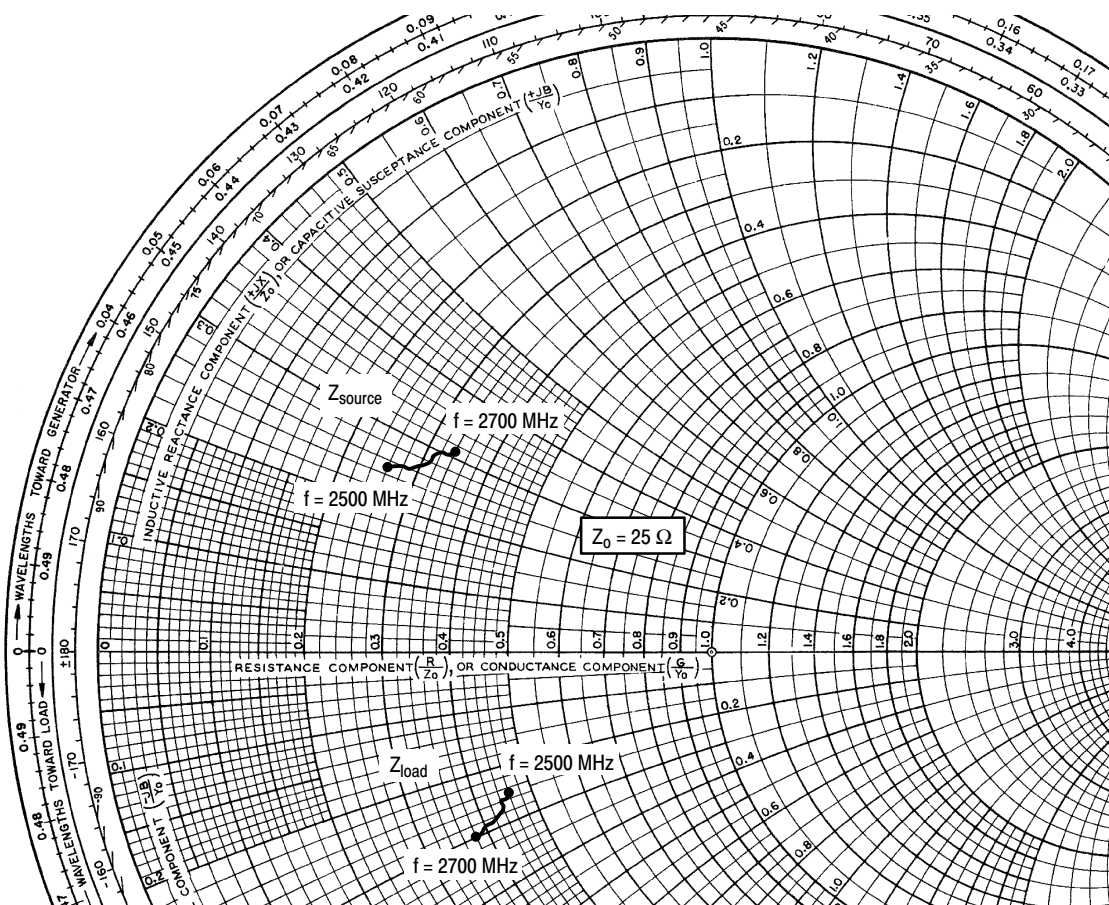


Figure 16. Single-Carrier W-CDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 7 \text{ W Avg.}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 2500 | $6.897 + j6.212$ | $11.524 - j6.193$ |
| 2525 | $7.062 + j6.412$ | $11.325 - j6.396$ |
| 2550 | $7.239 + j6.611$ | $11.110 - j6.594$ |
| 2575 | $7.428 + j6.808$ | $10.880 - j6.783$ |
| 2600 | $7.630 + j7.002$ | $10.634 - j6.962$ |
| 2625 | $7.846 + j7.193$ | $10.373 - j7.130$ |
| 2650 | $8.075 + j7.380$ | $10.098 - j7.283$ |
| 2675 | $8.320 + j7.561$ | $9.810 - j7.420$ |
| 2700 | $8.579 + j7.737$ | $9.511 - j7.541$ |

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

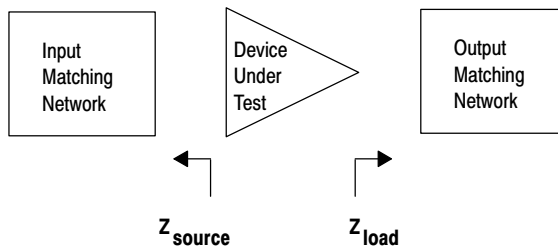
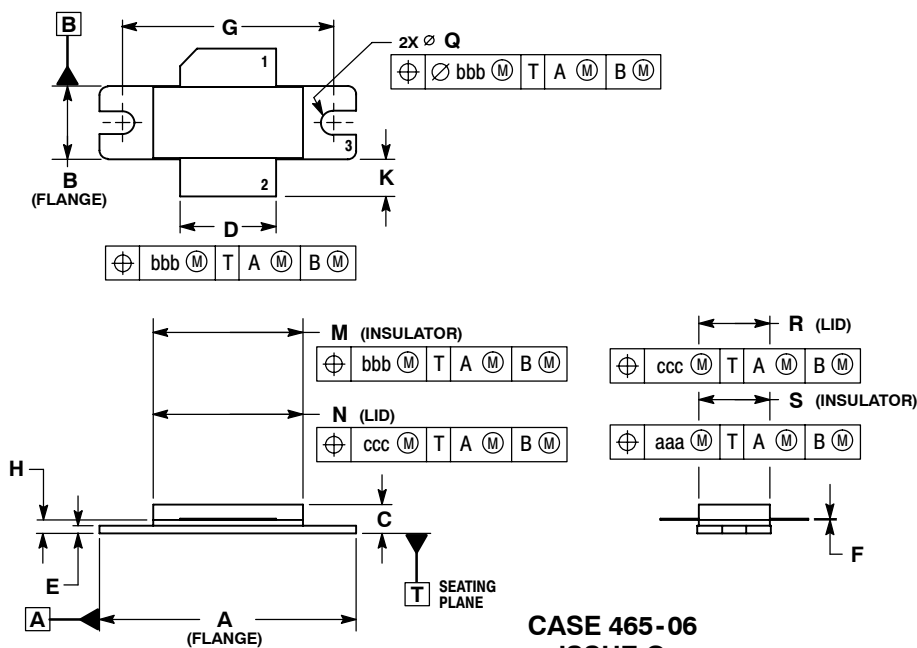


Figure 17. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS

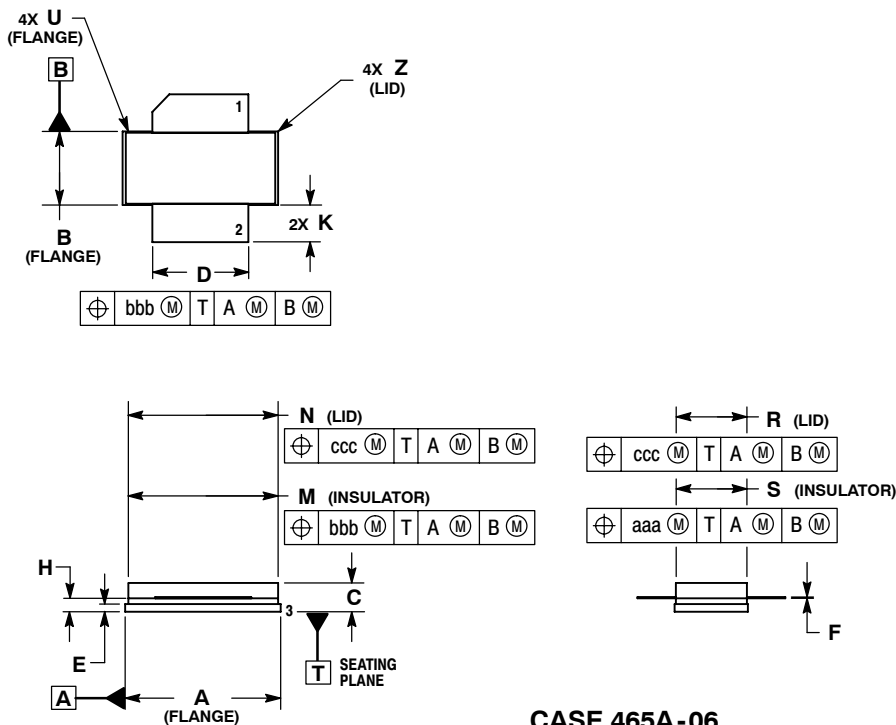


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.335 | 1.345 | 33.91 | 34.16 |
| B | 0.380 | 0.390 | 9.65 | 9.91 |
| C | 0.125 | 0.170 | 3.18 | 4.32 |
| D | 0.495 | 0.505 | 12.57 | 12.83 |
| E | 0.035 | 0.045 | 0.89 | 1.14 |
| F | 0.003 | 0.006 | 0.08 | 0.15 |
| G | 1.100 BSC | | 27.94 BSC | |
| H | 0.057 | 0.067 | 1.45 | 1.70 |
| K | 0.170 | 0.210 | 4.32 | 5.33 |
| M | 0.774 | 0.786 | 19.66 | 19.96 |
| N | 0.772 | 0.788 | 19.60 | 20.00 |
| Q | Ø.118 | Ø.138 | Ø3.00 | Ø3.51 |
| R | 0.365 | 0.375 | 9.27 | 9.53 |
| S | 0.365 | 0.375 | 9.27 | 9.52 |
| aaa | 0.005 REF | | 0.127 REF | |
| bbb | 0.010 REF | | 0.254 REF | |
| ccc | 0.015 REF | | 0.381 REF | |

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465-06
 ISSUE G
 NI-780
 MRF6S27050HR3**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DELETED
 4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.805 | 0.815 | 20.45 | 20.70 |
| B | 0.380 | 0.390 | 9.65 | 9.91 |
| C | 0.125 | 0.170 | 3.18 | 4.32 |
| D | 0.495 | 0.505 | 12.57 | 12.83 |
| E | 0.035 | 0.045 | 0.89 | 1.14 |
| F | 0.003 | 0.006 | 0.08 | 0.15 |
| H | 0.057 | 0.067 | 1.45 | 1.70 |
| K | 0.170 | 0.210 | 4.32 | 5.33 |
| M | 0.774 | 0.786 | 19.61 | 20.02 |
| N | 0.772 | 0.788 | 19.61 | 20.02 |
| R | 0.365 | 0.375 | 9.27 | 9.53 |
| S | 0.365 | 0.375 | 9.27 | 9.52 |
| U | --- | 0.040 | --- | 1.02 |
| Z | --- | 0.030 | --- | 0.76 |
| aaa | 0.005 REF | | 0.127 REF | |
| bbb | 0.010 REF | | 0.254 REF | |
| ccc | 0.015 REF | | 0.381 REF | |

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 5. SOURCE

**CASE 465A-06
 ISSUE H
 NI-780S
 MRF6S27050HSR3**

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|--|
| 0 | Nov. 2006 | <ul style="list-style-type: none">• Initial Release of Data Sheet |
| 1 | Dec. 2008 | <ul style="list-style-type: none">• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2• Removed Lower Thermal Resistance and Low Gold Plating bullets from Features section as functionality is standard, p. 1• Corrected V_{DS} to V_{DD} in the RF test condition voltage callout for $V_{GS(Q)}$, On Characteristics table, p. 2• Updated PCB information to show more specific material details, Fig. 1, Test Circuit Schematic, p. 3• Updated Part Numbers in Table 5, Component Designations and Values, to latest RoHS compliant part numbers, p. 3• Replaced Fig. 14, MTTF versus Junction Temperature with updated graph. Removed Amps² and listed operating characteristics and location of MTTF calculator for device, p. 7 |

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