

AD1362—SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

| Parameter | Test Condition | AD1362KD | | | AD1362SD | | | Units | |
|--|--------------------------------------|-------------|-----|--------|----------|-----|------|--------|-------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| ANALOG INPUTS | | | | | | | | | |
| Input Voltage Range | T_{min} to T_{max} | -10 | | +10 | * | | * | V | |
| Input Bias Current | Per Channel | | | ±50 | | | * | nA | |
| Input Impedance | On Channel | | 10 | | | * | | GΩ | |
| | | | 100 | | | * | | pF | |
| | | Off Channel | 10 | | | | * | GΩ | |
| | | 10 | | | | * | pF | | |
| Input Fault Current | Power Off or On | | | 20 | | | * | mA | |
| Common Mode Rejection | Diff Mode, 1kHz, 20V p-p | 70 | 80 | | * | * | | dB | |
| Mux Crosstalk, Any Off Ch to Any On Ch | 1kHz, 20V p-p | -80 | -90 | | * | * | | dB | |
| Ch to Ch Offset | | | | ±2.5 | | | * | mV | |
| ACCURACY | | | | | | | | | |
| Gain Error | T_{min} to T_{max} | | | ±0.02 | | | * | % FSR | |
| Offset Error | T_{min} to T_{max} | | | ±4 | | | * | mV | |
| Linearity Error | @ 25°C | | | ±0.005 | | | * | % | |
| | T_{min} to T_{max} | | | ±0.01 | | | * | % | |
| Noise Error | 25°C, 0.1 to 1MHz | | | 0.5 | | | * | mV p-p | |
| | T_{min} to T_{max} , 0.1 to 1MHz | | | 1.0 | | | * | mV p-p | |
| TEMPERATURE COEFFICIENTS | | | | | | | | | |
| Gain | T_{min} to T_{max} | | | ±4 | | | ±2 | ppm/°C | |
| Offset | ±10V Range, T_{min} to T_{max} | | | ±2 | | | ±1.5 | ppm/°C | |
| SAMPLE AND HOLD DYNAMICS | | | | | | | | | |
| Aperture Delay | 20V Step to ±0.01% 1kHz | | 150 | 200 | | * | * | ns | |
| Aperture Uncertainty | | | 100 | 500 | | * | * | ps | |
| Acquisition Time | | | | 10 | 18 | | * | * | μs |
| Feedthrough | | | | -80 | -70 | | * | * | dB |
| Droop Rate | | | | 1 | 2 | | * | * | mV/ms |
| Pedestal Voltage | | | -15 | 11 | +15 | | * | * | mV |
| | | | | | | | * | * | |
| POWER SUPPLY REQUIREMENTS | | | | | | | | | |
| +V, Analog Voltage | | +14.25 | | +15.75 | * | | * | V | |
| -V, Analog Voltage | | -14.25 | | -14.75 | * | | * | V | |
| +V, Digital Voltage | | +4.75 | | +5.25 | * | | * | V | |
| +V, Analog Current | | | | 30 | | | * | mA | |
| -V, Analog Current | | | | 30 | | | * | mA | |
| +V, Digital Current | | | | 40 | | | * | mA | |
| Total Power Dissipation | | | 0.5 | 1.1 | | | * | W | |
| TEMPERATURE RANGE | | | | | | | | | |
| Specification | | 0 | | +70 | | -55 | +125 | °C | |
| Storage | | -55 | | +85 | | -55 | +150 | °C | |

DIGITAL INPUT SIGNALS

| Signal | Pins | TTL ¹ | | Logic High | Logic Low |
|-------------------------------|-------|------------------|--|------------------------|--------------|
| | | Loads | | | |
| Input Channel Select | 28-31 | 1LS | | (4-Bit Binary Address) | |
| Channel Select Latch | 32 | 8LS | | Transparent | Latched |
| Single Ended/Diff Mode Select | 1 | 3LS | | Differential | Single Ended |
| Sample-and-Hold Command | 13 | 2LS | | Hold | Sample |

NOTE

¹One TTL Load is defined as $I_{IL} = -1.6\text{mA max @ } V_{IL} = 0.4\text{V}$, $I_{IH} = 40\mu\text{A max @ } V_{IH} = 2.4\text{V}$. One LSTTL Load is defined as $I_{IL} = -0.36\text{mA @ } V_{IL} = 0.4\text{V}$, $I_{IH} = 20\mu\text{A max @ } V_{IH} = 2.7\text{V}$.

*Specifications same as AD1362KD.

ABSOLUTE MAXIMUM RATINGS

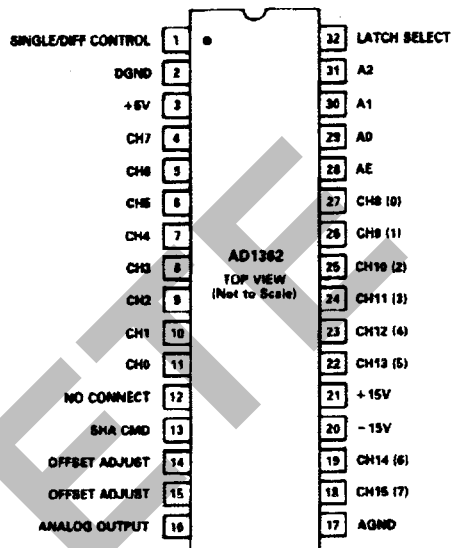
| | | | |
|--------------------|------------|---------------------------|------------------------------|
| +V, Digital Supply |+5.5V | V _{IN} , Signal |±V Analog Supply |
| +V, Analog Supply |+17V | V _{IN} , Digital |0 to +V, Digital Supply |
| -V, Analog Supply |-17V | AGND to DGND |±1V |

ORDERING GUIDE

| Model | Temperature Range | Max Gain TC | Package Option* |
|---------------|-------------------|-------------|-----------------|
| AD1362KD | 0 to +70°C | ±4ppm/°C | DH-32E |
| AD1362SD | -55°C to +125°C | ±2ppm/°C | DH-32E |
| AD1362SD/883B | -55°C to +125°C | ±2ppm/°C | DH-32E |

*DH-32E = Bottom Brazed Ceramic DIP.

PIN ASSIGNMENTS



| Function | Number | Description |
|---------------------|--------|--|
| Single/Diff Control | 1 | Mode Select, Differential or Single Ended |
| DGND | 2 | Digital Ground |
| +5V | 3 | Digital Power Supply, +5V dc |
| Ch 7 | 4 | "High" Analog Input Channel 7 |
| Ch 6 | 5 | "High" Analog Input Channel 6 |
| Ch 5 | 6 | "High" Analog Input Channel 5 |
| Ch 4 | 7 | "High" Analog Input Channel 4 |
| Ch 3 | 8 | "High" Analog Input Channel 3 |
| Ch 2 | 9 | "High" Analog Input Channel 2 |
| Ch 1 | 10 | "High" Analog Input Channel 1 |
| Ch 0 | 11 | "High" Analog Input Channel 0 |
| NC | 12 | No Connect |
| SHA Cmd | 13 | Sample/Hold Control Input to SHA |
| Offset Adjust | 14 | Offset Adjustment Input #1 |
| Offset Adjust | 15 | Offset Adjustment Input #2 |
| Analog Output | 16 | Analog Output to ADC |
| AGND | 17 | Analog Ground |
| Ch 15 | 18 | "High" ("Low") Analog Input Channel 15 (7) |
| Ch 14 | 19 | "High" ("Low") Analog Input Channel 14 (6) |
| -15V | 20 | Negative Analog Power Supply -15V dc |
| +15V | 21 | Positive Analog Power Supply +15V dc |
| Ch 13 | 22 | "High" ("Low") Analog Input Channel 15 (5) |
| Ch 12 | 23 | "High" ("Low") Analog Input Channel 14 (4) |
| Ch 11 | 24 | "High" ("Low") Analog Input Channel 13 (3) |
| Ch 10 | 25 | "High" ("Low") Analog Input Channel 12 (2) |
| Ch 9 | 26 | "High" ("Low") Analog Input Channel 11 (1) |
| Ch 8 | 27 | "High" ("Low") Analog Input Channel 10 (0) |
| AE | 28 | Input Channel Address MSB |
| A0 | 29 | Input Channel Address Bit 0 |
| A1 | 30 | Input Channel Address Bit 1 |
| A2 | 31 | Input Channel Address Bit 2 |
| Latch Select | 32 | Channel Select Latch Control Input |

AD1362

FUNCTIONAL DESCRIPTION

The AD1362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high speed output buffer, channel address latches and control logic as shown in the block diagram. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD1362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD1362 to perform in either mode without external hard-wire interconnections. Of more significance is

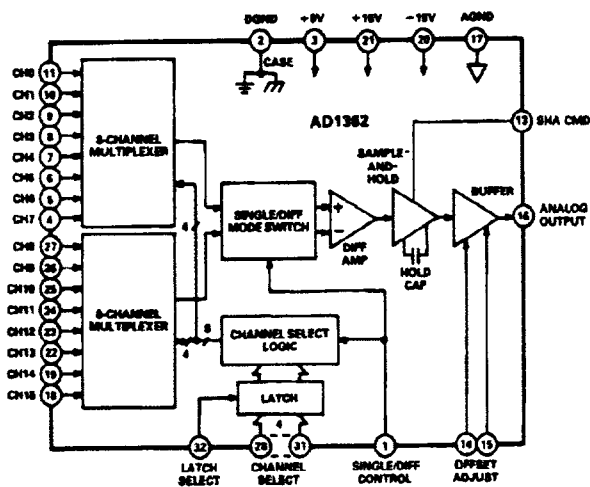
the ability to serve a mixture of both single-ended and differential sources with a single AD1362 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Latch Select input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Latch Select input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes.

The sample-and-hold is a high speed device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD1362 may drive a fast, unbuffered, precision ADC without loss of accuracy.



AD1362 Block Diagram

THEORY OF OPERATION

Concept

The AD1362 is intended to be used in conjunction with a high speed, precision analog-to-digital converter to form a complete data acquisition system (DAS). Figure 1 shows a general AD1362 with ADC DAS application.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

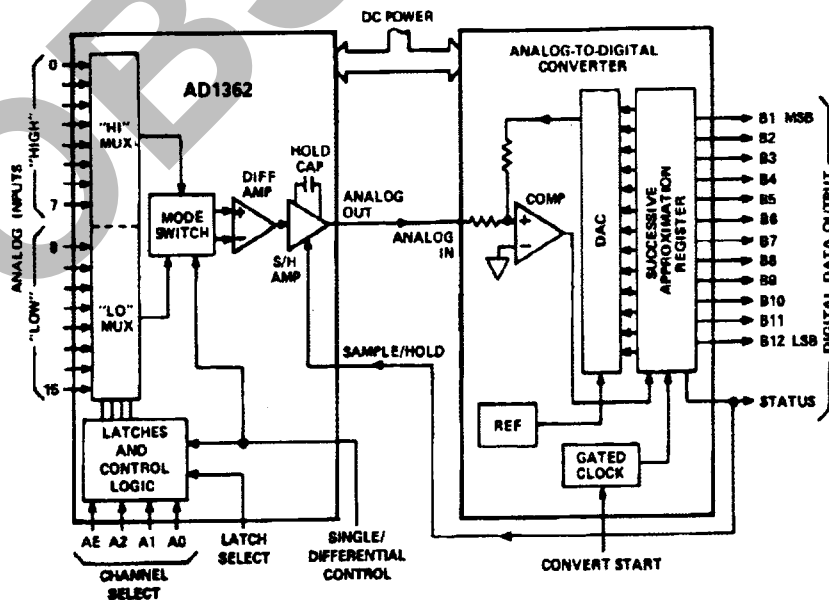


Figure 1. AD1362 with ADC as a Complete Data Acquisition System

System Timing

Figure 2 is a timing diagram for the AD1362 connected as shown in Figure 1 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12-bit type such as the AD573 or AD ADC80.

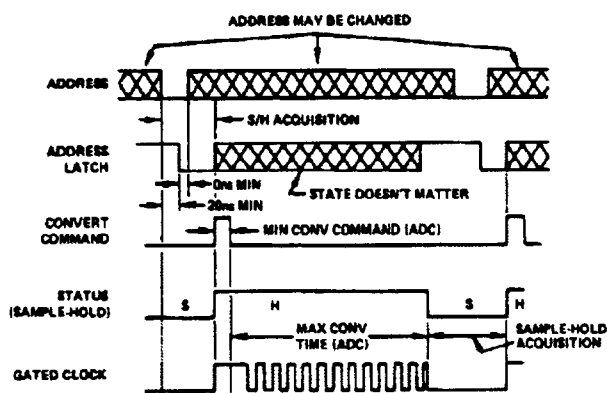


Figure 2. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status Line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy," the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0." The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full scale (different channels may have widely-varying data), the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

NOTE

Valid Output Data

Nor all ADCs have all data bits available when Status indicates that the conversion is complete. Some successive approximation ADCs must have a Status delay built in or the final data bit will lag Status. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external delay or use of an ADC with a valid Status output is necessary to prevent this problem.

Single-Ended/Differential Mode Control

The AD1362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to Pin 1:

- "0": Single-Ended (16 channels)
- "1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output to settle to within $\pm 0.01\%$ of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Channel Select address bits, AE, A0, A1, A2 (Pins 28-31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1, and A2; AE must be enabled with a Logic "1." Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

When the channel address is changed, six microseconds must be allowed for the AD1362 to settle to within $\pm 0.01\%$ of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

AD1362

| ADDRESS | | | | ON CHANNEL | | |
|---------|----|----|----|--------------|--------------|------|
| AE | A2 | A1 | A0 | Single Ended | Differential | |
| | | | | | "Hi" | "Lo" |
| 0 | 0 | 0 | 0 | 0 | None | |
| 0 | 0 | 0 | 1 | 1 | None | |
| 0 | 0 | 1 | 0 | 2 | None | |
| 0 | 0 | 1 | 1 | 3 | None | |
| 0 | 1 | 0 | 0 | 4 | None | |
| 0 | 1 | 0 | 1 | 5 | None | |
| 0 | 1 | 1 | 0 | 6 | None | |
| 0 | 1 | 1 | 1 | 7 | None | |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 |
| 1 | 0 | 0 | 1 | 9 | 1 | 1 |
| 1 | 0 | 1 | 0 | 10 | 2 | 2 |
| 1 | 0 | 1 | 1 | 11 | 3 | 3 |
| 1 | 1 | 0 | 0 | 12 | 4 | 5 |
| 1 | 1 | 0 | 1 | 13 | 5 | 5 |
| 1 | 1 | 1 | 0 | 14 | 6 | 6 |
| 1 | 1 | 1 | 1 | 15 | 7 | 7 |

Table 1. Input Channel Addressing Truth Table

Input Channel Address Latch

The AD1362 is equipped with a latch for the input Channel Select address bits. If the Latch Select pin is at Logic "1," input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input is normally connected to the Status output from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1" putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within $\pm 0.01\%$ of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD1362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Data Acquisition System. An example of such a case would be if the input signals were small ($< 10\text{mV}$) relative to AD1362 offset and gain errors. To adjust the offset of the AD1362, the circuit shown in Figure 3 is recommended.

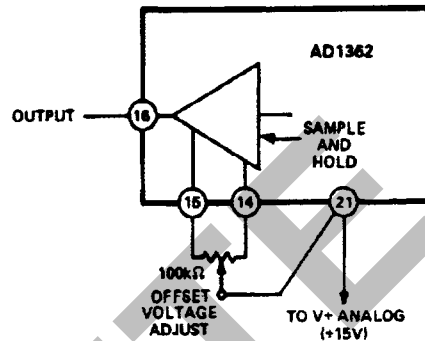


Figure 3. AD1362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground and Digital Ground are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD1362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD1362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 4. This will protect the AD1362 from possible damage caused by voltages in excess of ± 1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as $\pm 200\text{mV}$ between grounds; however, this difference will be reflected directly as an input offset voltage.

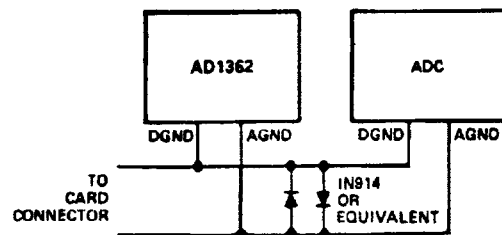


Figure 4. Ground-Fault Protection Diodes

Power Supply Bypassing: The $\pm 15V$ and $+5V$ power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. One microfarad tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disk capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a $0.039\mu F$ ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD1362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

Complete system throughput performance is determined by combining the worst-case specifications of the AD1362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD1362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD1362 and an AD574 12-bit, micro-processor compatible, low cost ADC. Each is specified as a complete, two-package system.

Figure 5a shows the AD1362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

Figure 5b shows a 10-bit application based on the AD1362 and the AD573, a complete low cost 10-bit, 25-microsecond ADC. In this case, one of the above requirements is not met:

1. \overline{DR} ($\overline{DATA\ READY}$), as Status, is positive-true, but . . .
2. \overline{DR} does not indicate that a conversion is in progress until $1.5\mu s$ after conversion starts.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD1362. CC must last for more than $1.5\mu s$ so that \overline{DR} may then assume control of Hold.

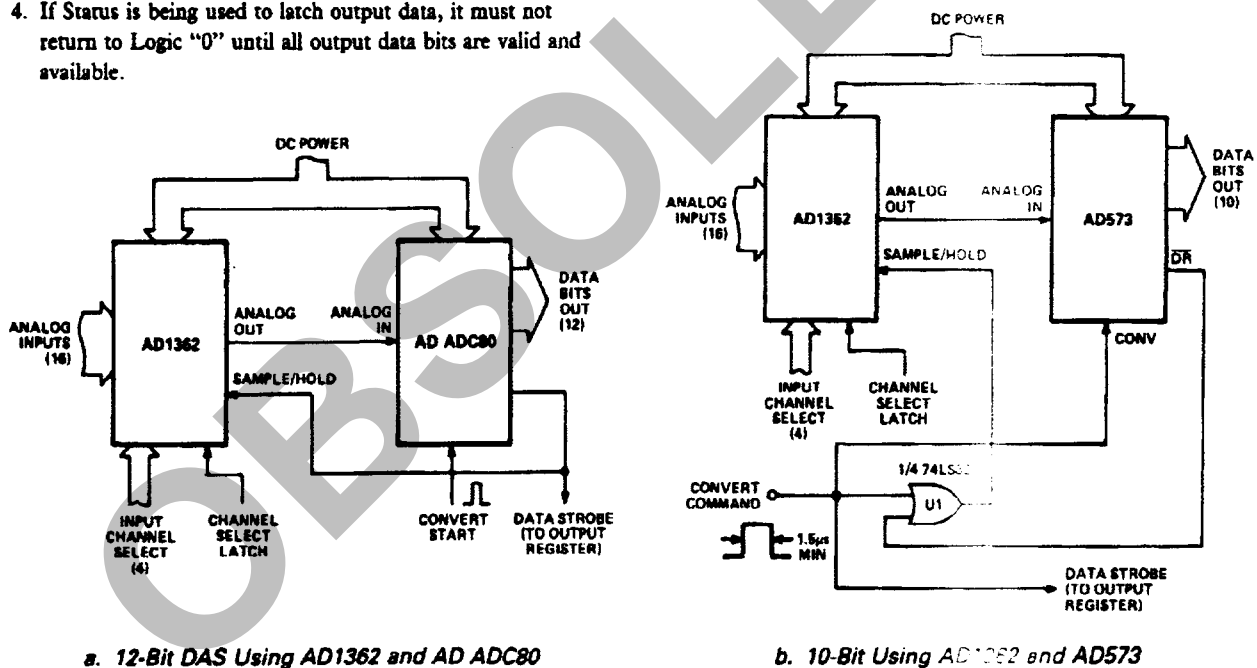
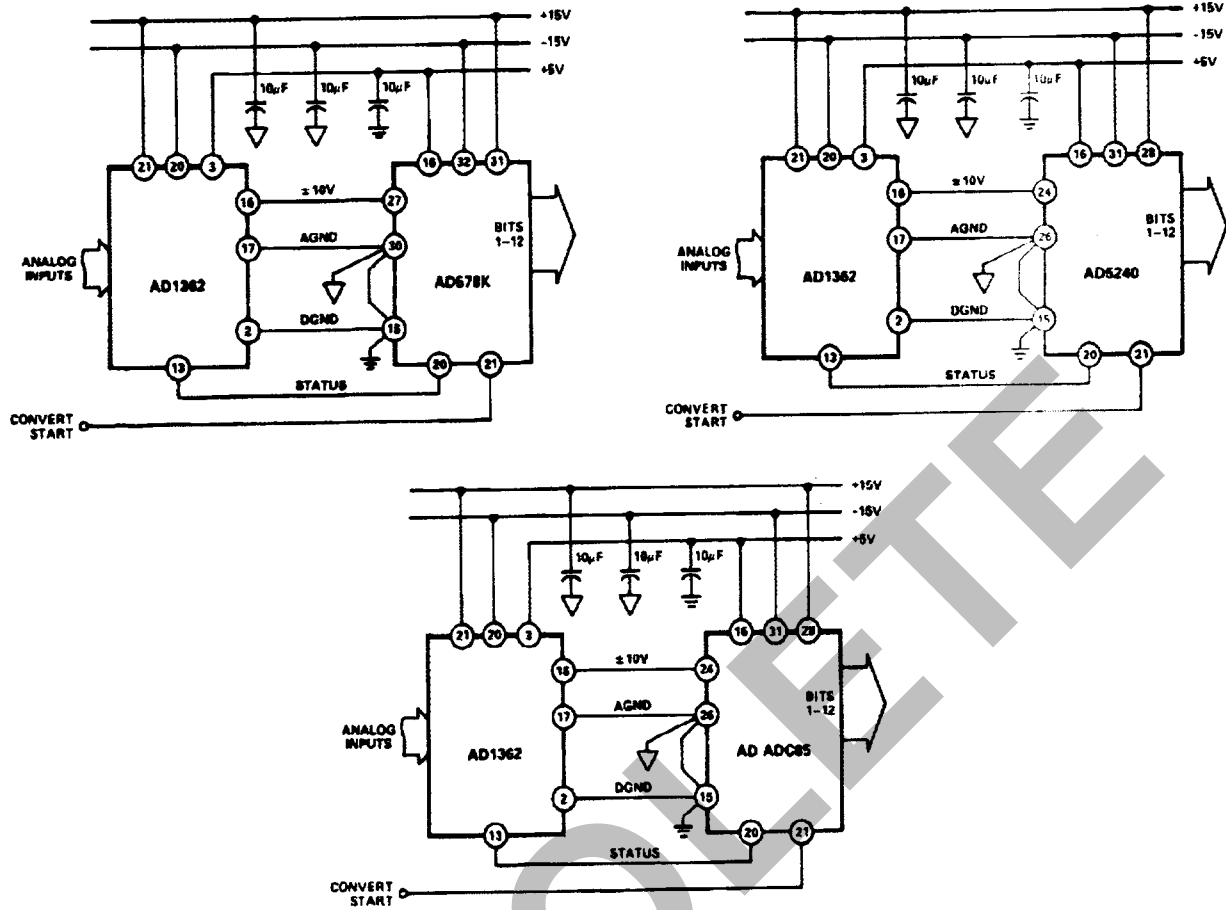


Figure 5. Data Acquisition Systems Based on the AD1362 and Popular ADCs

AD1362

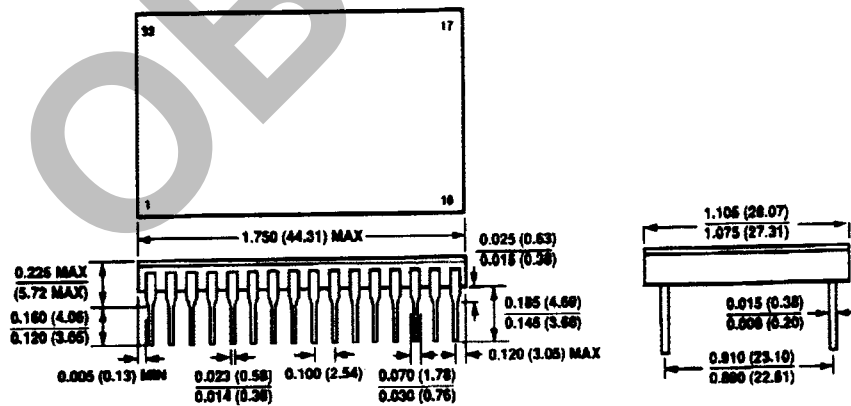


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Figure 6. High Speed Data Acquisition Systems Based on AD1362 and Fast ADCs.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



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