Electrical Specifications, *(continued)*

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Output					
RF Frequency Range		4.0		7.0	GHz
RF Return Loss			8		dB
LO Input					
LO Frequency Range		4.0		7.0	GHz
LO Input Power		-3	+3	+9	dBm
LO Port Return Loss			10		dB
Baseband Input Port (Note 1)					
Baseband Port Bandwidth	With 50Ω source & external 10 pF shunt cap to ground. Refer to HMC496LP3 Application Circuit.	DC		250	MHz
Baseband Input DC Voltage (Vbbdc)	This parameter can be varied in order to optimize the device performance over temperature and/or supply.	1.0	1.3	1.6	V
Baseband Input DC Bias Current (Ibbdc)	Single-ended		32		µA
Baseband Input Capacitance	Single-ended. De-embeded to the part pin.		0.8		pF
DC Power Requirements	See Test Conditions Below				
Supply Voltage (Vcc)		2.7	3.0	3.3	V
Supply Current (Icc)			93		mA

Test Conditions: *Unless Otherwise Specified, the Following Test Conditions Were Used*

Parameter	Condition
Temperature	+25 °C
Baseband Input Frequency	200 kHz
Baseband Input DC Voltage (Vbbdc)	1.3V
Baseband Input AC Voltage (Peak to Peak Differential, I and Q)	1.2V
Baseband Input AC Voltage for OIP3 Measurement (Peak to Peak Differential, I and Q)	600 mV per tone @ 150 & 250 kHz
Frequency Offset for Output Noise Measurements	20 MHz
Supply	+3.0V
LO Input Power	+3 dBm
LO Input Mode	Single-Ended
Mounting Configuration	Refer to HMC496LP3 Application Schematic Herein
Sideband & Carrier Suppression	Uncalibrated
RF Output Mode	Differential

Calibrated vs. Uncalibrated Test Results

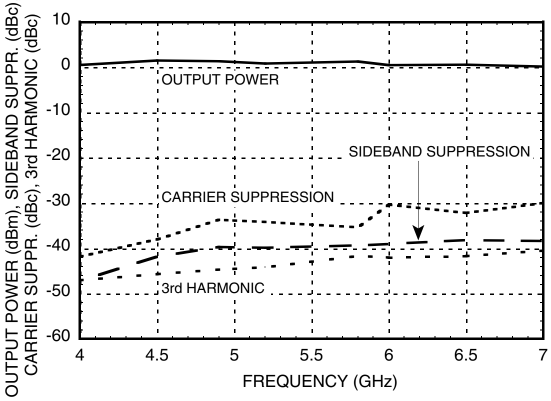
During the Uncalibrated Sideband and Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The "Uncalibrated, +25 °C" Sideband and Carrier Suppression plots were measured at room temperature, while the "Uncalibrated, over Temperature" Sideband and Carrier Suppression plots represent the worst case uncalibrated suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

The "Calibrated, +25 °C" Sideband Suppression data was plotted after a manual adjustment of the I/Q amplitude balance and I/Q phase offset (skew) at +25C, and an LO input power level of + 3 dBm. This adjustment setting was held constant during tests over LO input power level and temperature. The "Calibrated, over Temperature" plots represent the worst case calibrated Sideband Suppression levels at T= -40 °C, +25 °C, and +85 °C.

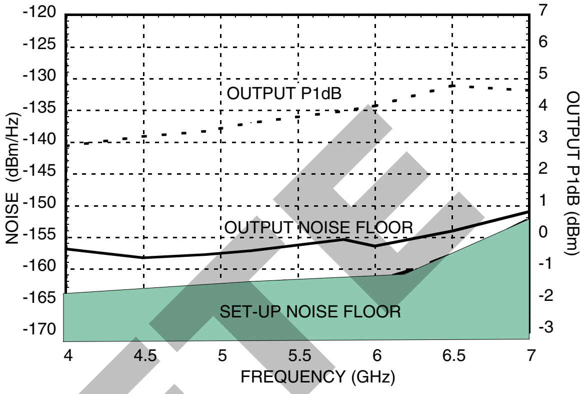
The "Calibrated, +25 °C" Carrier Suppression data was plotted after a manual adjustment of the Ip/In & Qp/Qn DC offsets at +25 °C, and an LO input power level of + 3 dBm. This adjustment setting was held constant during tests over LO input power level and temperature. The "Calibrated, over Temperature" plots represent the worst case Carrier Suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

Note 1: When I leads Q, the output spectrum results in lower sideband as the desired signal.

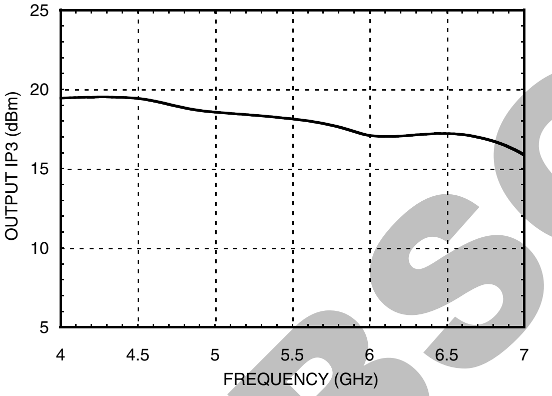
Wideband Performance vs. Frequency



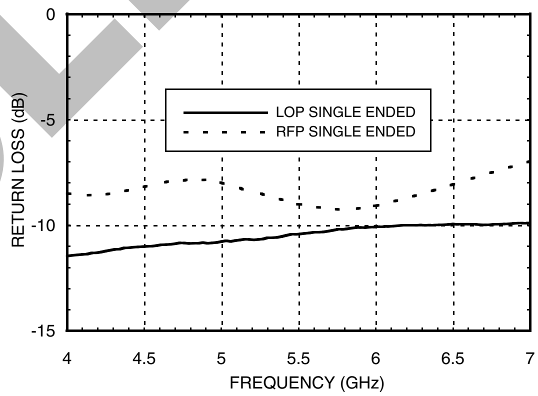
Output Noise Floor and P1dB vs. Frequency



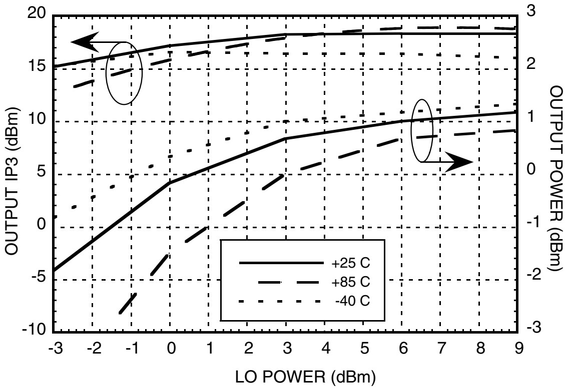
Output IP3 vs. Frequency



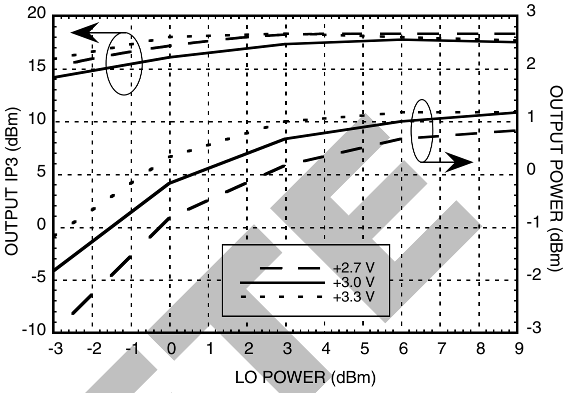
Return Loss



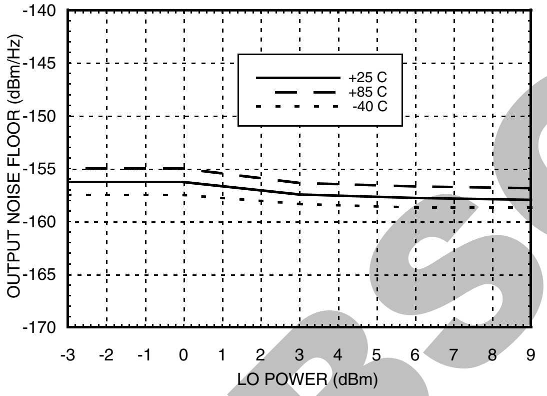
Output IP3 & Output Power vs. LO Power Over Temperature@ 5200 MHz



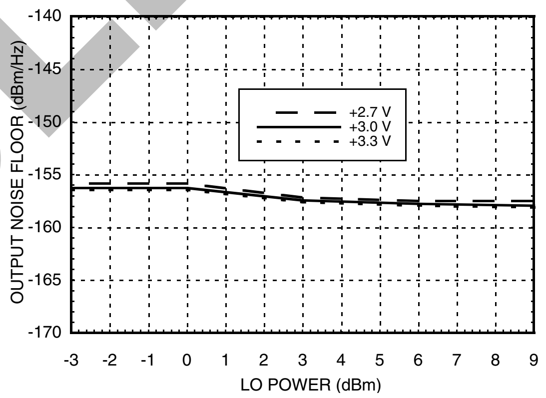
Output IP3 & Output Power vs. LO Power Over Supply@ 5200 MHz



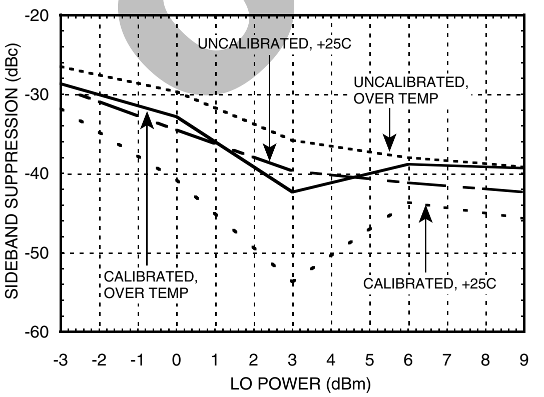
Output Noise vs. LO Power Over Temperature@ 5200 MHz



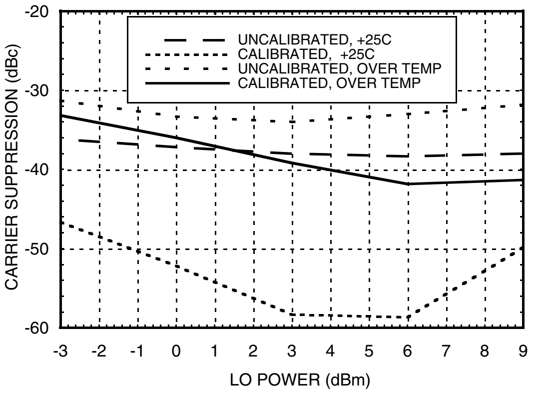
Output Noise vs. LO Power Over Supply@ 5200 MHz



Sideband Suppression* vs. LO Power@ 5200 MHz

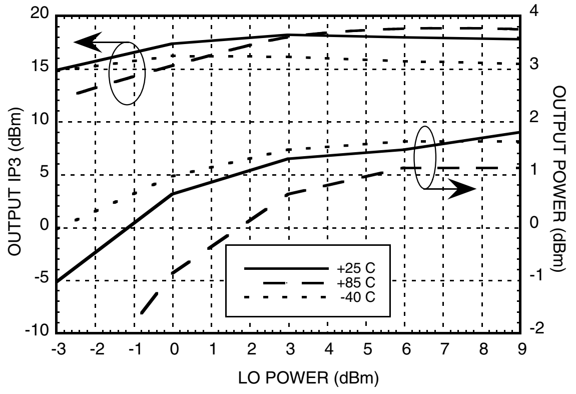


Carrier Suppression* vs. LO Power@ 5200 MHz

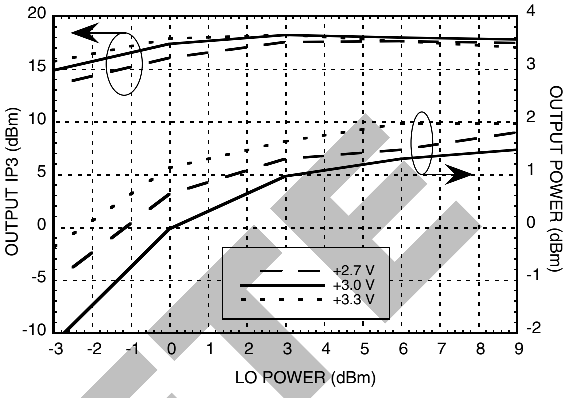


** See note regarding Calibrated vs. Uncalibrated test results herein.*

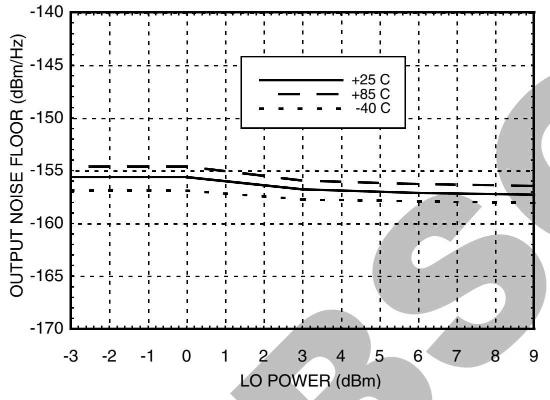
Output IP3 & Output Power vs. LO Power Over Temperature@ 5800 MHz



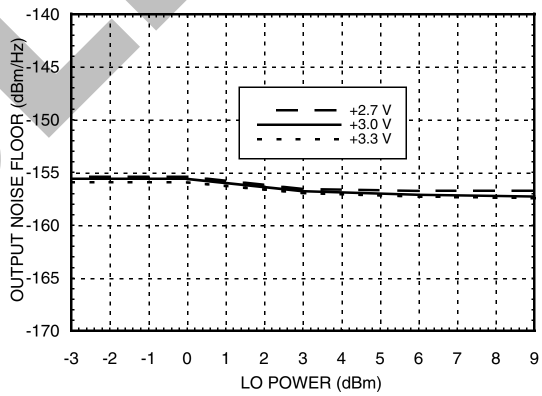
Output IP3 & Output Power vs. LO Power Over Supply@ 5800 MHz



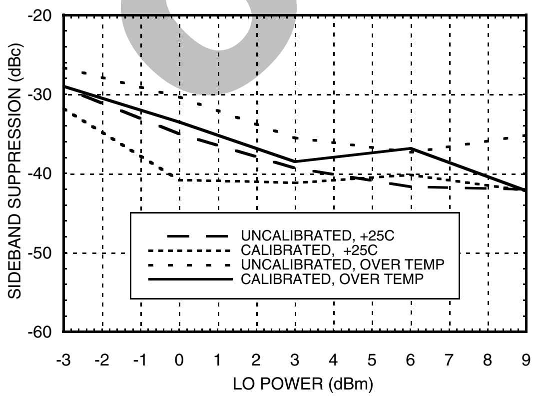
Output Noise vs. LO Power Over Temperature@ 5800 MHz



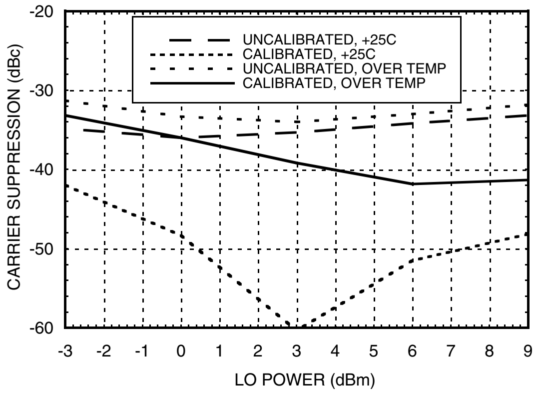
Output Noise vs. LO Power Over Supply@ 5800 MHz



Sideband Suppression* vs. LO Power@ 5800 MHz



Carrier Suppression* vs. LO Power@ 5800 MHz



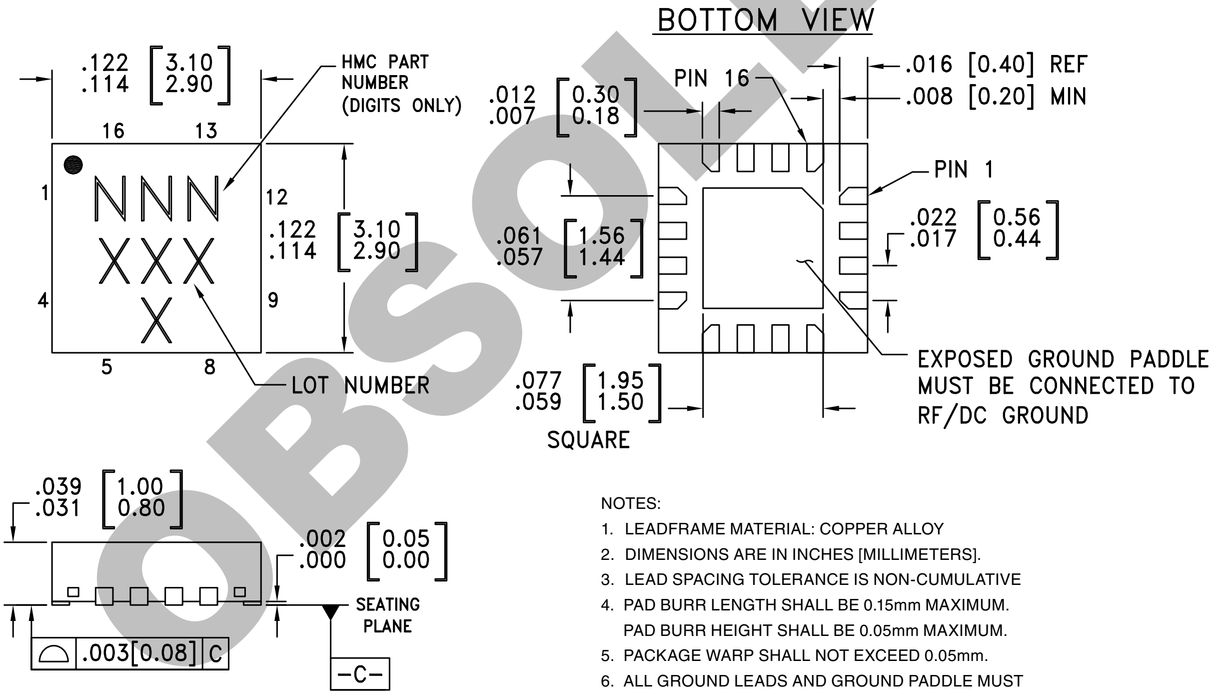
SiGe WIDEBAND DIRECT MODULATOR RFIC, 4 - 7 GHz

Absolute Maximum Ratings

Vcc	-0.5 to +6.0V
LO Input Power	+10 dBm
Baseband Input Voltage (Reference to GND)	-0.5 to +2.0V
Channel Temperature	150 °C
Continuous Pdiss (T = 85°C) (Derate 110 mW/°C above 85°C)	7 Watts
Thermal Resistance (R_{th}) (junction to lead)	9 °C/Watt
Storage Temperature	-40 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

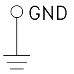
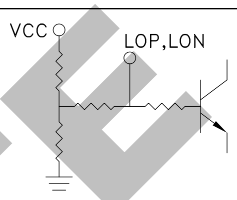
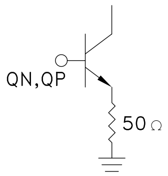
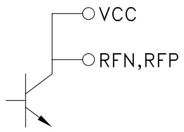
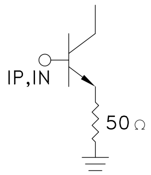
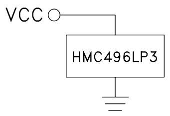
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

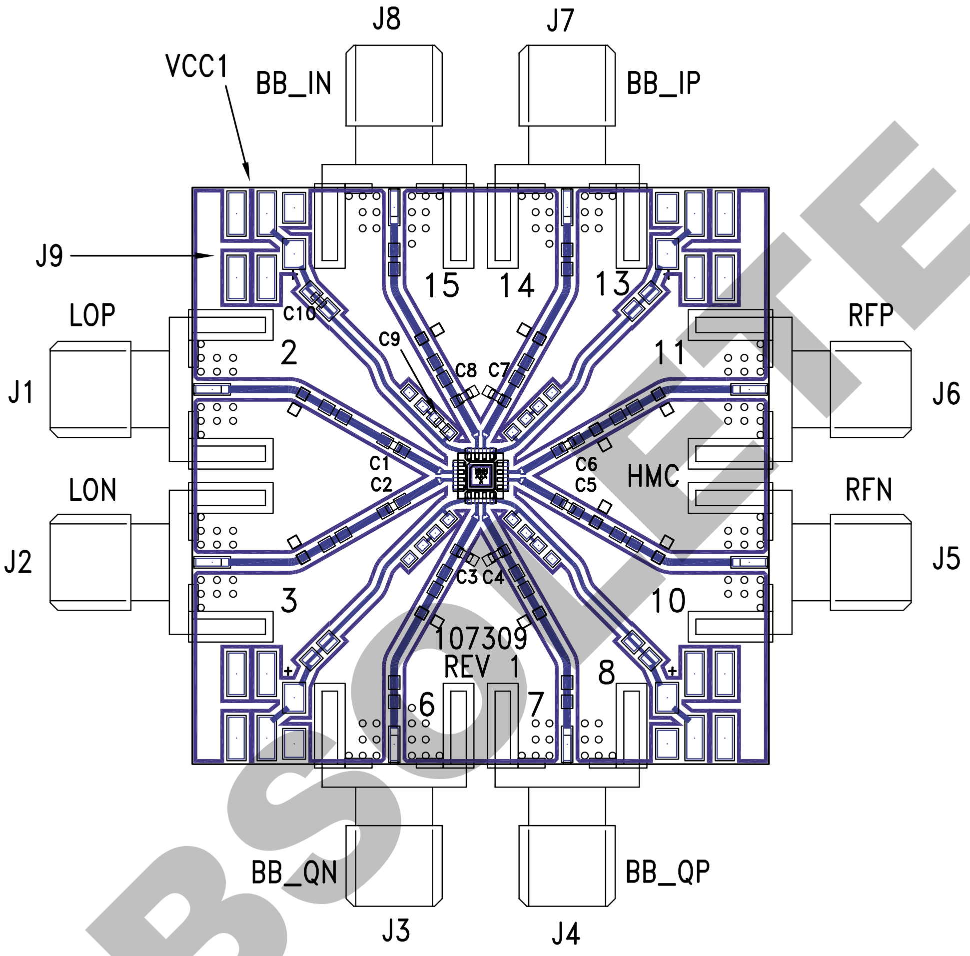
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC496LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	496 XXXX
HMC496LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	<u>496</u> XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 9, 12	GND	These pins and the ground paddle must be connected to a high quality RF/DC ground.	
2, 3	LOP, LON	Differential LO input ports. This device may be driven in either differential or single ended mode. In single ended mode, one port should be driven by the LO source while the other port may be terminated with a 50Ω resistor to ground.	
5, 8, 13	N/C	No Connection required. These pins may be connected to RF/DC ground without affecting performance.	
6, 7	QN, QP	Differential Quadrature baseband input. These are high impedance ports. The nominal recommended bias voltage is between 1.2 - 1.4V. The nominal recommended baseband input voltage is 1.2V peak to peak differential. By adjusting the DC bias voltage on ports QN & QP, the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltage for optimization is less than 15 mV. The amplitude and phase difference between the I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level.	
10, 11	RFN, RFP	RF Output port. This port is matched to 50 Ohms. A series capacitor should be connected to this port in order to prevent the DC supply voltage from appearing on the customer's PC board.	
14, 15	IP, IN	Differential Quadrature baseband input. These are high impedance ports. The nominal recommended bias voltage is between 1.2 - 1.4V. The nominal recommended baseband input voltage is 1.2V peak to peak differential. By adjusting the DC bias voltage on ports IN & IP, the Carrier Suppression of the device can be optimized for a specific frequency band and LO power level. The typical offset voltage for optimization is less than 15 mV. The amplitude and phase difference between the I and Q inputs can be adjusted in order to optimize the Sideband Suppression for a specific frequency band and LO power level.	
16	VCC	Supply voltage. Set to 3.0V for nominal operation. The nominal current for this port is 93 mA.	

Evaluation PCB



List of Materials for Evaluation PCB 107871 [1]

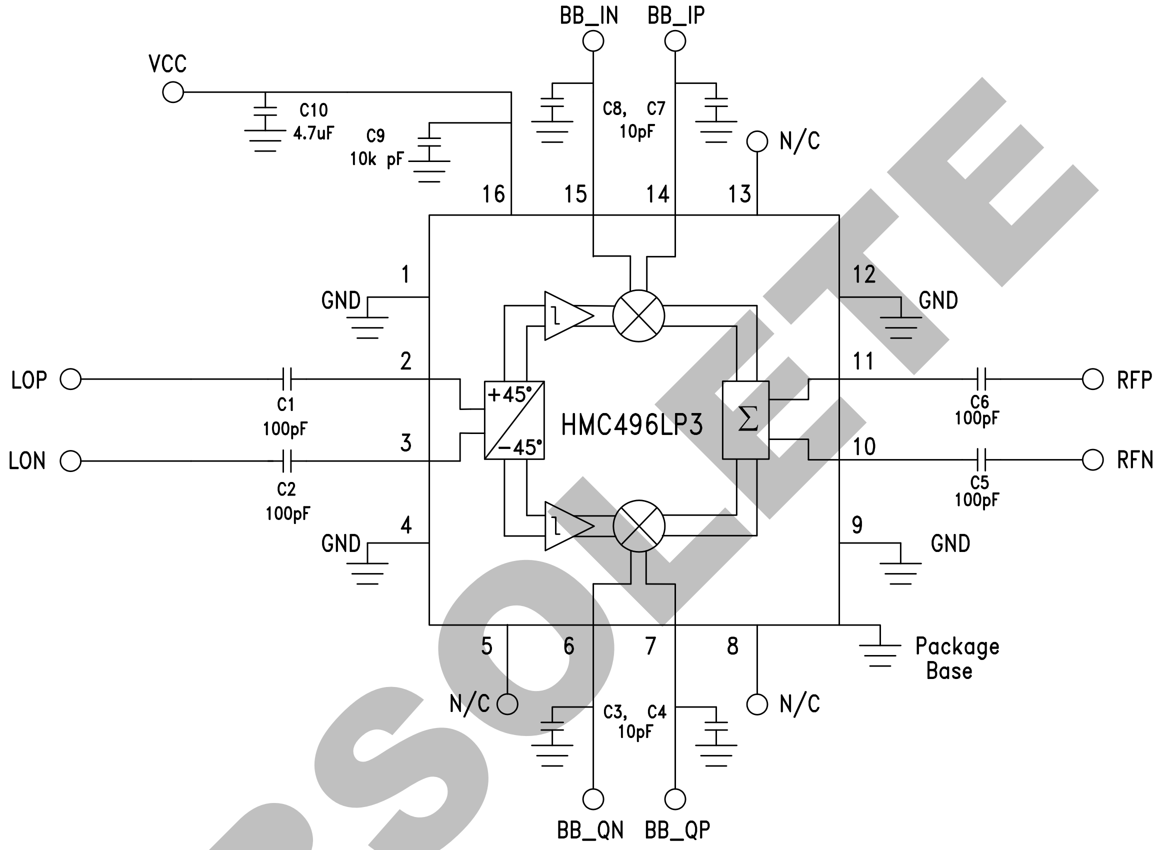
Item	Description
J1 - J8	PCB Mount SMA Connector
J9	DC Molex Connector
C1, C2, C5, C6	100 pF Chip Capacitor, 0402 Pkg.
C9	10k pF Chip Capacitor, 0402 Pkg.
C3, C4, C7, C8	10 pF Chip Capacitor, 0402 Pkg.
C15	4.7 uF, Case A, Tantulum
U1	HMC496LP3 / HMC496LP3E Modulator
PCB [2]	107309 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

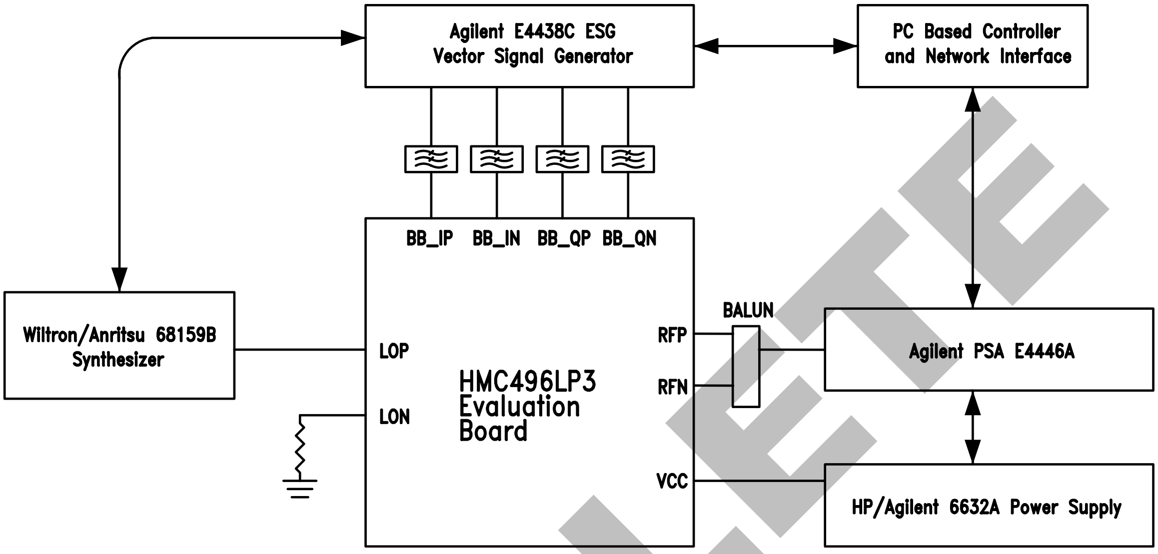
Application & Evaluation PCB Schematic



Note:

Baseband input frequency range is dependent on value of C3, C4, C7 and C8. The value of 10 pF was chosen to give a typical response of DC - 250 MHz. Input frequency range can be extended up to 3 GHz with possible degradation of LO leakage and broadband noise floor response by decreasing the value of C3, C4, C7 & C8.

Characterization Set-up



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