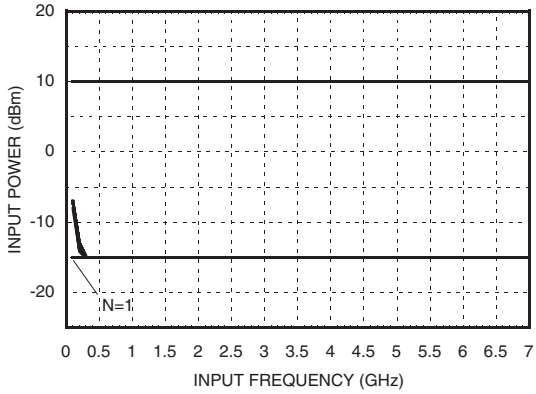
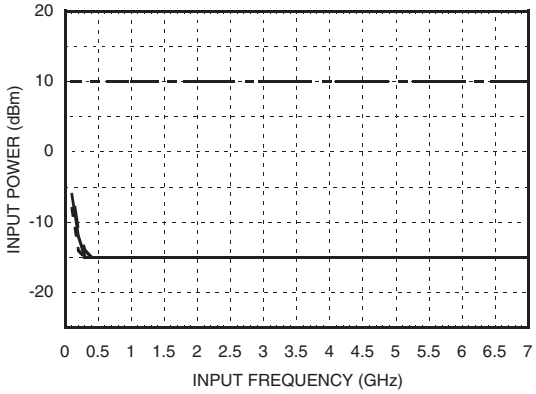
6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

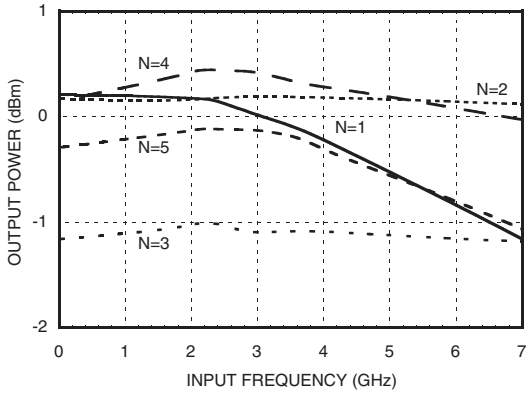
Input Sensitivity Window, All States



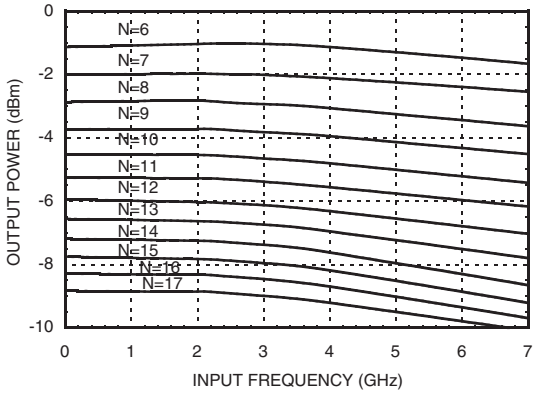
Input Sensitivity Window vs. Temperature, N = 17, T = -40°C to +85°C



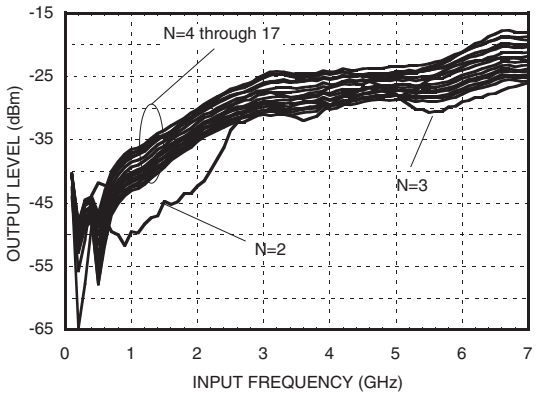
Output Power, Divide Ratio States 1 through 5



Output Power, Divide Ratio States 6 through 17



Fundamental Feedthru Power, Pin = 0 dBm



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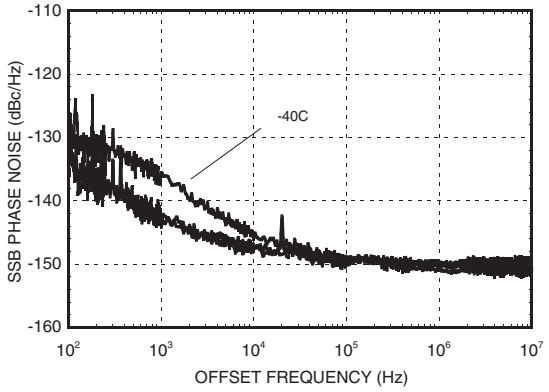
6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

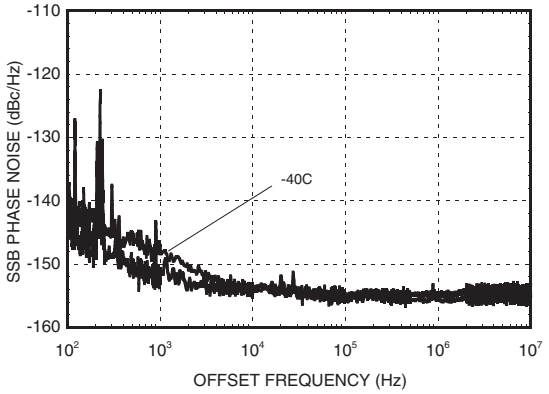
SSB Phase Noise Performance

Fin = 6 GHz, N = 2; T = -40°C, +25°C, +85°C



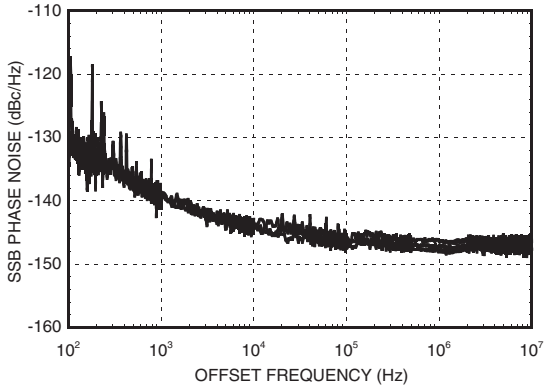
SSB Phase Noise Performance

Fin = 6 GHz, N = 17; T = -40°C, +25°C, +85°C



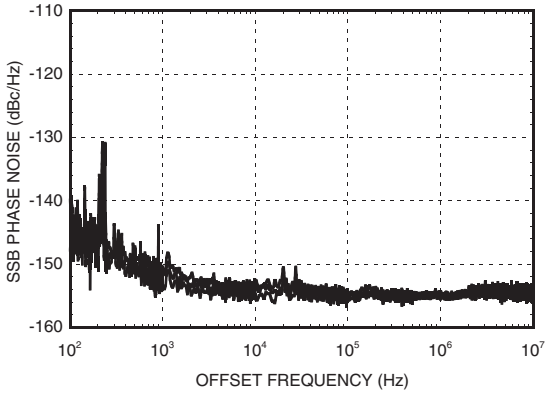
SSB Phase Noise Performance

Fin = 6 GHz, N = 2; Vcc = 4.75V, 5V, 5.25V

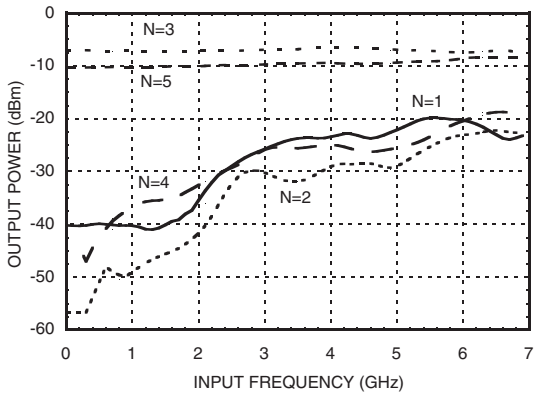


SSB Phase Noise Performance

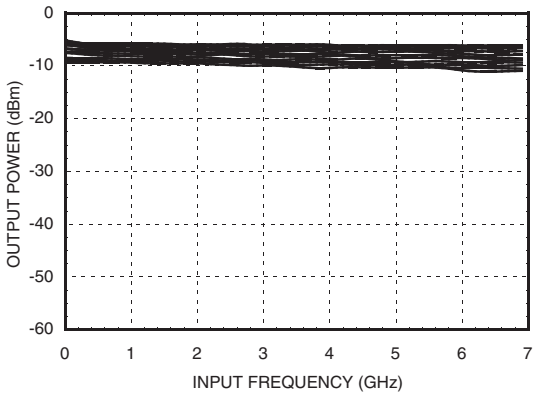
Fin = 6 GHz, N = 17; Vcc = 4.75V, 5V, 5.25V



2nd Harmonic, N = 1 through 5



2nd Harmonic, N = 6 through 17



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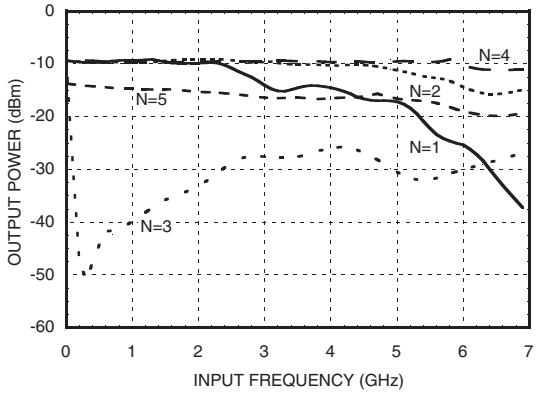
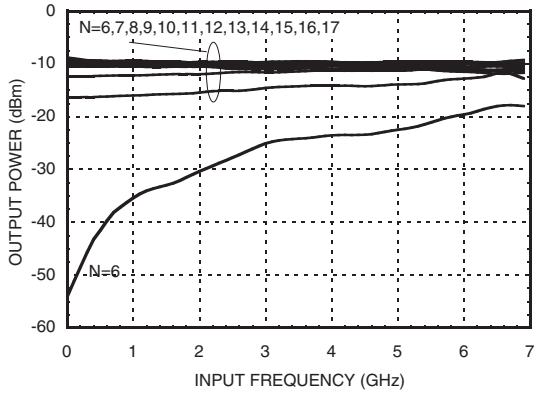
6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

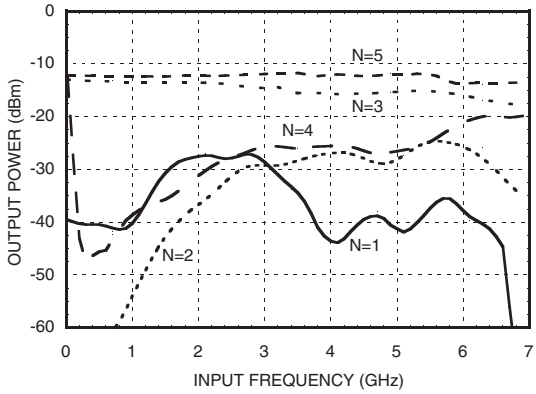
3rd Harmonic, N = 1 through 5



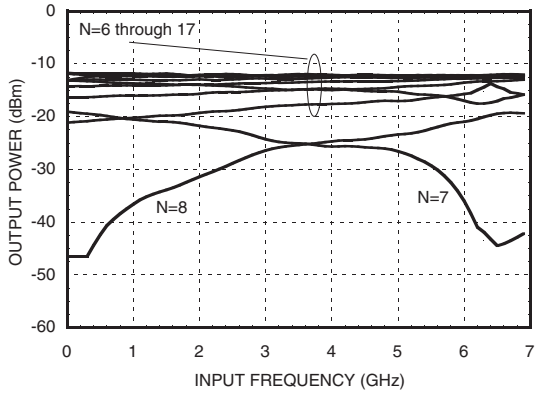
3rd Harmonic, N = 6 through 17



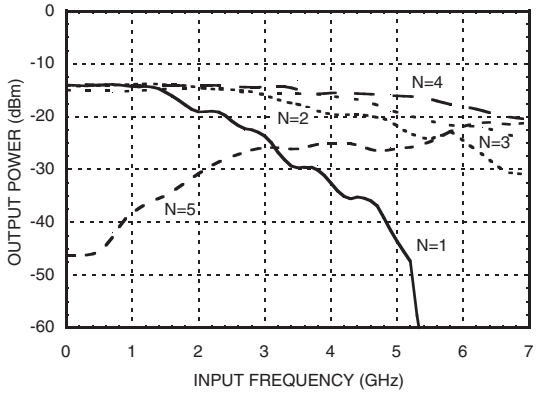
4th Harmonic, N = 1 through 5



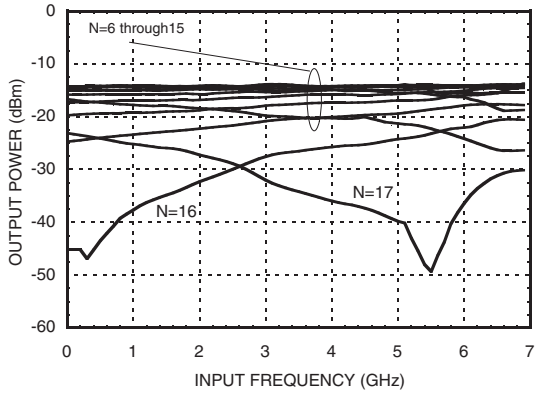
4th Harmonic, N = 6 through 17



5th Harmonic, N = 1 through 5



5th Harmonic, N = 6 through 17



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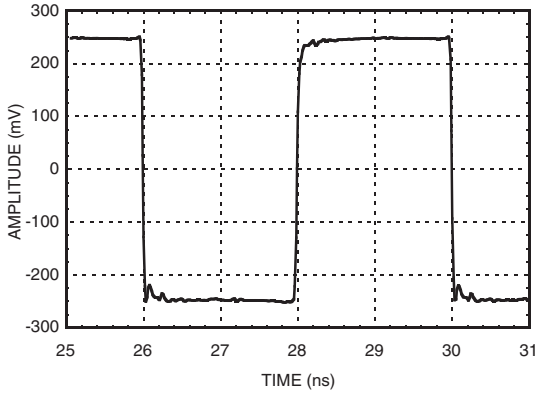
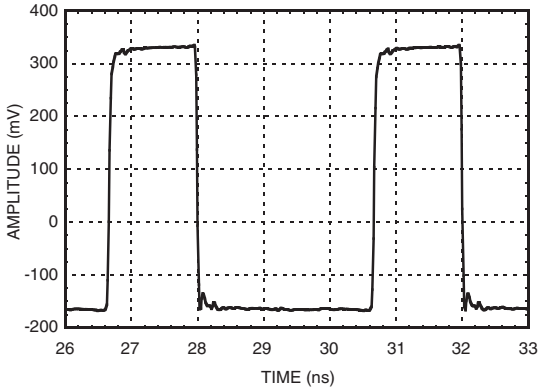
6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

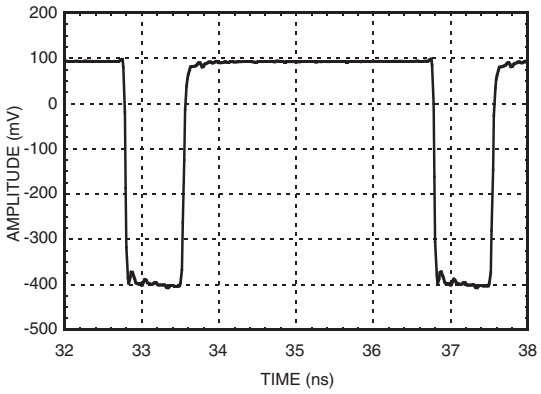
Output Voltage Waveform, Fin = 500 MHz, N = 2, Pin = 0 dBm, T= 25 °C



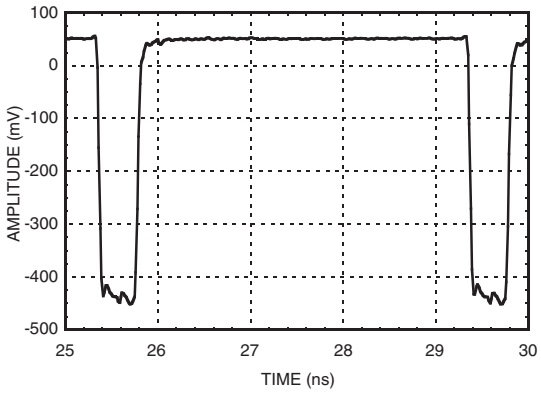
Output Voltage Waveform, Fin = 750 MHz, N = 3, Pin = 0 dBm, T= 25 °C



Output Voltage Waveform, Fin = 2500 MHz, N = 10, Pin = 0 dBm, T= 25 °C



Output Voltage Waveform, Fin = 4250 MHz, N = 17, Pin = 0 dBm, T= 25 °C



N	Output Duty Cycle (%)
1	Input
2	50
3 - 17	[1 - (2/N)] x 100

Note:
[1] Peak to peak amplitude does not change relative to N.
[2] Pulse duty cycle changes relative to N.

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6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

Absolute Maximum Ratings

RF Input (Vcc= +5V)	+13 dBm
Supply Voltage (Vcc)	+5.5V
Logic Inputs	-0.5V to (0.5V + Vcc)
Junction Temperature (Tc)	135 °C
Continuous Pdiss (T = 85 °C) (derate 49 mW/° C above 85 °C)	2.4 W
Thermal Resistance (Junction to ground paddle)	20.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

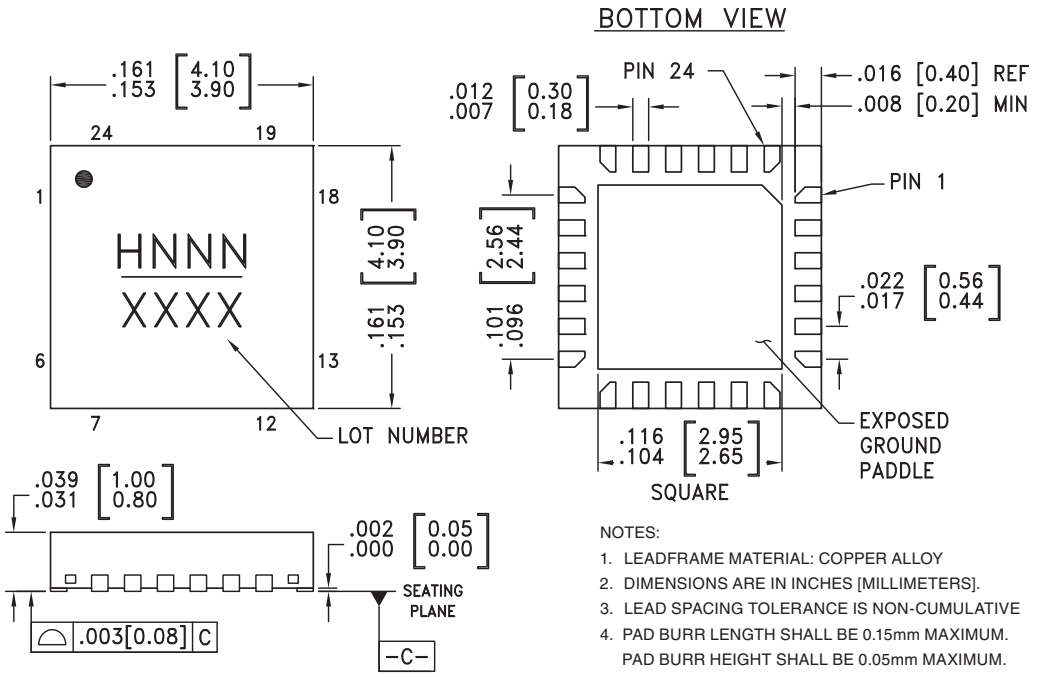
Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
4.75	180
5.00	190
5.25	210

Note: HMC705LP4E will work over full voltage range above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC705LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H705 XXXX
HMC705LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H705 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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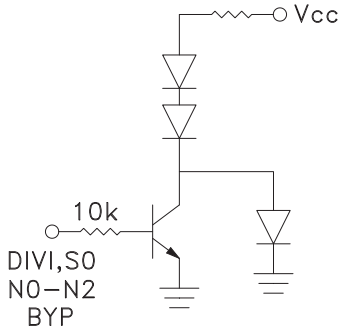
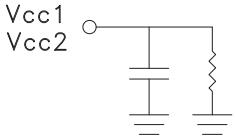
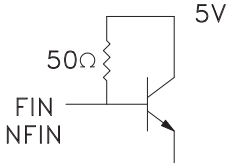
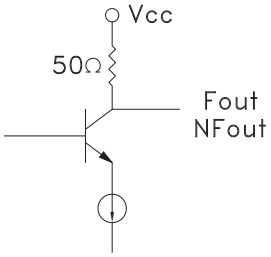
Pin Description

Pin Number	Function	Description	Interface Schematic
1 - 6, 8, 18	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
7, 20 - 24	DIV1, S0 N0 - N2 BYP	PFD INVERT function CMOS compatible input control bit Logic "LOW" = NORMAL Logic "HIGH" = INVERT	
9, 19	Vcc1, Vcc2	Supply Voltage	
10, 13, 14, 17	GND	These pins and package bottom must be connected to RF DC ground.	
11	NFIN	(These pins are AC coupled and must be DC Blocked externally.) Frequency Input	
12	FIN	Frequency Input Complement	
15	NFout	Frequency, output complement	
16	Fout	Frequency output	

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HMC705LP4(E) Programming Truth Table

Division Ratio N	S0	N0	N1	N2	DIV 1	BYP
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	1	0	0	0	1	0
4	0	1	0	0	0	0
5	1	1	0	0	0	0
6	0	0	1	0	0	0
7	1	0	1	0	0	0
8	0	1	1	0	0	0
9	1	1	1	0	0	0
10	0	0	0	1	0	0
11	1	0	0	1	0	0
12	0	1	0	1	0	0
13	1	1	0	1	0	0
14	0	0	1	1	0	0
15	1	0	1	1	0	0
16	0	1	1	1	0	0
17	1	1	1	1	0	0

0 = Logic Low
1 = Logic High

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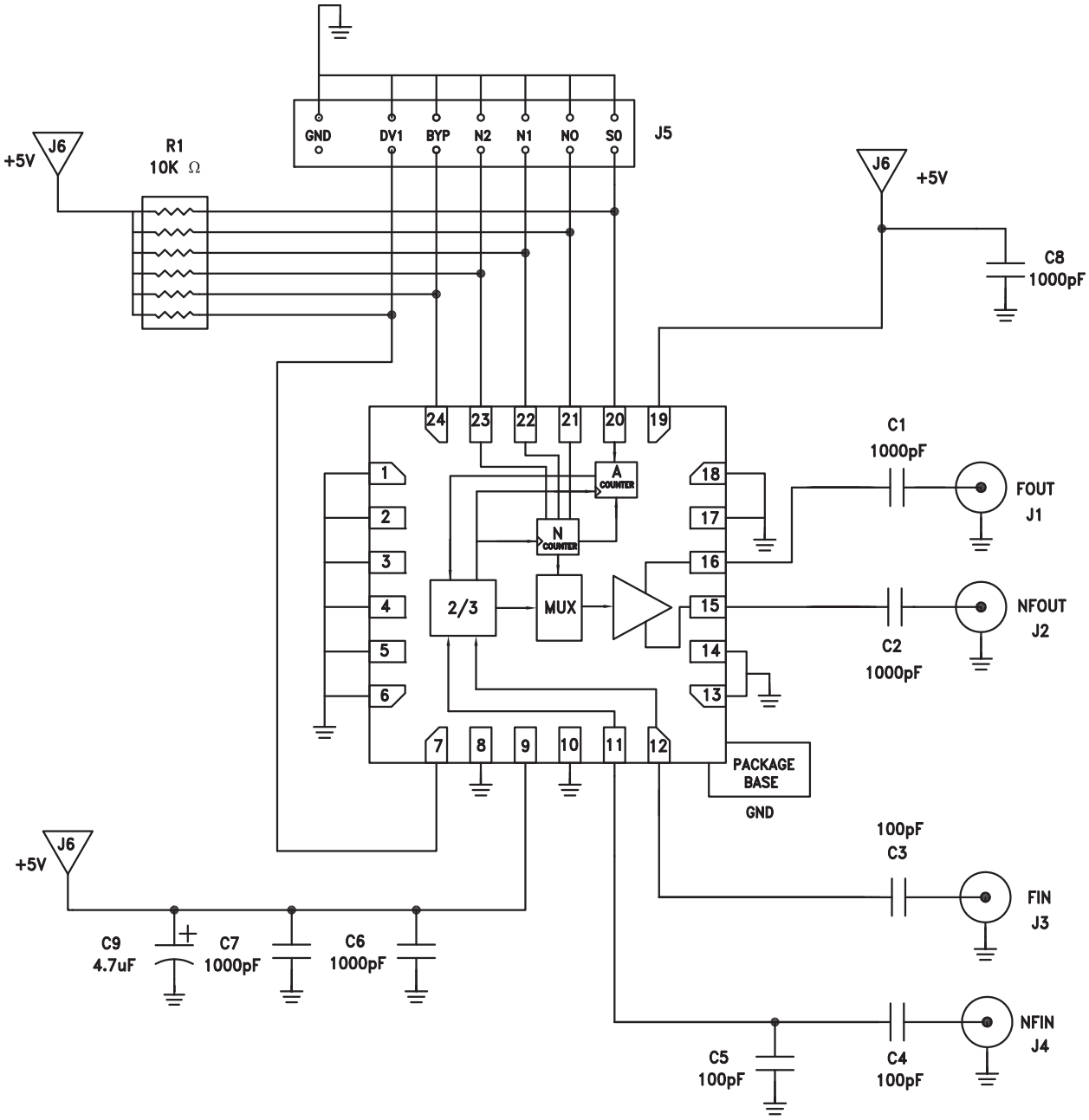
Evaluation PCB Circuit



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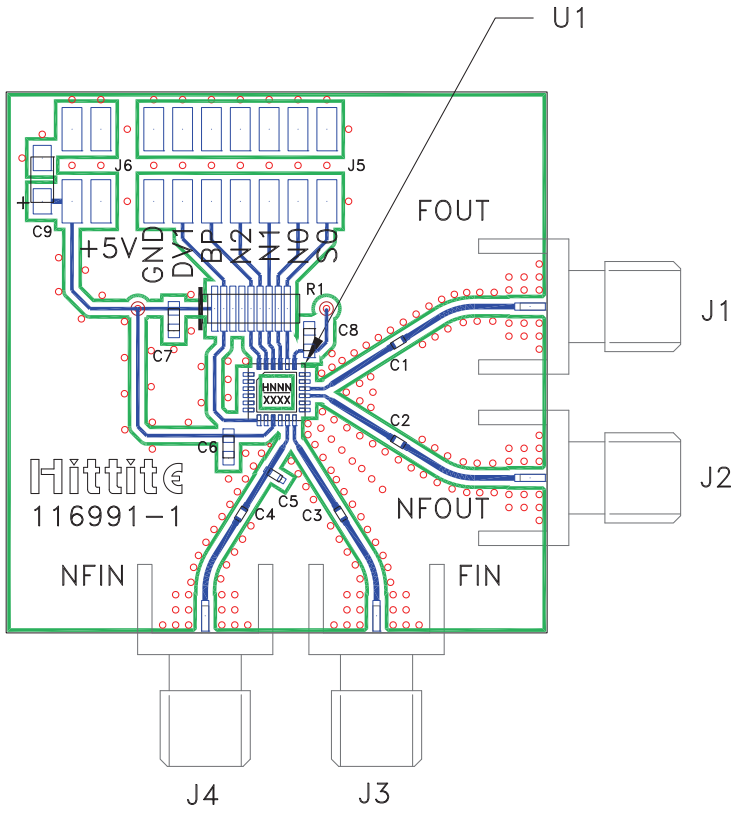
RoHS✓ EARTH FRIENDLY

Evaluation PCB



List of Materials for Evaluation PCB 116993 [1]

Item	Description
J1 - J4	PCB Mount SMA Connector
J5	14 Position Header
J6	4 Position Header
R1	10K Ohm Resistor Network, Bissel SMD
C1, C2	1000 pF Capacitor, 0402 Pkg.
C3 - C5	100 pF Capacitor, 0402 Pkg.
C6 - C8	1000 pF Capacitor, 0603 Pkg.
C9	4.7 µF Tantalum Capacitor, Case A
U1	HMC705LP4(E) Programmable Divider
PCB [2]	116991 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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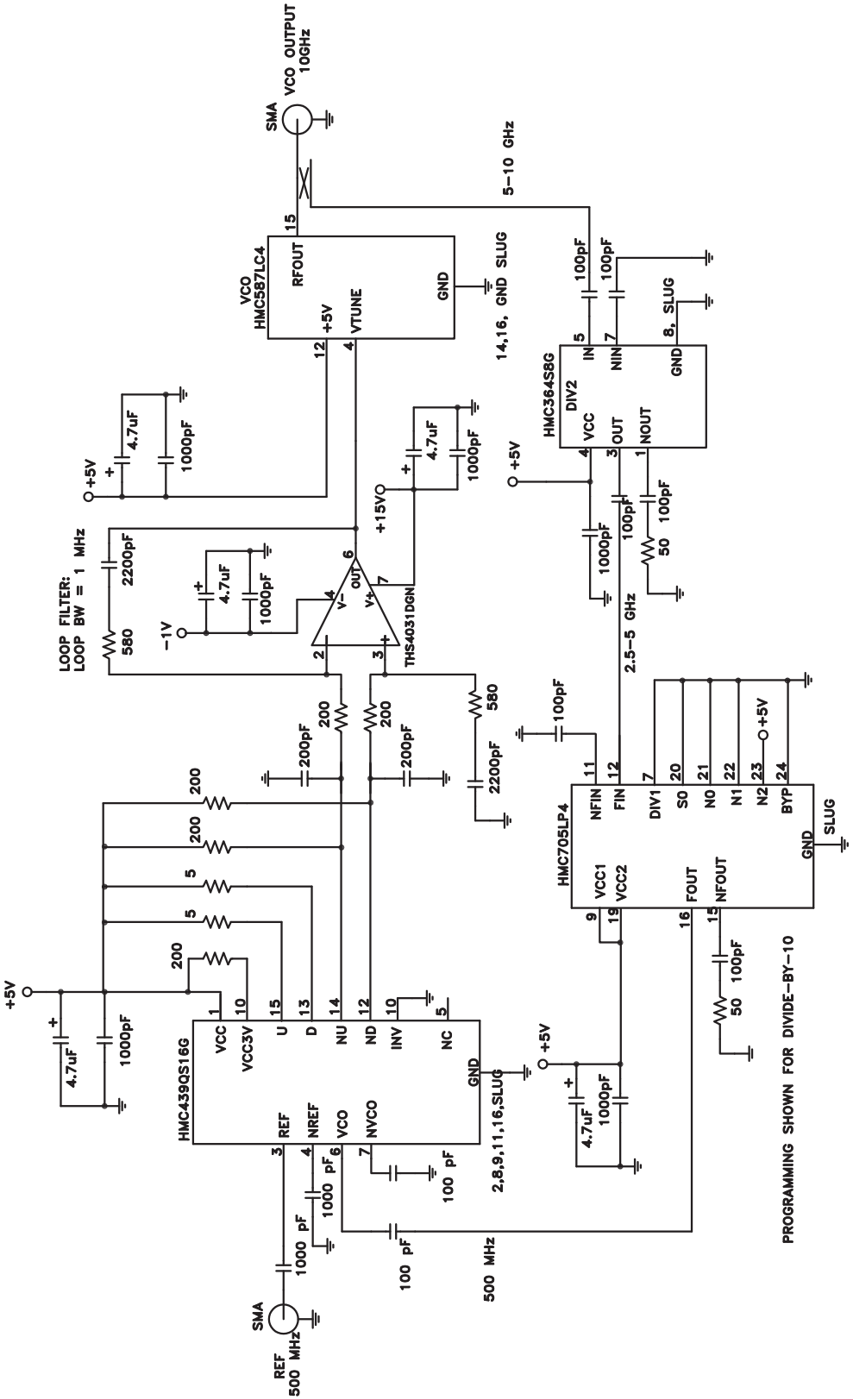
6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

Typical PLL Application Circuit using HMC705LP4(E)

PLL application shown for Divide-by-10. Contact HMC to discuss your specific application.



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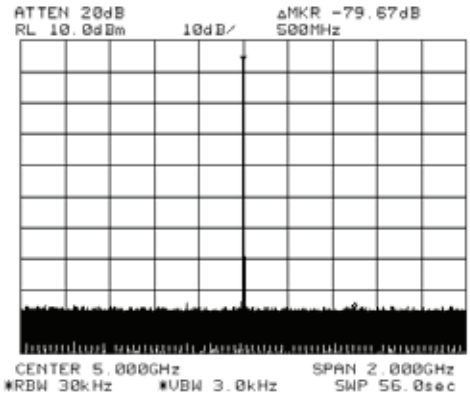
Typical Application Showing Spurious Performance

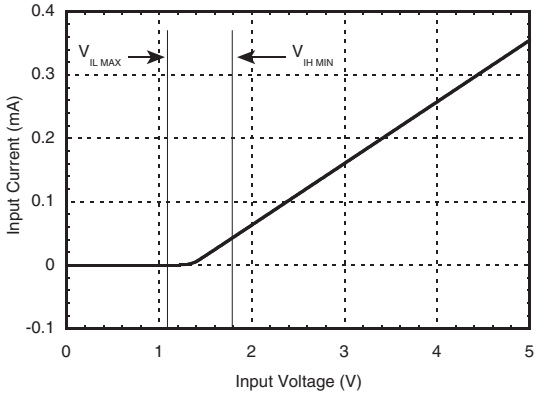


CMOS/TTL Input Characteristics

Maximum Input Logic "0" Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 1 µA.

Minimum Input Logic "1" Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 50 µA.

Input IV characteristics for the logic inputs (S0, N0 - N2, DIVI, BYP) are shown below:



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