Digital Attenuator
31.5 dB, 6-Bit, TTL Driver, DC-2.0 GHz

Electrical Specifications: T_A = +25°C[2]

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC - 2.0 GHz	dB	—	3.2	3.8
Attenuation Accuracy[1,3,4]	Any Bit or Combination of Bits	DC - 2.0 GHz	dB	—	—	+(.3 +7% of atten.) -(.2 +1% of atten.)
VSWR	Full Range	DC - 2.0 GHz	Ratio	—	—	1.8:1
Trise, Tfall Ton, Toff Transients	10% to 90% 50% Control to 90%/10% RF In-band (peak to peak)	— — —	ns ns mV	— — —	50 150 50	— — —
1 dB Compression [5]	Input Power Input Power	50 MHz 0.5 - 2.0 GHz	dBm dBm	— —	+21 +29	— —
Input IP_3 [5]	Two Tone Inputs up to +5 dBm	50 MHz 0.5 - 2.0 GHz	dBm dBm	— —	+35 +48	— —
Input IP_2 [5]	Two Tone Inputs up to +5 dBm	50 MHz 0.5 - 2.0 GHz	dBm dBm	— —	+45 +79	— —
Vcc -Vee	— —	— —	V V	4.5 -8.0	5.0 —	5.5 -5.0
Icc	Vcc = 4.5 to 5.5V	—	mA	—	—	6.0
-Iee	-Vee = -5.0 to -8.0V	—	mA	—	—	1.0

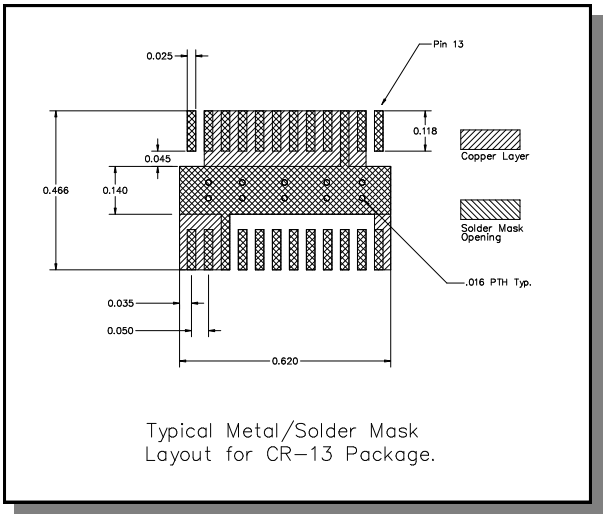
1. Above reference insertion loss.
2. All specifications apply when operated with bias voltages of +5V for V_{CC} and –5.0 V to –8.0 V for V_{EE} and 50Ω impedance at all ports unless otherwise stated.
3. This attenuator is guaranteed monotonic.
4. For the attenuator to meet the guaranteed specifications, it is necessary to have a DC return on either RF1 or RF2. The DC return can be either a 10KΩ resistor, or an RF choke.
5. V_{EE} = -5 V for the typical numbers given.

Absolute Maximum Ratings [6,7]

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 2.0 GHz	 +27 dBm +34 dBm
V_{CC}	-0.5V ≤ V_{CC} ≤ +7.0V
V_{EE}	-8.5V ≤ V_{EE} ≤ +0.5V
V_{CC} - V_{EE}	-0.5V ≤ V_{CC} - V_{EE} ≤ 14.5V
Vin[8]	-0.5V ≤ Vin ≤ V_{CC} + 0.5V
Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. M/A-COM does not recommend sustained operation near these survivability limits.
8. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Recommended PCB Configuration



Typical Metal/Solder Mask Layout for CR-13 Package.

Handling Procedures

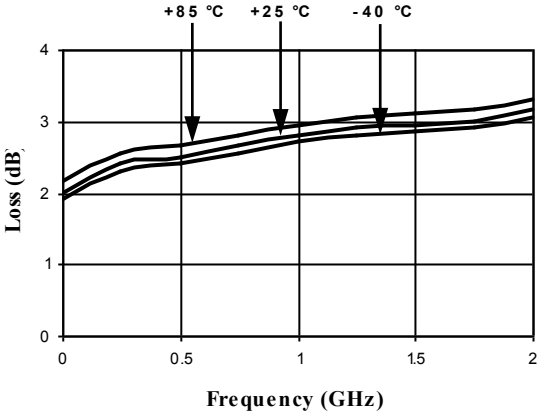
Please observe the following precautions to avoid damage:

Static Sensitivity

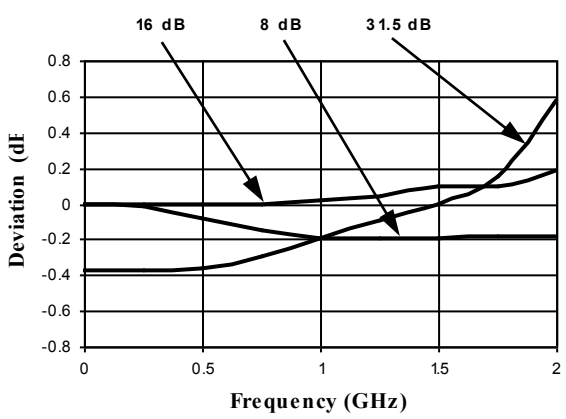
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Typical Performance Curves

Insertion Loss vs. Frequency



Attenuation Accuracy vs. Frequency

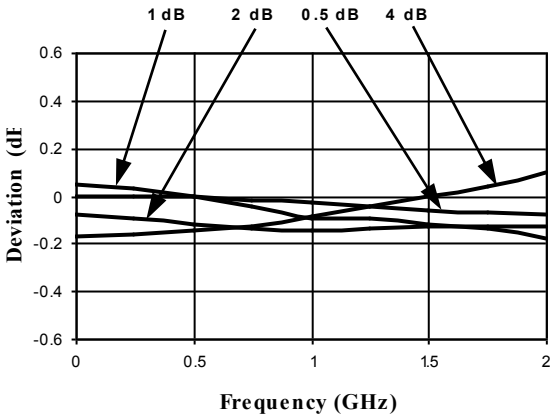


Truth Table (Digital Attenuator)

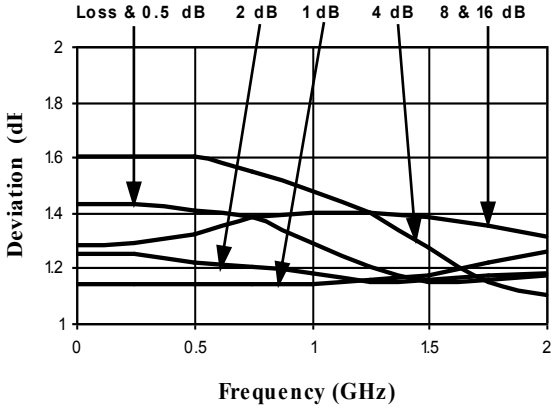
C16	C8	C4	C2	C1	C0.5	Attenuation
0	0	0	0	0	0	Loss, Reference
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1.0 dB
0	0	0	1	0	0	2.0 dB
0	0	1	0	0	0	4.0 dB
0	1	0	0	0	0	8.0 dB
1	0	0	0	0	0	16.0 dB
1	1	1	1	1	1	31.5 dB

0 = TTL Low; 1 = TTL High

Attenuation Accuracy vs. Frequency

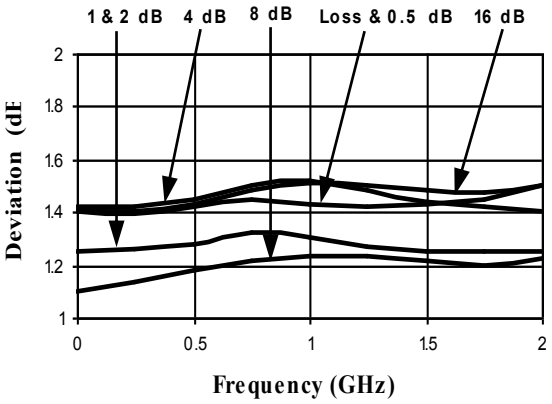


RF1 VSWR vs. Frequency

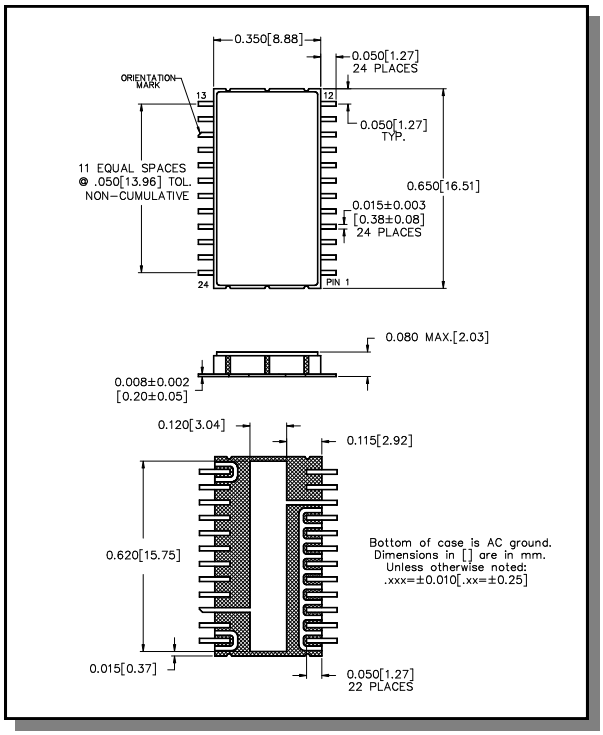


Typical Performance Curves

RF2 VSWR vs. Frequency



Lead-Free, CR-13 Ceramic Package†



† Reference Application Note M538 for lead-free solder reflow recommendations.

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