+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND..... -0.3V to +0.3V
CH0–CH3, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.30mW/°C above +70°C)..... 667mW
CERDIP (derate 10.00mW/°C above +70°C)..... 800mW
Operating Temperature Ranges
MAX1248_C_E/MAX1249_C_E ..... 0°C to +70°C
MAX1248_E_E/MAX1249_E_E..... -40°C to +85°C
MAX1248_MJE/MAX1249_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1248—4.7µF capacitor at VREF pin; MAX1249—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX124_A			±0.5	LSB
		MAX124_B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX124_A			±1	LSB
		MAX124_B			±2	
Gain Error (Note 3)		MAX124_A			±1	LSB
		MAX124_B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.05		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		65kHz, 2.500Vp-p (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1248—4.7µF capacitor at VREF pin; MAX1249—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF / 2			±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH\_}$ = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance				16		pF
INTERNAL REFERENCE (MAX1248 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C (Note 7)	2.470	2.500	2.530	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient		MAX1248		±30		ppm/°C
Load Regulation (Note 8)		0mA to 0.2mA output load		0.35		mV
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.01			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled)						
VREF Input Voltage Range (Note 9)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
REFADJ Buffer-Disable Threshold			V_{DD} - 0.5			V
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX1248		2.06		V/V
		MAX1249		2.00		
REFADJ Input Current		MAX1248			±50	µA
		MAX1249			±10	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$	2.0			V
		V_{DD} > 3.6V	3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 10)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current	I_S	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1248—4.7µF capacitor at VREF pin; MAX1249—external reference; VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = FLOAT			V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = FLOAT				±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 10)				15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input (Note 11)	V_{DD} = 5.25V		1.6	3.0	mA
			V_{DD} = 3.6V		1.2	2.0	
		Full power-down	V_{DD} = 5.25V		3.5	15	µA
			V_{DD} = 3.6V		1.2	10	
	I_{DD}	Fast power-down (MAX1248)			30	70	
Supply Rejection (Note 12)	PSR	V_{DD} = 2.7V to 5.25V, full-scale input, external reference = 2.500V			±0.3		mV

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX124__C/E	20		200	ns
			MAX124__M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 10)		0			ns

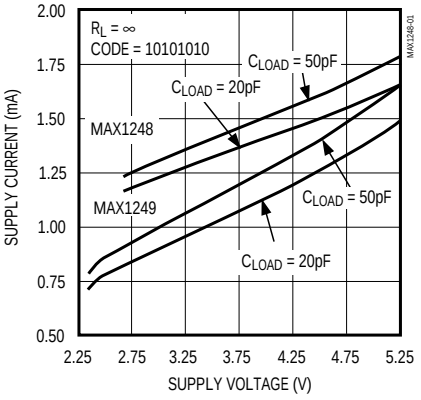
Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX1248—internal reference, offset nulled; MAX1249—external reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7 Sample tested to 0.1% AQL.
Note 8: External load should not change during conversion for specified accuracy.
Note 9: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 10 Guaranteed by design. Not subject to production testing.
Note 11: The MAX1249 typically draws 400µA less than the values shown.
Note 12: Measured as $|V_{FS}(2.7V) - V_{FS}(5.25V)|$.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

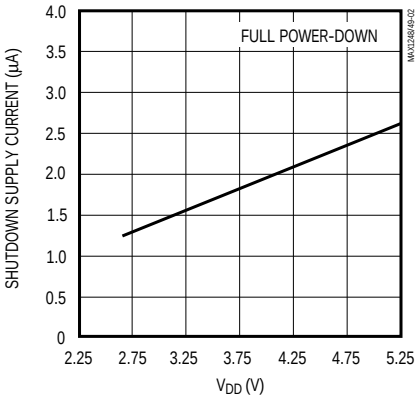
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

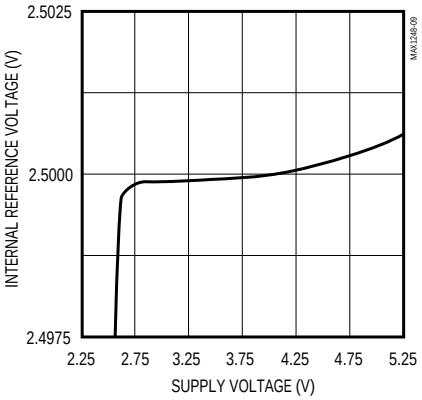
SUPPLY CURRENT vs. SUPPLY VOLTAGE



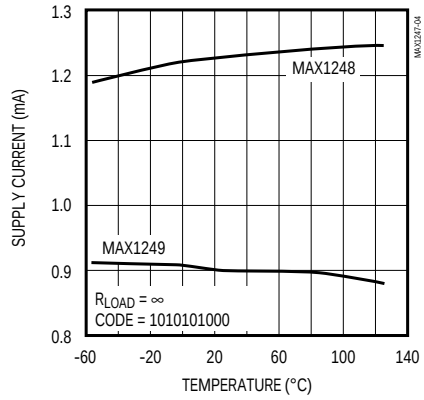
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



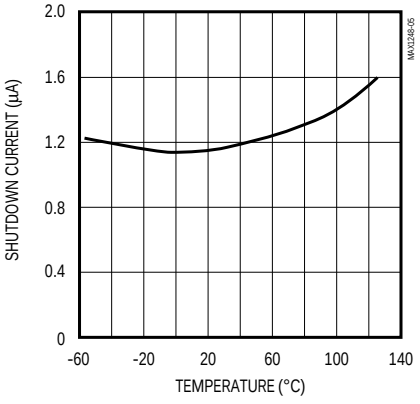
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



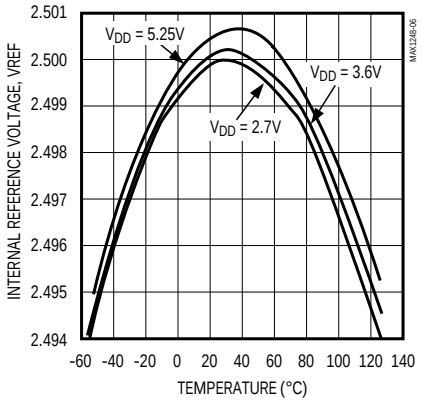
SUPPLY CURRENT vs. TEMPERATURE



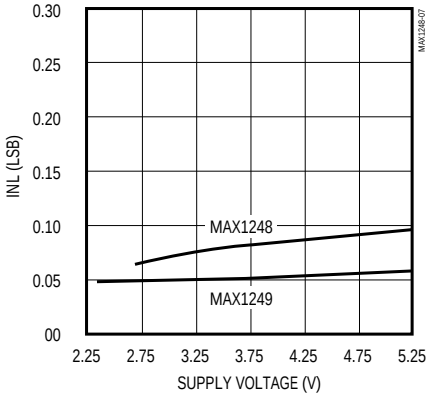
SHUTDOWN CURRENT vs. TEMPERATURE



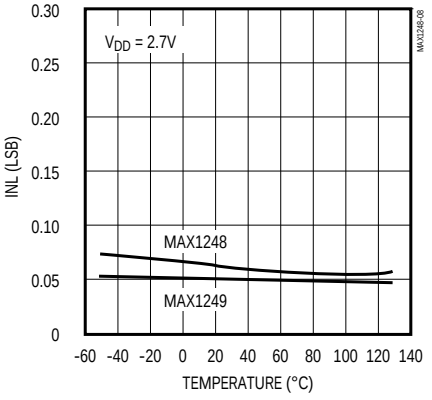
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



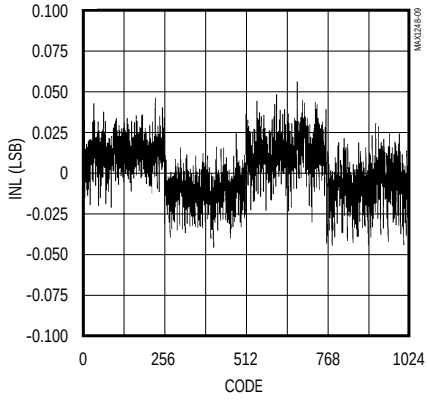
INTERGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. CODE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2–5	CH0–CH3	Sampling Analog Inputs
6	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
7	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1248/MAX1249 down; otherwise, the devices are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
8	VREF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX1248 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
9	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
10	AGND	Analog Ground
11	DGND	Digital Ground
12	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
13	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1248/MAX1249 begin the A/D conversion and goes high when the conversion is completed. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
14	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
15	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
16	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

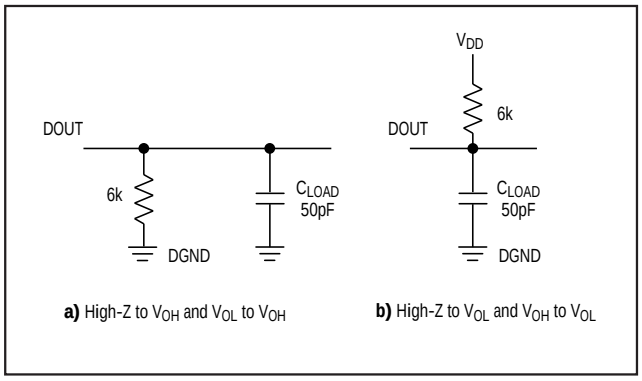


Figure 1. Load Circuits for Enable Time

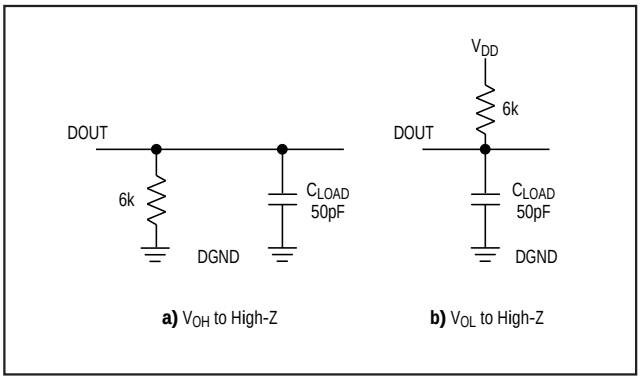


Figure 2. Load Circuits for Disable Time

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

Detailed Description

The MAX1248/MAX1249 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX1248/MAX1249.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH3, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from two pairs: CH0/CH1 and CH2/CH3. Configure the channels with Tables 2 and 3. Please note that the codes for CH0–CH3 in the MAX1248/MAX1249 correspond to the codes for CH2–CH5 in the eight-channel (MAX148/MAX149) versions.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN+}) - (V_{IN-})]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of $|IN+ - IN-|$ is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high,

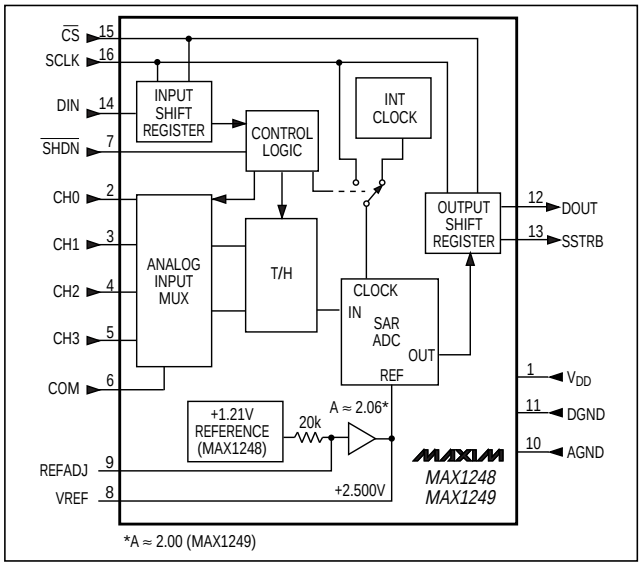


Figure 3. Block Diagram

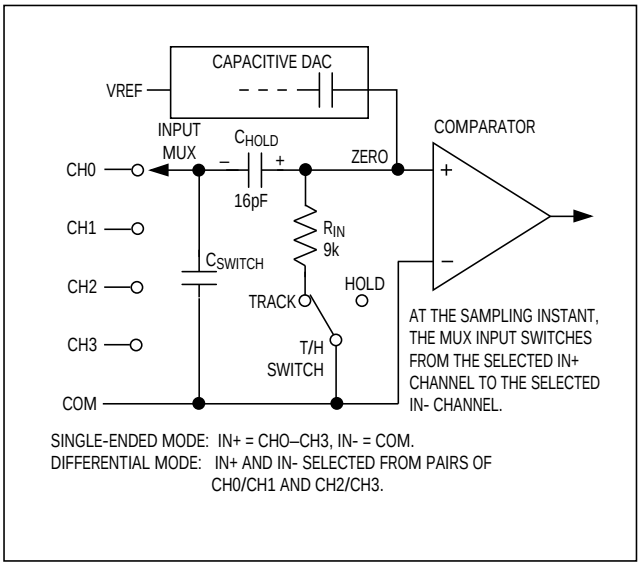


Figure 4. Equivalent Input Circuit

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION		
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.		
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the four channels are used for the conversion (Tables 2 and 3).		
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF / 2 to +VREF / 2.		
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).		
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 0 0 1 1	 PD0 0 1 0 1	 Mode Full power-down Fast power-down (MAX1248 only) Internal clock mode External clock mode

the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 7.6 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 3kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 4mA.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1248/MAX1249's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1248/MAX1249 are compatible with SPI/QSPI and MICROWIRE devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the sim-

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	1	+				–
1	0	1		+			–
0	1	0			+		–
1	1	0				+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	1	+	–		
0	1	0			+	–
1	0	1	–	+		
1	1	0			–	+

plest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 10-bit conversion result). See Figure 19 for MAX1248/MAX1249 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 5 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with one leading zero, two sub-bits, and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 16). For bipolar inputs, the output is two's complement (Figure 17). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1248/MAX1249 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1248/MAX1249. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 6–9 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 10 SCLK falling edges (Figure 5). SSTRB and DOUT go into a high-impedance state when

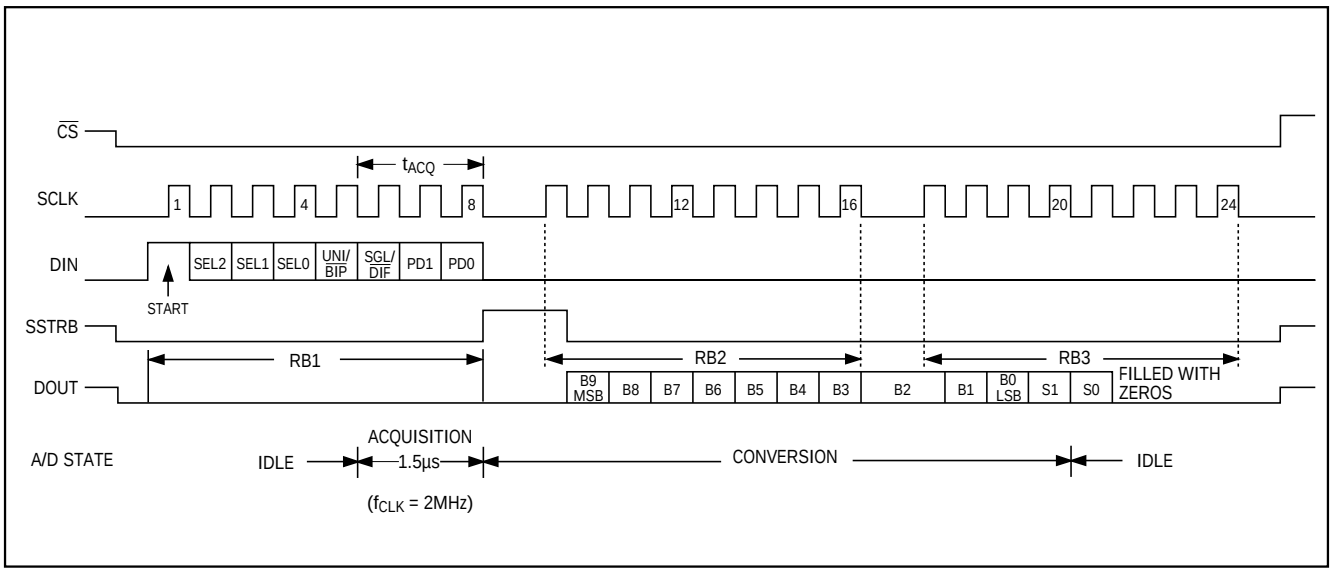


Figure 5. 24-Clock External Clock Mode Conversion Timing (MICROWIRE and SPI-Compatible, QSPI-Compatible with $f_{SCLK} \leq 2MHz$)

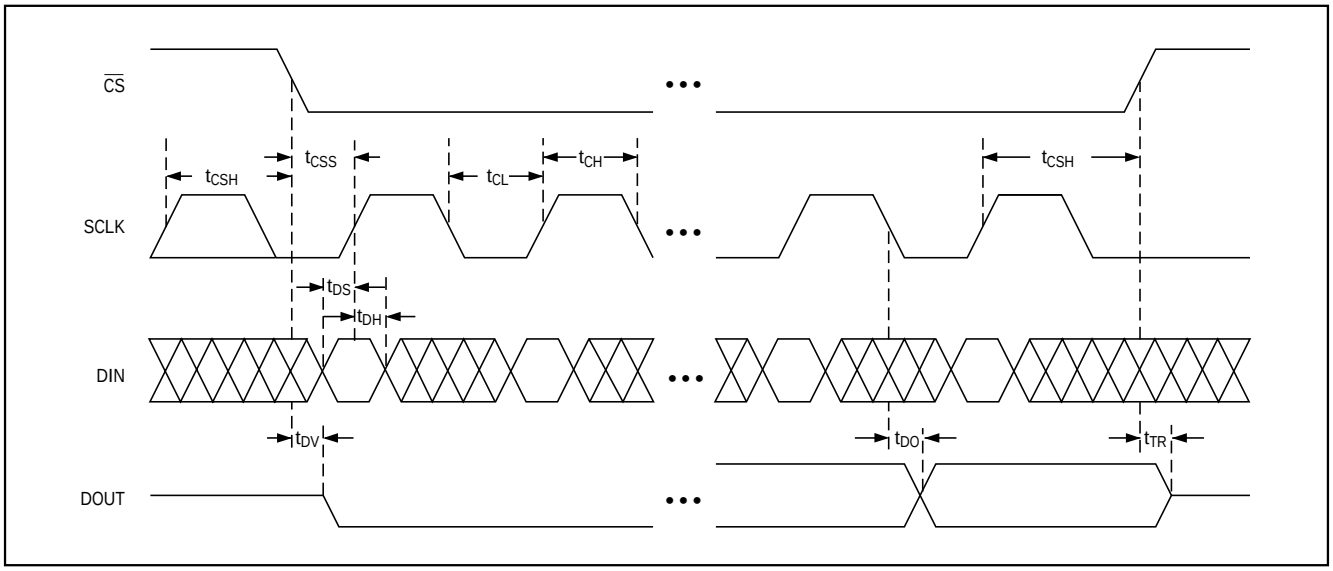


Figure 6. Detailed Serial-Interface Timing

$\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 7 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

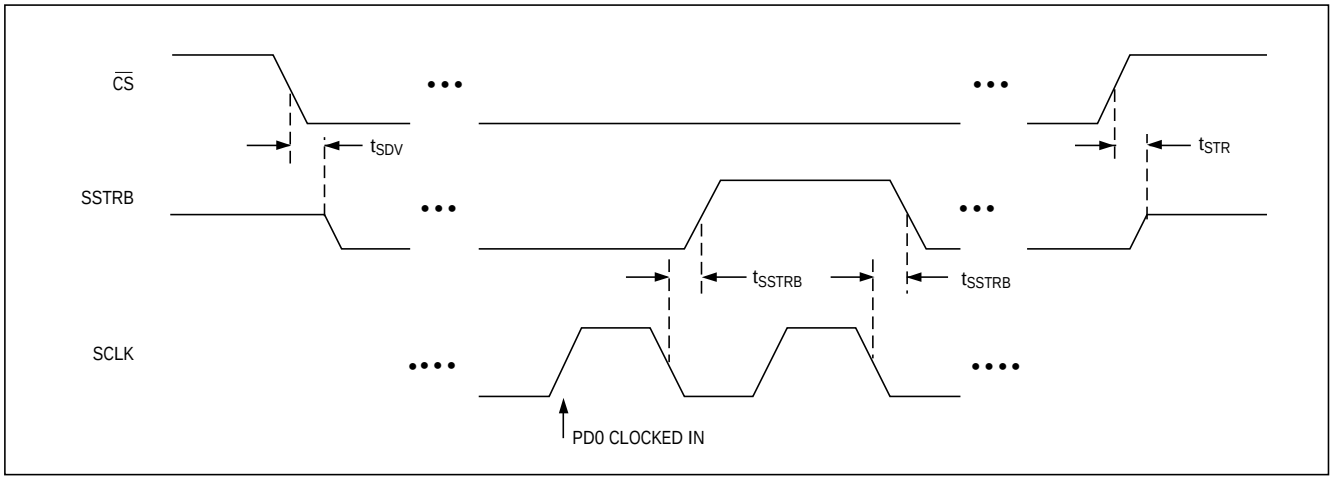


Figure 7. External Clock Mode SSTRB Detailed Timing

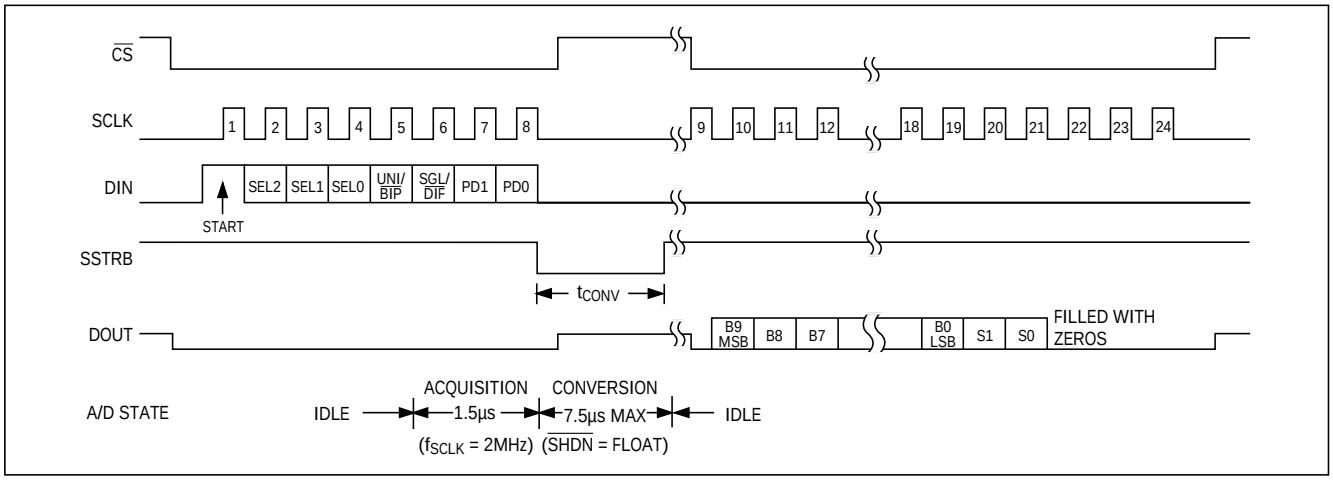


Figure 8. Internal Clock Mode Timing

Internal Clock

In internal clock mode, the MAX1248/MAX1249 generate their own conversion clocks internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 8). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1248/MAX1249 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 9 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1248/MAX1249 at clock rates exceeding 2.0MHz if the minimum acquisition time, t_{ACQ}, is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1248/MAX1249 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion. Figure 10a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1248/MAX1249. Figure 10b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1248/MAX1249 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros (also see Table 4).

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The 100kHz minimum clock rate is limited by droop on the sample-and-hold, and is independent of the compensation used.

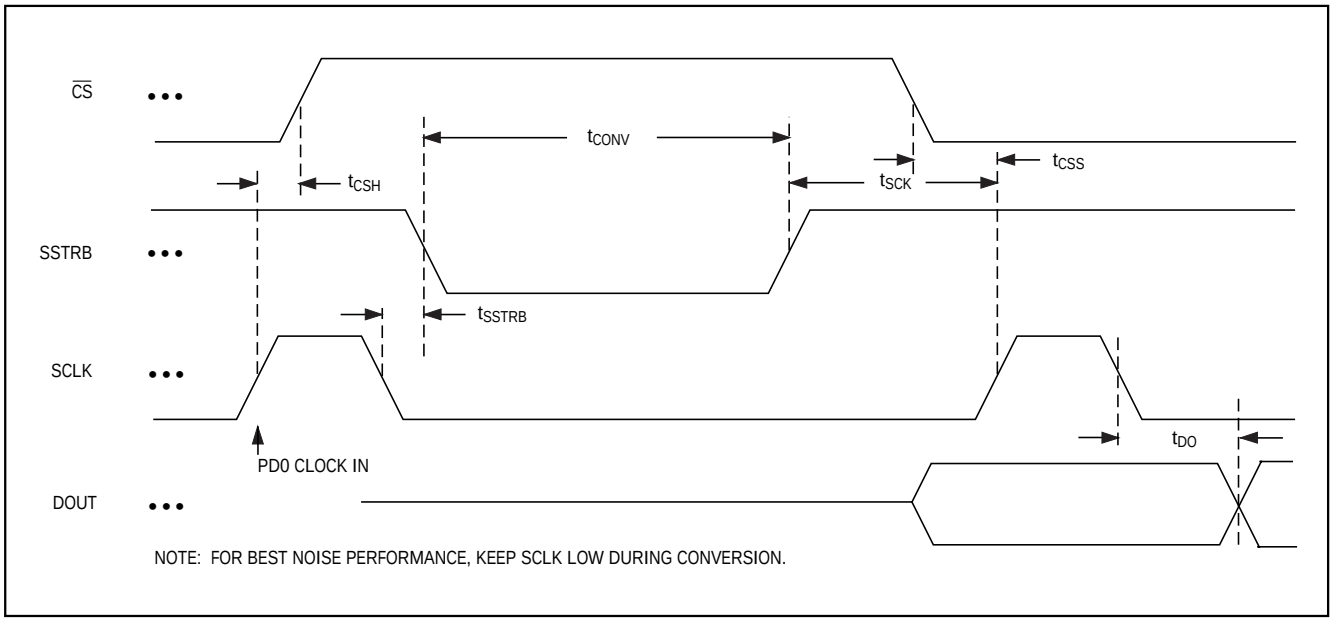


Figure 9. Internal Clock Mode SSTRB Detailed Timing

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

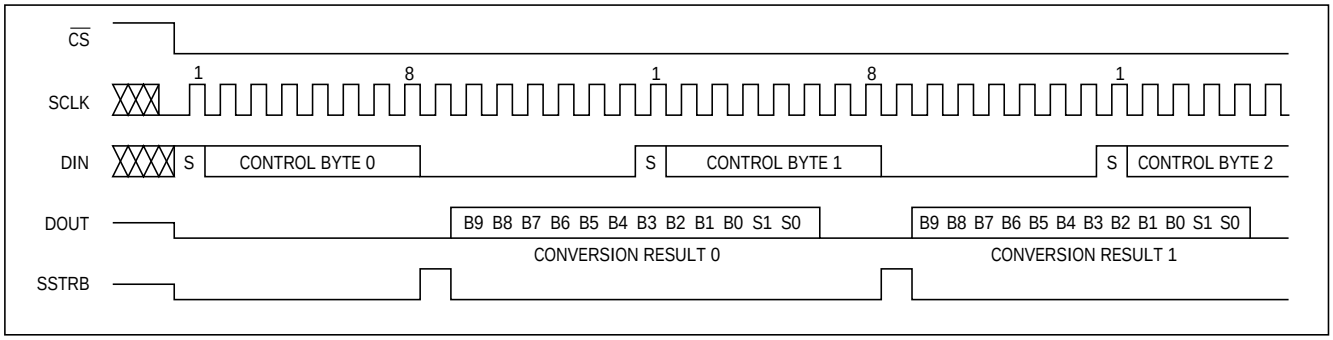


Figure 10a. External Clock Mode, 15 Clocks/Conversion Timing

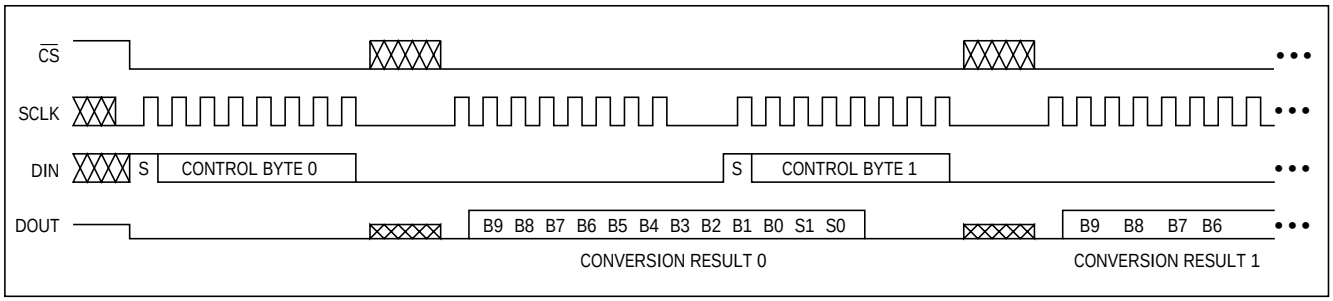


Figure 10b. External Clock Mode, 16 Clocks/Conversion Timing

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see *Choosing Power-Down Mode* and Table 4).

Pull $\overline{SHDN}$ high to select internal compensation. Internal compensation requires no external capacitor at VREF and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current typically to 2µA. Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, leakage currents at VREF cause droop on the reference bypass capacitor. Figures 11a and 11b show the various power-down sequences in both external and internal clock modes.

Table 4. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	VREF CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal	—	Fast	5	26
Enabled	Internal	—	Full	300	26
Enabled	External	4.7	Fast	See Figure 13c	133
Enabled	External	4.7	Full	See Figure 13c	133
Disabled	—	—	Fast	2	133
Disabled	—	—	Full	2	133

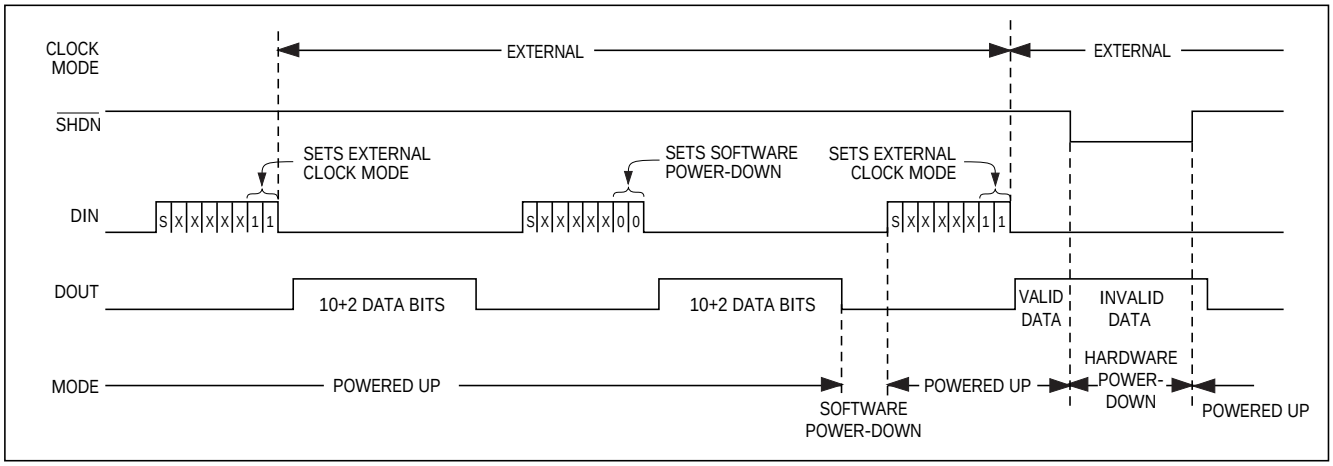


Figure 11a. Timing Diagram Power-Down Modes, External Clock

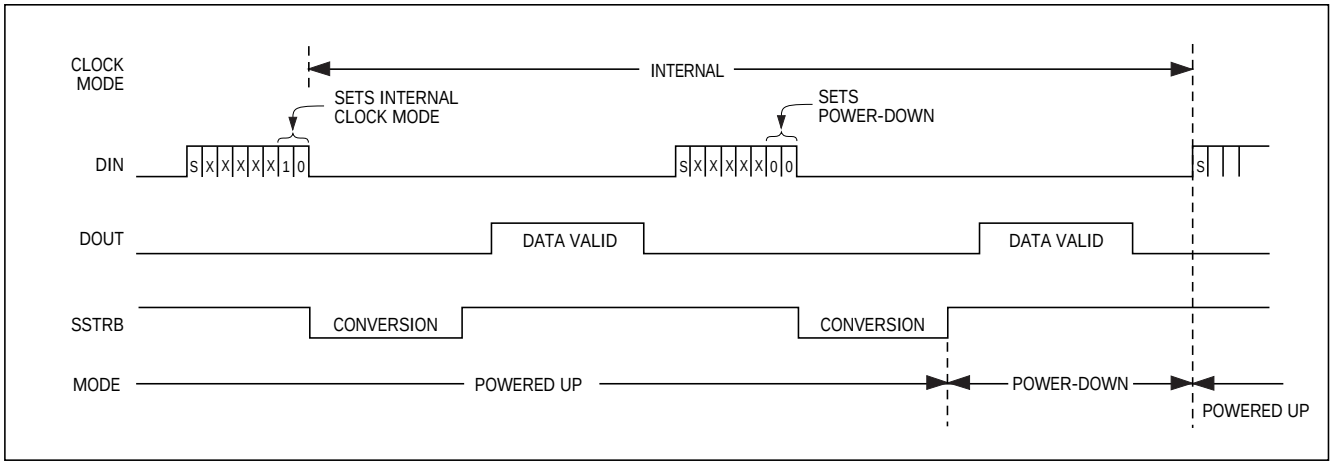


Figure 11b. Timing Diagram Power-Down Modes, Internal Clock

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

Table 5. Software Power-Down and Clock Mode

PD1	PD0	DEVICE
0	0	Full Power-Down
0	1	Fast Power-Down
1	0	Internal Clock
1	1	External Clock

Table 6. Hardware Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE-BUFFER COMPENSATION	INTERNAL CLOCK FREQUENCY
1	Enabled	Internal	225kHz
Floating	Enabled	External	1.8MHz
0	Power-Down	N/A	N/A

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1248/MAX1249 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1248/MAX1249. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz.

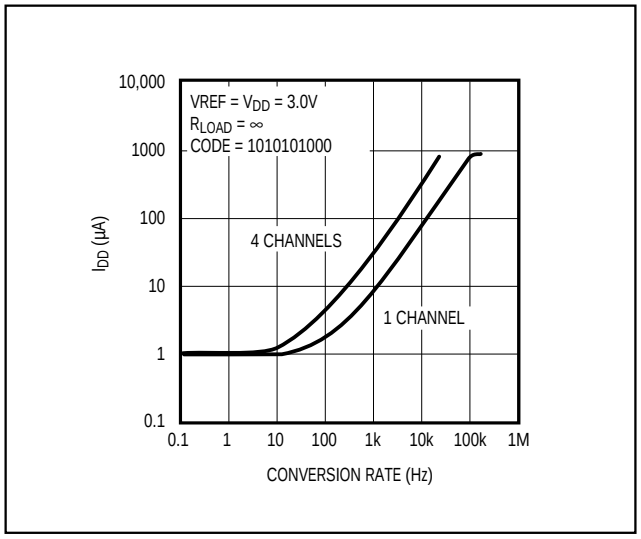


Figure 12. Average Supply Current vs. Conversion Rate with External Reference

This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX1248/MAX1249 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

Power-Down Sequencing

The MAX1248/MAX1249 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 12, 13a, and 13b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 13a depicts the MAX1248 power consumption for one or eight channel conversions, utilizing full power-down mode and internal-reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 10-bit accuracy, 8 time constants or 1.6ms are required after power-up. Waiting 1.6ms in FASTPD mode instead of in full power-up can reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 14.

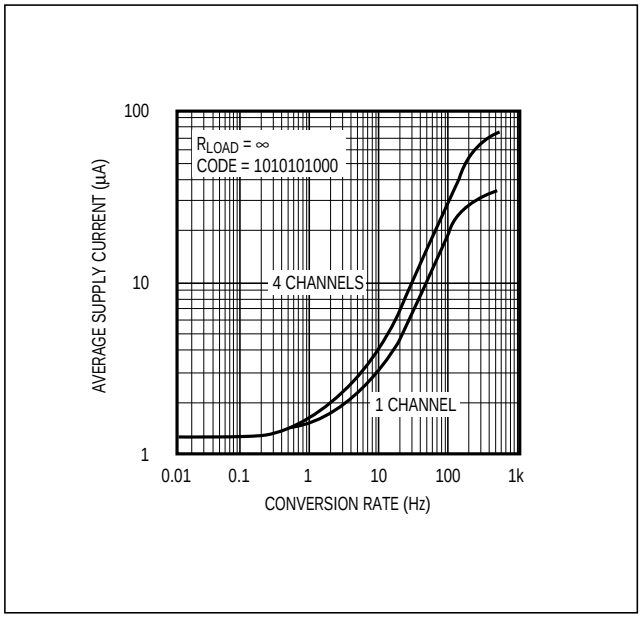


Figure 13a. MAX1248 Supply Current vs. Conversion Rate, FULLPD

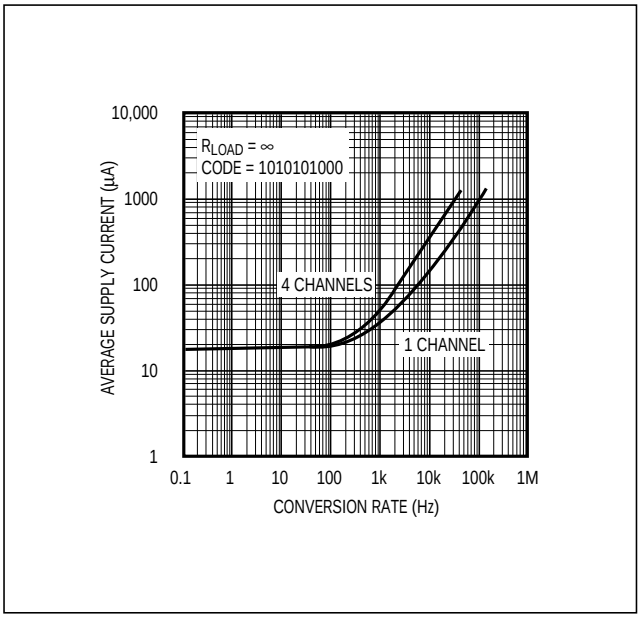


Figure 13b. MAX1248 Supply Current vs. Conversion Rate, FASTPD

Lowest Power at Higher Throughputs

Figure 13b shows the power consumption with external-reference compensation in fast power-down, with one and four channels converted. The external 4.7µF compensation requires a 75µs wait after power-up with one dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX1248/MAX1249 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

Internal and External References

The MAX1248 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX1249. An external reference can be connected directly at VREF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at VREF for both the MAX1248 and the MAX1249. The MAX1248's internally trimmed 1.21V reference is buffered with a gain of 2.06. The MAX1249's REFADJ pin is also buffered with a gain of 2.06 to scale an external 1.25V reference at REFADJ to 2.5V at VREF.

Internal Reference (MAX1248)

The MAX1248's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal-reference voltage is adjustable to ±1.5% with the circuit of Figure 15.

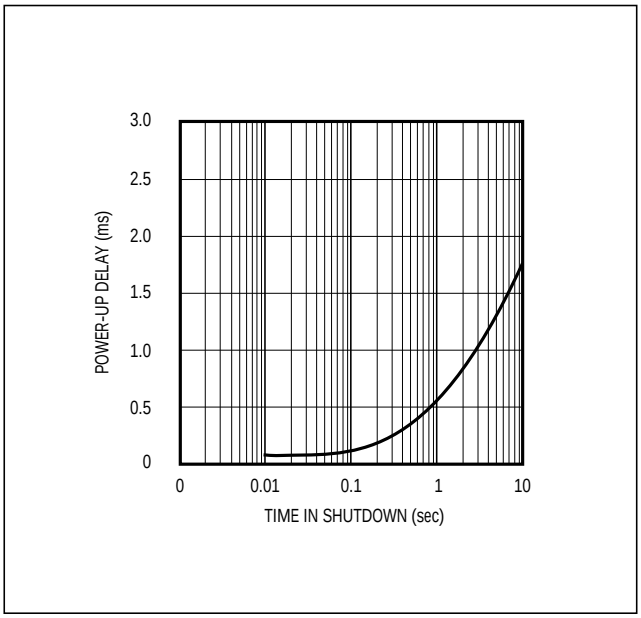


Figure 13c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

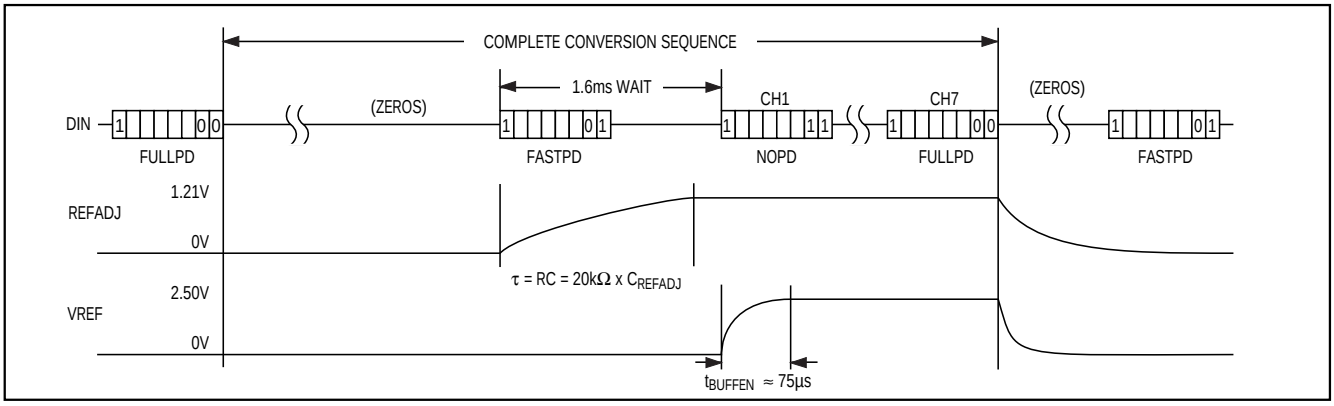


Figure 14. MAX1248 FULLPD/FASTPD Power-Up Sequence

External Reference

With both the MAX1248 and MAX1249, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX1248 and higher than 100kΩ for the MAX1249, where the internal reference is omitted. At VREF, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at VREF must deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ can be as much as 25µA with REFADJ tied to V_{DD}. Pull REFADJ to AGND to minimize the input bias current in power-down.

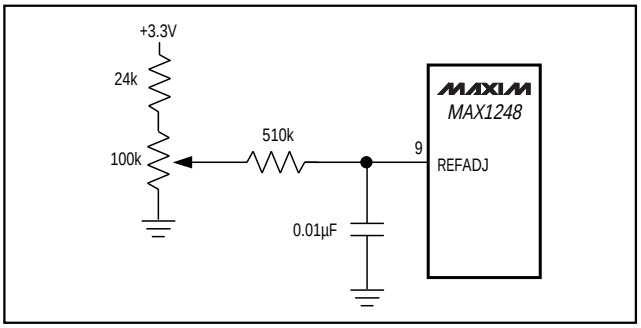


Figure 15. MAX1248 Reference-Adjust Circuit

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 20ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C.

Figure 16 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 17 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 2.44mV (2.500V / 1024) for unipolar operation and 1LSB = 2.44mV [(2.500V / 2 - -2.500V / 2) / 1024] for bipolar operation.

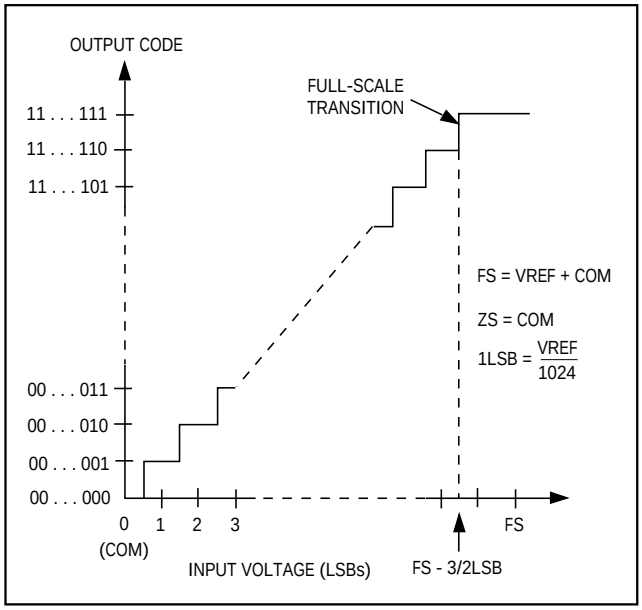


Figure 16. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

Table 7. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

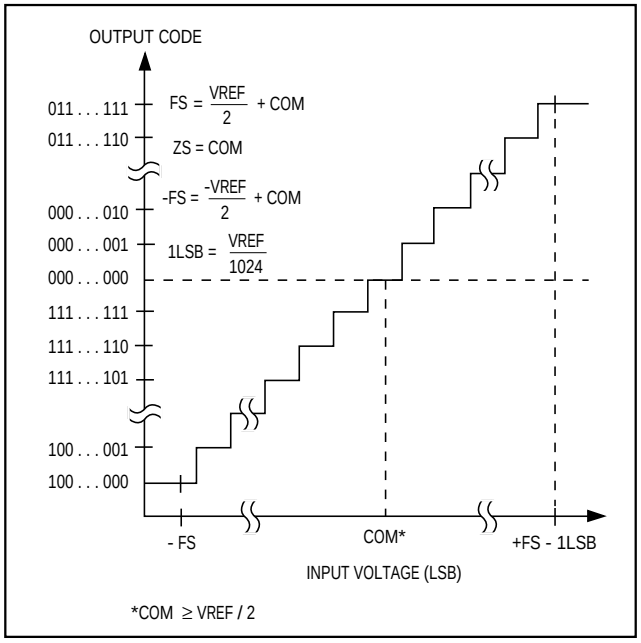


Figure 17. Bipolar Transfer Function, Zero Scale (ZS) = COM, Full Scale (FS) = VREF / 2 + COM

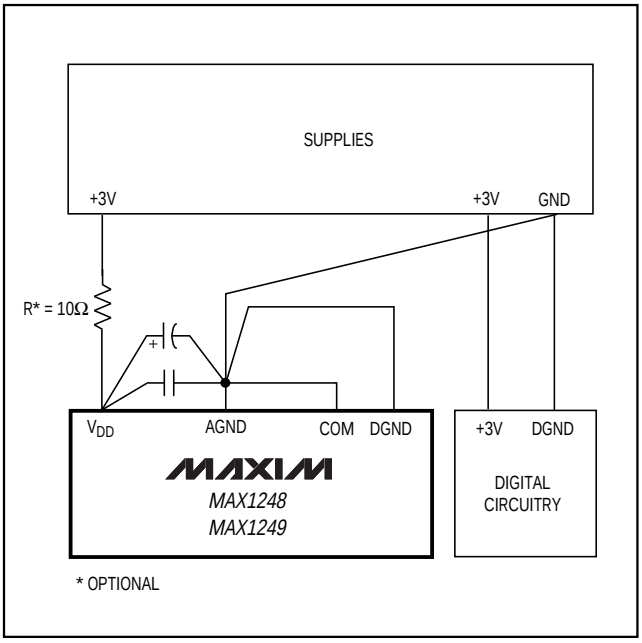


Figure 18. Power-Supply Grounding Connection

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to pin 1 of the MAX1248/MAX1249. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 18).

High-Speed Digital Interfacing with QSPI

The MAX1248/MAX1249 can interface with QSPI using the circuit in Figure 19 (f_{SCLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the four channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

The MAX1248/MAX1249 are QSPI compatible up to their maximum external clock frequency of 2MHz.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

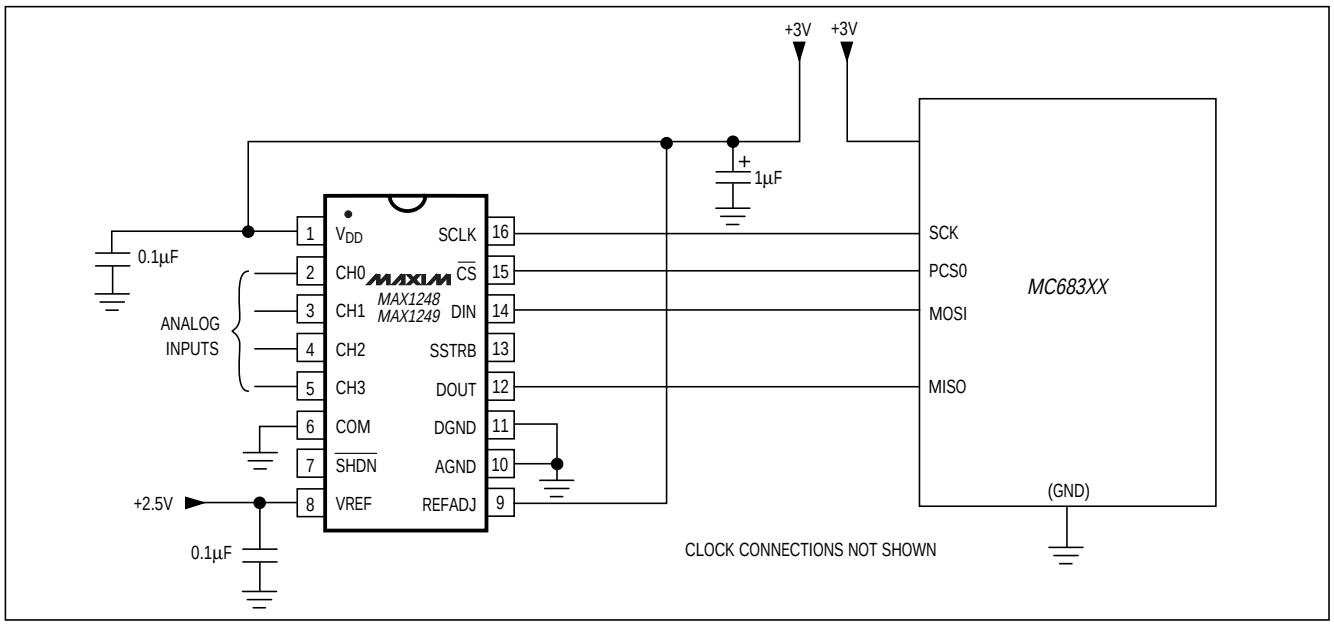


Figure 19. MAX1248/MAX1249 QSPI Connections External Reference

TMS320LC3x Interface

Figure 20 shows an application circuit to interface the MAX1248/MAX1249 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 21.

Use the following steps to initiate a conversion in the MAX1248/MAX1249 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1248/MAX1249's SCLK input.
2) The MAX1248/MAX1249's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX1248/MAX1249's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1248/MAX1249 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1248/MAX1249's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1248/MAX1249.

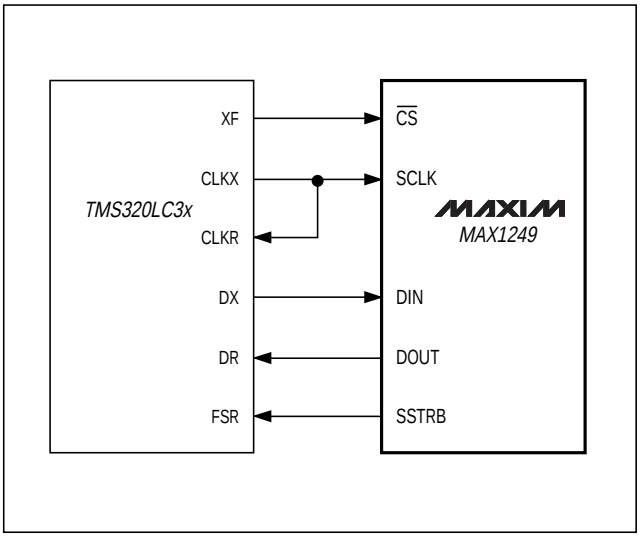


Figure 20. MAX1248/MAX1249-to-TMS320 Serial Interface

5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10 + 2-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1248/MAX1249 until the next conversion is initiated.

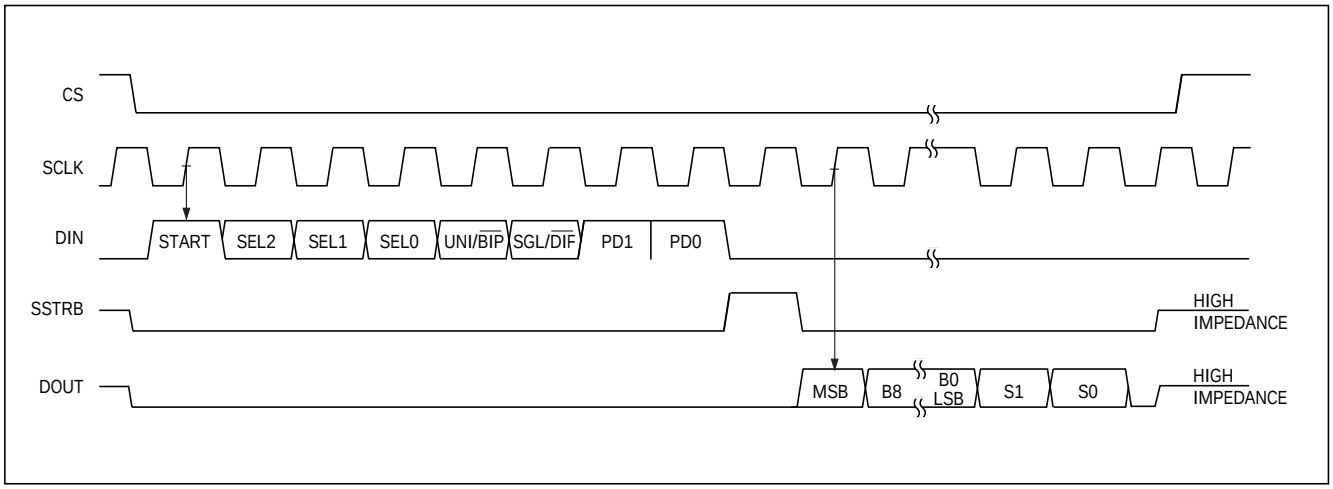


Figure 21. TMS320 Serial-Interface Timing Diagram

Ordering Information (continued)

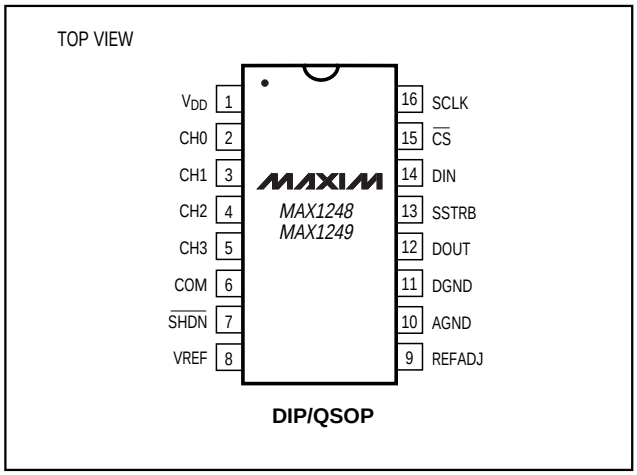
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1248AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1248BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1248AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1248BEEE	-40°C to +85°C	16 QSOP	±1
MAX1248AMJE	-55°C to +125°C	16 CERDIP*	±1/2
MAX1248BMJE	-55°C to +125°C	16 CERDIP*	±1
MAX1249ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1249BCPE	0°C to +70°C	16 Plastic DIP	±1

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1249ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1249BCEE	0°C to +70°C	16 QSOP	±1
MAX1249AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1249BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1249AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1249BEEE	-40°C to +85°C	16 QSOP	±1
MAX1249AMJE	-55°C to +125°C	16 CERDIP*	±1/2
MAX1249BMJE	-55°C to +125°C	16 CERDIP*	±1

† *Contact factory for availability of alternate surface-mount packages.*
* *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

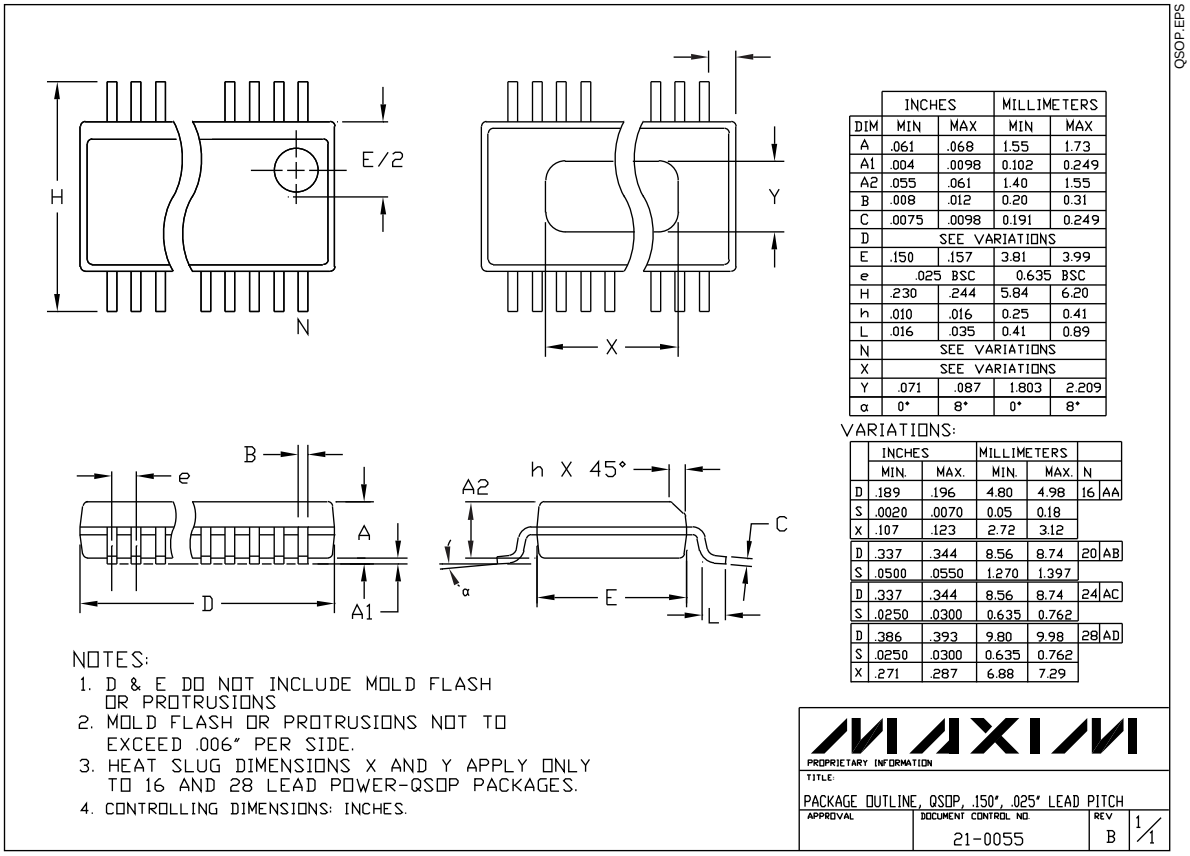
Pin Configuration



Chip Information

TRANSISTOR COUNT: 2554

Package Information

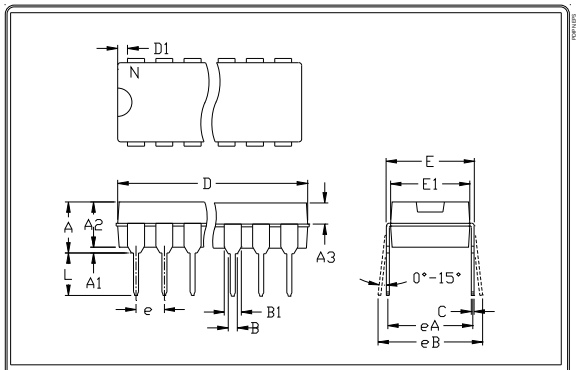


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

Package Information (continued)

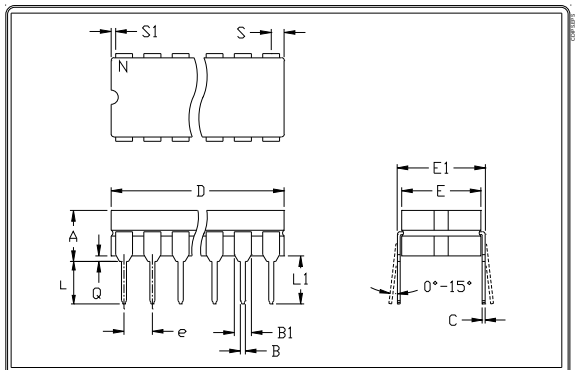


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A

NOTES

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX1249BCPE+ MAX1248BEEE+ MAX1249BEEE+ MAX1248ACEE+ MAX1248ACEE+T MAX1248ACPE+ MAX1248AEEE+ MAX1248AEEE+T MAX1248AEPE+ MAX1248BCEE+ MAX1248BCEE+T MAX1248BCPE+ MAX1248BEEE+T MAX1248BEPE+ MAX1249ACEE+ MAX1249ACEE+T MAX1249ACPE+ MAX1249AEEE+ MAX1249AEEE+T MAX1249BCEE+ MAX1249BCEE+T MAX1249BEEE+T MAX1249BEPE+ MAX1249AEPE+