

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

ABSOLUTE MAXIMUM RATINGS

All voltages are referenced to GND.

| | |
|---|-----------------------------------|
| V _{CC} | -0.3V to +4V |
| V _L | -0.3V to +4V |
| I/O V _{CC} | -0.3V to (V _{CC} + 0.3V) |
| I/O V _L | -0.3V to (V _L + 0.3V) |
| EN, $\overline{\text{EN}}$ | -0.3V to (V _L + 0.3V) |
| Short-Circuit Duration I/O V _L , I/O V _{CC} to GND | Continuous |
| Continuous Power Dissipation (T _A = +70°C) 6-Pin SC70 (derate 3.1mW/°C above +70°C) | 245mW |

| | |
|--|-----------------|
| 6-Bump UCSP (derate 3.9mW/°C above +70°C) | 308mW |
| 8-Bump UCSP (derate 4.7mW/°C above +70°C) | 379mW |
| 8-Pin SOT23 (derate 9.1mW/°C above +70°C) | 727mW |
| 12-Bump UCSP (derate 6.5mW/°C above +70°C) | 518.8mW |
| 14-Pin TSSOP (derate 9.1mW/°C above +70°C) | 727mW |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V), EN = V_L, $\overline{\text{EN}}$ = open (MAX3023 TSSOP package only), C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 40pF, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------|--|------|-----------------------|------|-------|
| POWER SUPPLY | | | | | | |
| V _L Supply Range | V _L | | 1.2 | V _{CC} - 0.4 | | V |
| V _{CC} Supply Range | V _{CC} | | 1.65 | 3.60 | | V |
| Supply Current from V _{CC} | I _{QVCC} | I/O V _{CC} = 0, I/O V _L = 0 or I/O V _{CC} = V _{CC} , I/O V _L = V _L | | 0.1 | 1 | µA |
| Supply Current from V _L | I _{QVL} | I/O V _{CC} = 0, I/O V _L = 0 or I/O V _{CC} = V _{CC} , I/O V _L = V _L | | 0.2 | 2 | µA |
| | | I/O V _{CC} = 0, I/O V _L = 0 or I/O V _{CC} = V _{CC} , I/O V _L = V _L , V _L < V _{CC} - 0.2V | | 10 | 100 | |
| V _{CC} Tri-state Output-Mode Supply Current | I _{TS-VCC} | T _A = +25°C, EN = 0 | | 0.03 | 1 | µA |
| V _L Tri-state Output-Mode Supply Current (MAX13013/MAX13014) | I _{TS-VL} | T _A = +25°C, EN = 0 | | 0.1 | 0.2 | µA |
| | | T _A = +25°C, EN = 0, V _L = V _{CC} - 0.2V | | 1 | 2 | |
| V _L Tri-state Output-Mode Supply Current (MAX3023 TSSOP Package Only) | I _{TS-VL} | T _A = +25°C, EN = 0 | | 50 | 70 | µA |
| | | T _A = +25°C, EN = 0, V _L = V _{CC} - 0.2V | | 55 | 74 | |
| I/O Tri-state Output-Mode Leakage Current | | T _A = +25°C, EN = 0 | | | 0.15 | µA |
| | | T _A = +25°C, EN = 0, V _L = V _{CC} - 0.2V | | | 20 | |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +1.65V$ to $+3.6V$, $V_L = +1.2V$ to $(V_{CC} - 0.4V)$, $EN = V_L$, $\overline{EN} = \text{open}$ (MAX3023 TSSOP package only), $C_{IOVL} \leq 15pF$, $C_{IOVCC} \leq 40pF$, $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ C$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|--|---------------------|---------------------|-----|------------|
| LOGIC-LEVEL THRESHOLDS | | | | | | |
| I/O V_L Input-Voltage High | V_{IHL} | | $2/3 \times V_L$ | | | V |
| I/O V_L Input-Voltage Low | V_{ILL} | | | $1/3 \times V_L$ | | V |
| Pullup Resistance on I/O V_L | | | 120 | | | Ω |
| Pulldown Resistance on I/O V_L | | | 75 | | | Ω |
| I/O V_{CC} Input-Voltage High | V_{IHC} | | $2/3 \times V_{CC}$ | | | V |
| I/O V_{CC} Input-Voltage Low | V_{ILC} | | | $1/3 \times V_{CC}$ | | V |
| Pullup Resistance on I/O V_{CC} | | | 2.5 | | | k Ω |
| Pulldown Resistance on I/O V_{CC} | | | 2.5 | | | k Ω |
| EN, \overline{EN} Input-Voltage High | V_{IH} | | $2/3 \times V_L$ | | | V |
| EN, \overline{EN} Input-Voltage Low | V_{IL} | | | $1/3 \times V_L$ | | V |
| EN Input Current | | MAX13013/MAX13014 | -5 | | +5 | μA |
| Pullup Resistance on EN | | MAX3023 | 46 | 62 | 81 | k Ω |
| Pulldown Resistance on \overline{EN} | | MAX3023, TSSOP package only | 46 | 62 | 81 | k Ω |
| I/O V_L Output-Voltage High | V_{OHL} | I/O V_L source current = 20 μA | $2/3 \times V_L$ | | | V |
| I/O V_L Output-Voltage Low | V_{OLL} | I/O V_L sink current = 20 μA | | $1/3 \times V_L$ | | V |
| I/O V_{CC} Output-Voltage High | V_{OHC} | I/O V_{CC} source current = 20 μA | $2/3 \times V_{CC}$ | | | V |
| I/O V_{CC} Output-Voltage Low | V_{OLC} | I/O V_{CC} sink current = 20 μA | | $1/3 \times V_{CC}$ | | V |

MAX13013/MAX13014/MAX3023

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TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +3.6V, V_L = +1.2V to (V_{CC} - 0.4V), EN = V_L , \overline{EN} = open (MAX3023 TSSOP package only), C_{IOVCC} \leq 15pF, C_{IOVCC} \leq 40pF, T_A = T_{MIN} to T_{MAX} . Typical values are at T_A = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|---|-----|-----|------|----------|
| I/O $V_{CC_}$ Rise Time | t_{RVCC} | C_{IOVCC} = 15pF, Figure 1 | | | 2.5 | ns |
| | | C_{IOVCC} = 20pF, Figure 1 | | | 3 | |
| | | C_{IOVCC} = 40pF, Figure 1 | | | 4 | |
| I/O $V_{CC_}$ Fall Time | t_{FVCC} | C_{IOVCC} = 15pF, Figure 1 | | | 2.5 | ns |
| | | C_{IOVCC} = 20pF, Figure 1 | | | 3 | |
| | | C_{IOVCC} = 40pF, Figure 1 | | | 4 | |
| I/O $V_{CC_}$ One-Shot Output Impedance | | | | | 18.5 | Ω |
| I/O V_L Rise Time | t_{RVL} | C_{IOVL} = 15pF, Figure 2 | | | 2.5 | ns |
| I/O V_L Fall Time | t_{FVL} | C_{IOVL} = 15pF, Figure 2 | | | 2.5 | ns |
| I/O V_L One-Shot Output Impedance | | | | | 12.5 | Ω |
| Propagation Delay, Driving I/O V_L | I/O V_L -VCC | C_{IOVCC} = 15pF, Figure 1 | | | 6.5 | ns |
| Propagation Delay, Driving I/O $V_{CC_}$ | I/O V_{CC} -VL | C_{IOVL} = 15pF, Figure 2 | | | 6 | ns |
| Part-to-Part Skew (Note 3) | t_{PPSKEW} | C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_{CC} = 2.5V, V_L = 1.8V | | | 4 | ns |
| Propagation Delay from I/O V_L to I/O $V_{CC_}$ after Enable | t_{EN-VCC} | C_{IOVCC} = 15pF, Figure 3 | | | 1000 | ns |
| Propagation Delay from I/O $V_{CC_}$ to I/O V_L after Enable | t_{EN-VL} | C_{IOVL} = 15pF, Figure 4 | | | 1000 | ns |
| Maximum Data Rate | | C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_L > 1.8V | 100 | | | Mbps |
| | | C_{IOVCC} = 15pF, C_{IOVL} = 15pF, V_L > 1.2V | 80 | | | |

Note 1: V_L must be less than or equal to V_{CC} - 0.4V during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

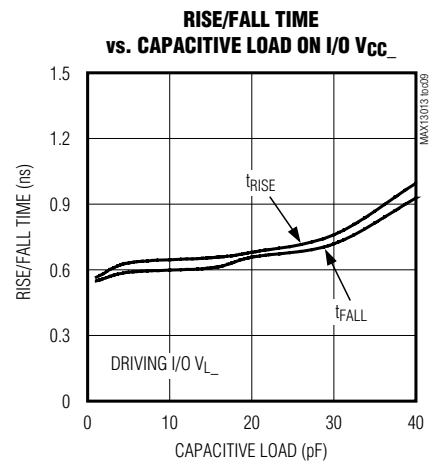
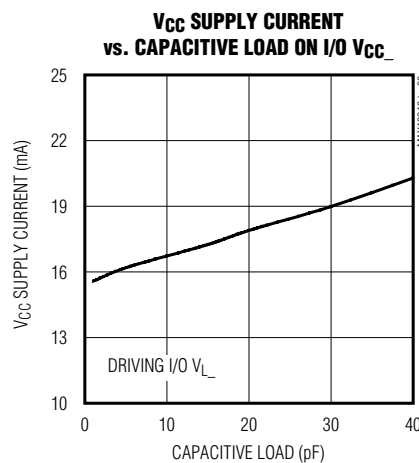
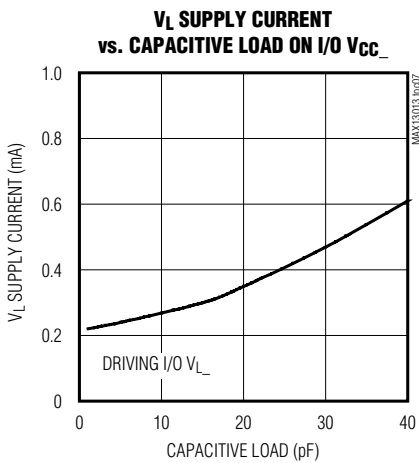
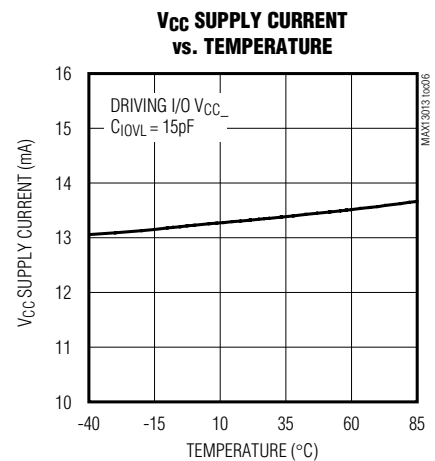
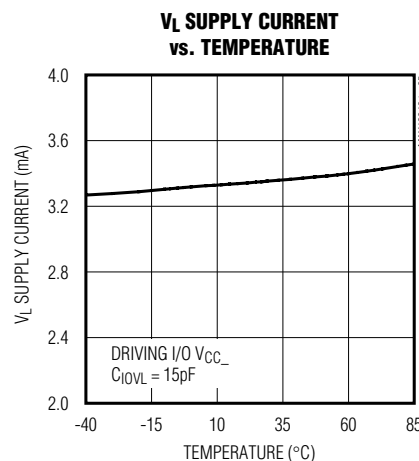
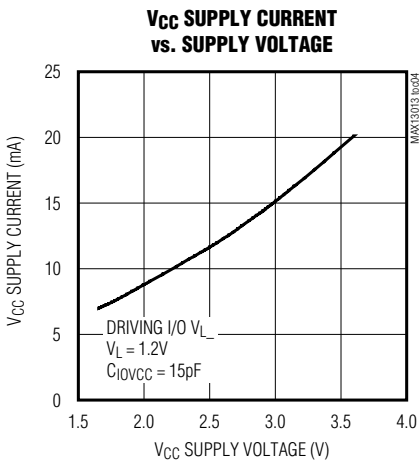
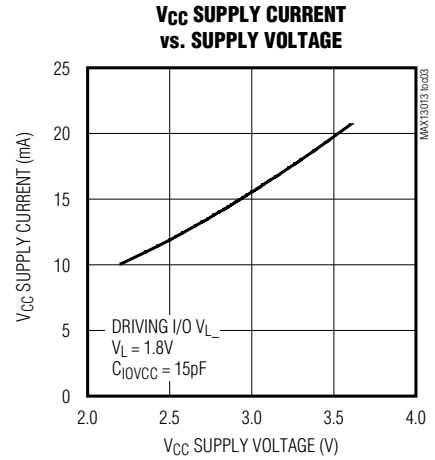
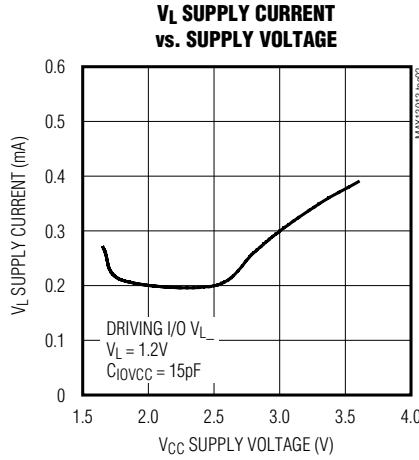
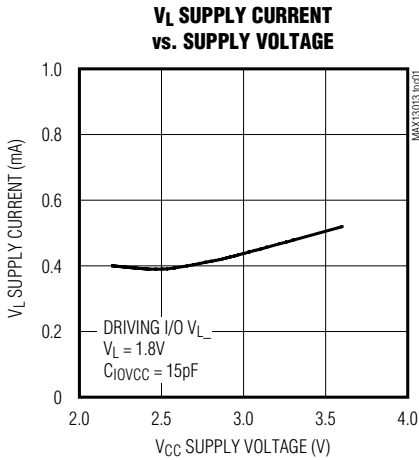
Note 3: Not production tested. Guaranteed by design.

+1.2V to +3.6V, 0.1μA, 100Mbps, Single-/Dual-/Quad-Level Translators

Typical Operating Characteristics

(Data rate = 100Mbps, $V_{CC} = 3.3V$, $V_L = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.)

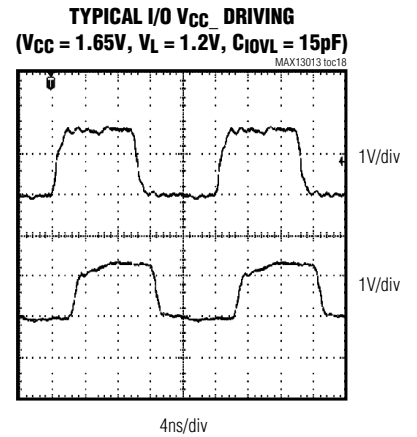
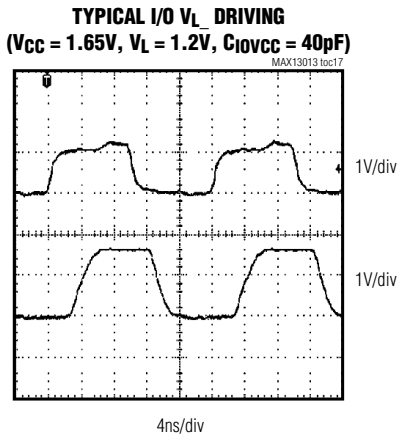
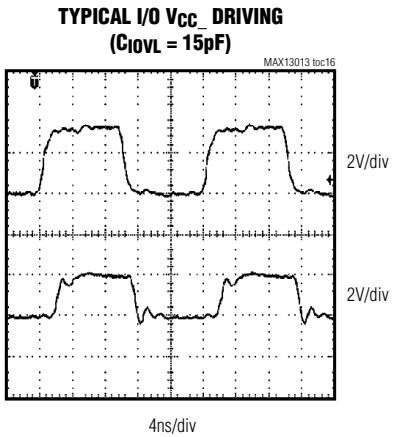
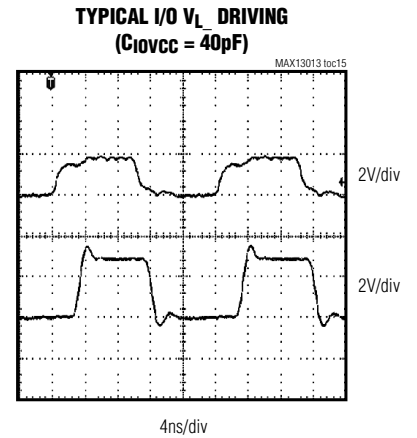
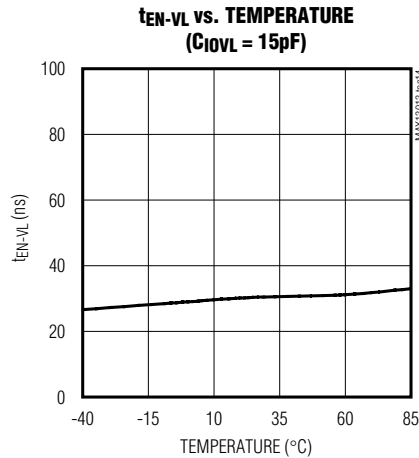
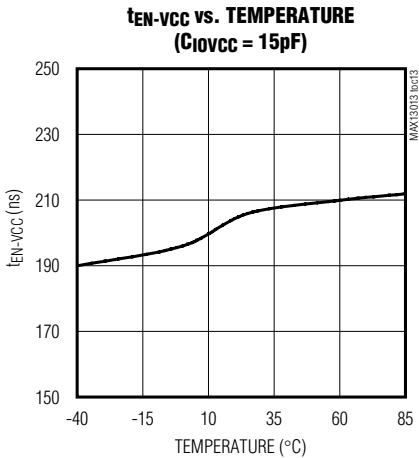
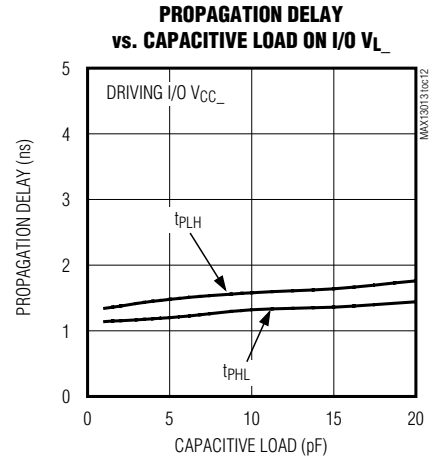
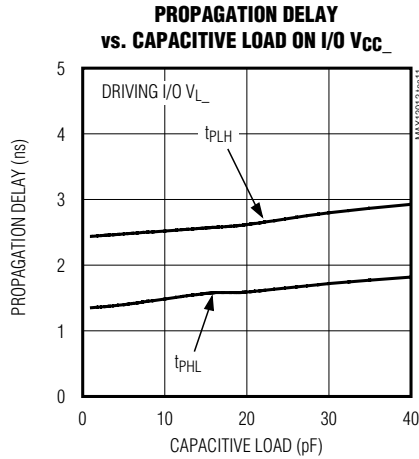
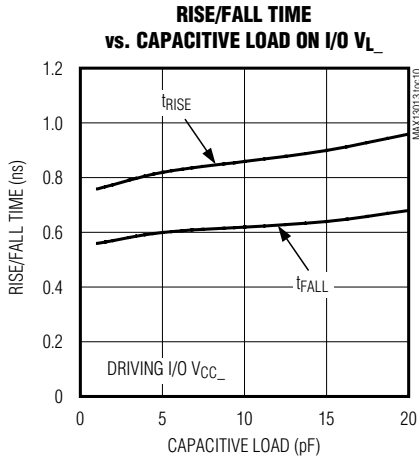
MAX13013/MAX13014/MAX3023



+1.2V to +3.6V, 0.1μA, 100Mbps, Single-/Dual-/Quad-Level Translators

Typical Operating Characteristics (continued)

(Data rate = 100Mbps, $V_{CC} = 3.3V$, $V_L = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.)



+1.2V to +3.6V, 0.1μA, 100Mbps, Single-/Dual-/Quad-Level Translators

Pin Description—MAX13013/MAX13014/ MAX3023 (Bidirectional Devices)

| PIN | | | | | | NAME | FUNCTION |
|---------|------------|----------|------------|----------|------------|------------------------|---|
| MAX3023 | | MAX13013 | | MAX13014 | | | |
| TSSOP | 4 x 3 UCSP | SC70 | 3 x 2 UCSP | SOT23 | 3 x 3 UCSP | | |
| 1 | A1 | 4 | B2 | 7 | A2 | I/O V _{L1} | Input/Output 1, Referenced to V _L |
| 2 | B2 | — | — | 6 | A3 | I/O V _{L2} | Input/Output 2, Referenced to V _L |
| 3 | A2 | 5 | B1 | 8 | A1 | V _L | V _L Input Voltage, +1.2V ≤ V _L ≤ V _{CC} - 0.4V. Bypass V _L to GND with a 0.1μF capacitor. |
| 4 | — | — | — | — | — | N.C. | No Connection |
| 5 | B3 | — | — | — | — | I/O V _{L3} | Input/Output 3, Referenced to V _L |
| 6 | A3 | — | — | — | — | I/O V _{L4} | Input/Output 4, Referenced to V _L |
| 7 | A4 | 6 | B3 | 5 | B1 | EN | Active-High Enable Input. If EN is pulled low, all inputs/outputs are in tristate. Drive EN high (V _L) for normal operation. |
| 8 | — | — | — | — | — | $\overline{\text{EN}}$ | Active-Low Enable Input. If $\overline{\text{EN}}$ is pulled high (V _L), all inputs/outputs are in tri-state. Drive $\overline{\text{EN}}$ low for normal operation (MAX3023 TSSOP package only). |
| 9 | B4 | — | — | — | — | I/O V _{CC4} | Input/Output 4, Referenced to V _{CC} |
| 10 | C4 | — | — | — | — | I/O V _{CC3} | Input/Output 3, Referenced to V _{CC} |
| 11 | C3 | 2 | A3 | 4 | B3 | GND | Ground |
| 12 | C2 | 1 | A1 | 1 | C1 | V _{CC} | V _{CC} Input Voltage, +1.65V ≤ V _{CC} ≤ +3.6V. Bypass V _{CC} to GND with a 0.1μF capacitor. |
| 13 | C1 | — | — | 3 | C3 | I/O V _{CC2} | Input/Output 2, Referenced to V _{CC} |
| 14 | B1 | 3 | A2 | 2 | C2 | I/O V _{CC1} | Input/Output 1, Referenced to V _{CC} |

MAX13013/MAX13014/MAX3023

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Test Circuits/Timing Diagrams

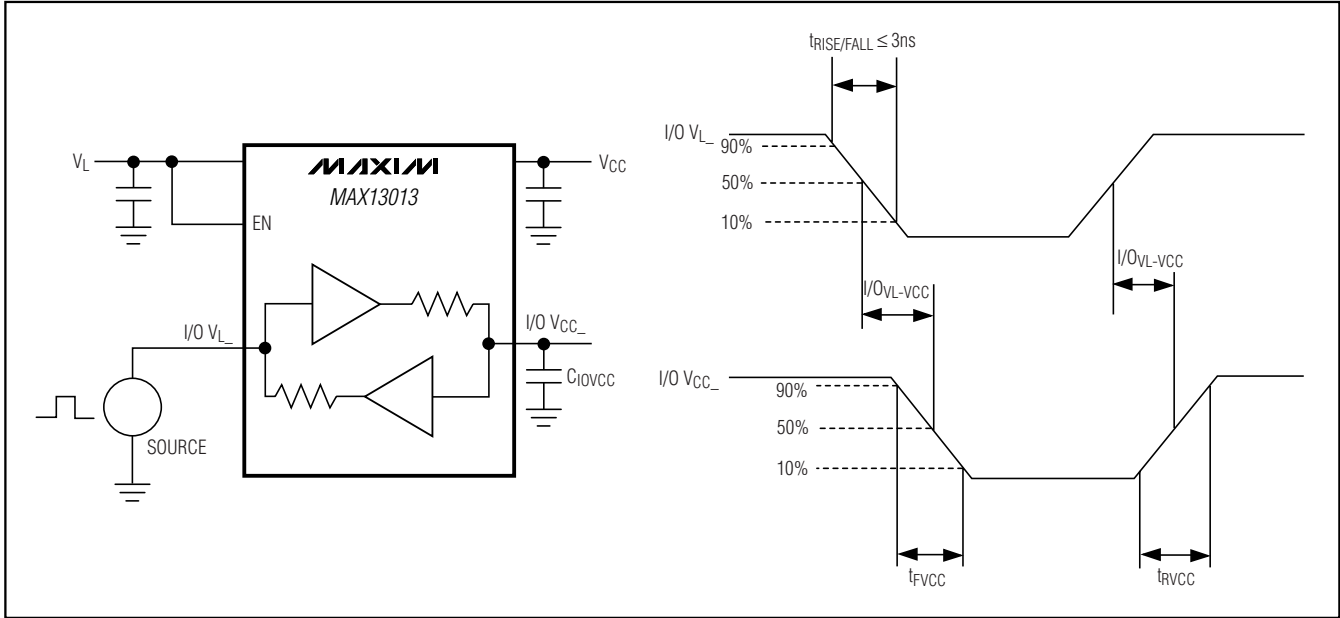


Figure 1. Driving I/O V_L_ Test Circuit and Timing

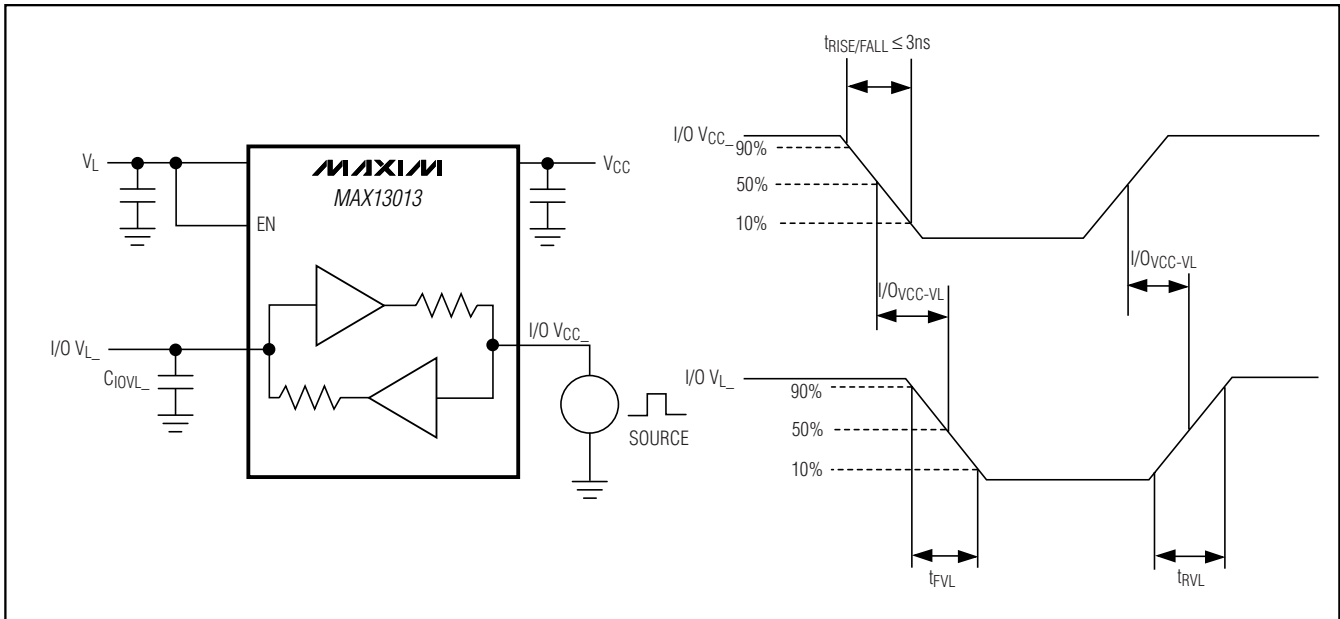


Figure 2. Driving I/O V_{CC}_ Test Circuit and Timing

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Test Circuits/Timing Diagrams (continued)

MAX13013/MAX13014/MAX3023

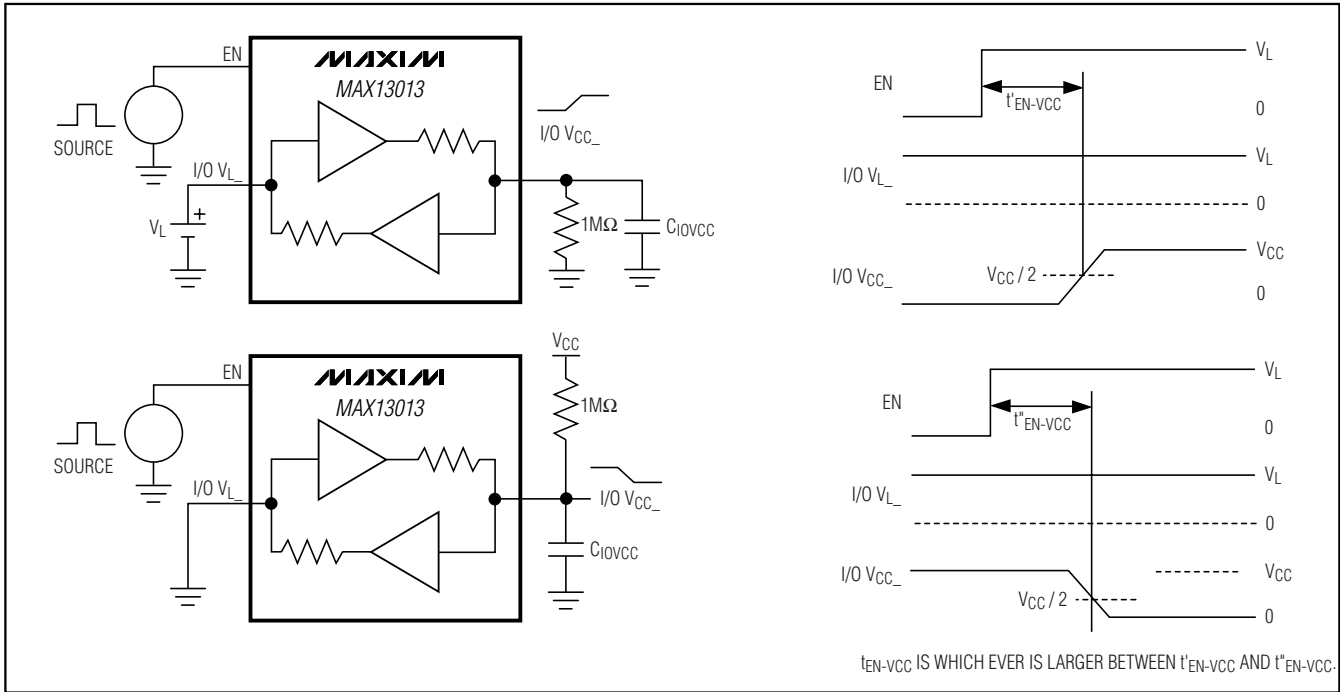


Figure 3. Propagation Delay from I/O VL₋ to I/O VCC₋ After EN

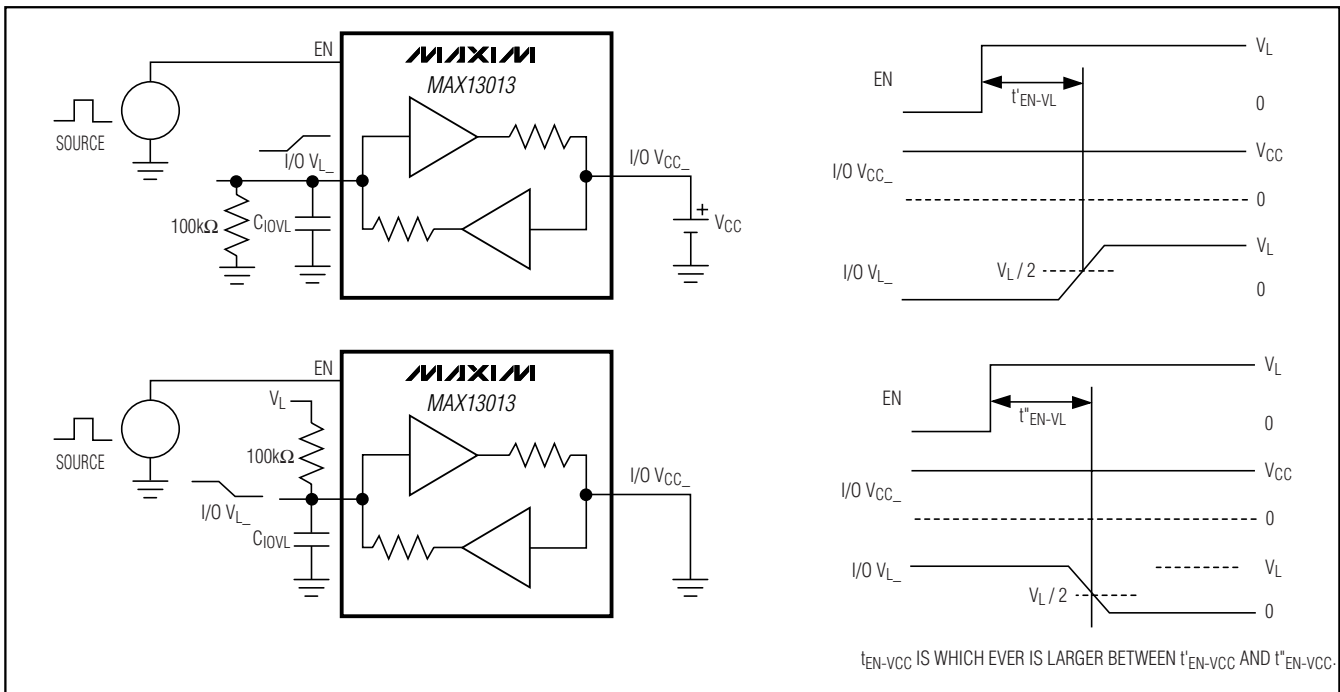


Figure 4. Propagation Delay from I/O VCC₋ to I/O VL₋ After EN

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Detailed Description

The MAX13013/MAX13014/MAX3023 logic-level translators provide the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher-voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX13013/MAX13014/MAX3023 bidirectional level translators allow data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX13013/MAX13014/MAX3023 accept V_L from +1.2V to ($V_{CC} - 0.4V$) and operate with V_{CC} from +1.65V to +3.6V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

When in tri-state mode, the MAX13013/MAX13014/MAX3023 reduce the V_{CC} supply current to 0.03µA, and the V_L supply current to 0.1µA. These devices operate at a guaranteed data rate of 100Mbps for $V_L > 1.8V$.

Level Translation

For proper operation, ensure that $+1.65V \leq V_{CC} \leq +3.6V$, and $+1.2V \leq V_L \leq V_{CC} - 0.4V$. During power-up sequencing, $V_L \geq V_{CC}$ does not damage the device. During power-supply sequencing, when V_{CC} is floating and V_L is powering up, up to 40mA current can be sourced to each load on the V_L side, without the device latching up. The maximum data rate depends heavily on

the load capacitance (see the *Typical Operating Characteristics Rise/Fall Time* graph), output impedance of the driver, and the operating voltage range (Table 1).

Input Driver Requirements

The MAX13013/MAX13014/MAX3023 architecture is based on a one-shot accelerator output stage (see Figure 5). Accelerator output stages are in tri-state mode except when there is a transition on any of the translators on the input side, either I/O V_L or I/O V_{CC} . A short pulse is then generated during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to the architecture, both sides become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior simply helps to speed up the transition on the driven side.

For proper operation, the driver has to meet the following conditions: less than 25Ω output impedance and greater than 20mA peak output current capability.

Table 1. Data Rate

| V_L (V) | GUARANTEED DATA RATE (Mbps) |
|----------------|-----------------------------|
| $V_L < 1.8$ | 80 |
| $V_L \geq 1.8$ | 100 |

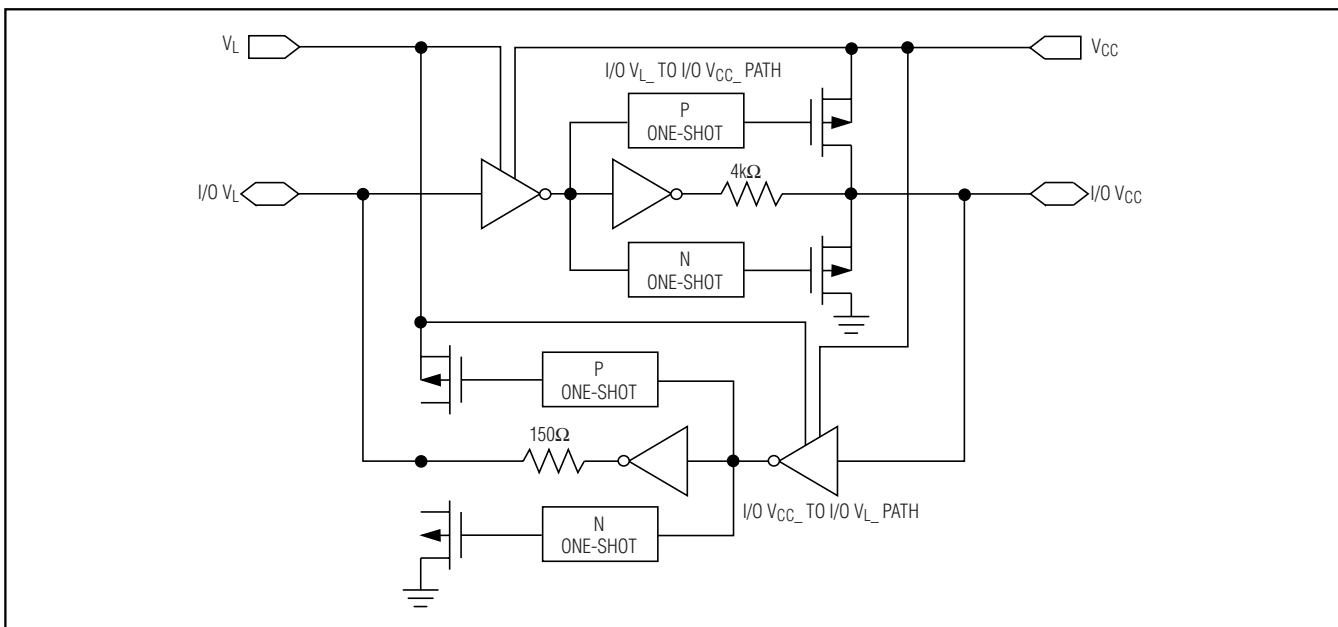


Figure 5. Simplified Functional Diagram (One I/O Line)

+1.2V to +3.6V, 0.1μA, 100Mbps, Single-/Dual-/Quad-Level Translators

Figure 6 shows a graph of typical input current versus input voltage.

Output Load Requirements

The MAX13013/MAX13014/MAX3023 I/O are designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ. Also, do not place an RC circuit at the input of these devices to slow down the edges. If a slower rise/fall time is required, refer to the MAX3000E/MAX3001E logic-level-translators data sheet.

For I²C level translation, refer to the MAX3372E-MAX3379E/MAX3390E-MAX3393E data sheet.

Enable Inputs

The MAX13013 single-, the MAX13014 dual- and the MAX3023 (UCSP package) quad-level translators feature an EN input. The MAX3023 (TSSOP package) quad-level translator features both EN and $\overline{\text{EN}}$ inputs (see Table 2 for operating mode). Note that the MAX3023 (TSSOP package) has internal pullup and pulldown circuitry on EN and $\overline{\text{EN}}$, respectively. If left unconnected, EN is pulled up to V_L and $\overline{\text{EN}}$ is pulled down to GND.

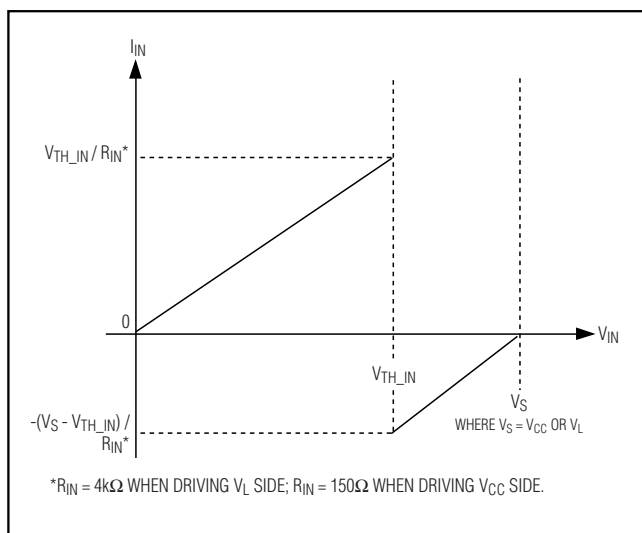


Figure 6. Typical I_{IN} vs. V_{IN}

**Table 2. MAX3023 (TSSOP Package)
Operating Mode**

| EN | $\overline{\text{EN}}$ | OPERATING MODE |
|----------------|------------------------|---|
| 0 | 0 | Both I/O V _L and I/O V _{CC} are in tri-state. |
| V _L | 0 | Normal operation. |
| 0 | V _L | Both I/O V _L and I/O V _{CC} are in tri-state. |
| V _L | V _L | Both I/O V _L and I/O V _{CC} are in tri-state. |

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with a 0.1μF ceramic capacitor. Place all capacitors as close to the power-supply inputs as possible.

Unidirectional vs. Bidirectional Level Translator

The MAX13013/MAX13014/MAX3023 bidirectional translators can operate as a unidirectional device to translate signals without inversion. These devices provide the smallest solution (UCSP package) for unidirectional level translation without inversion.

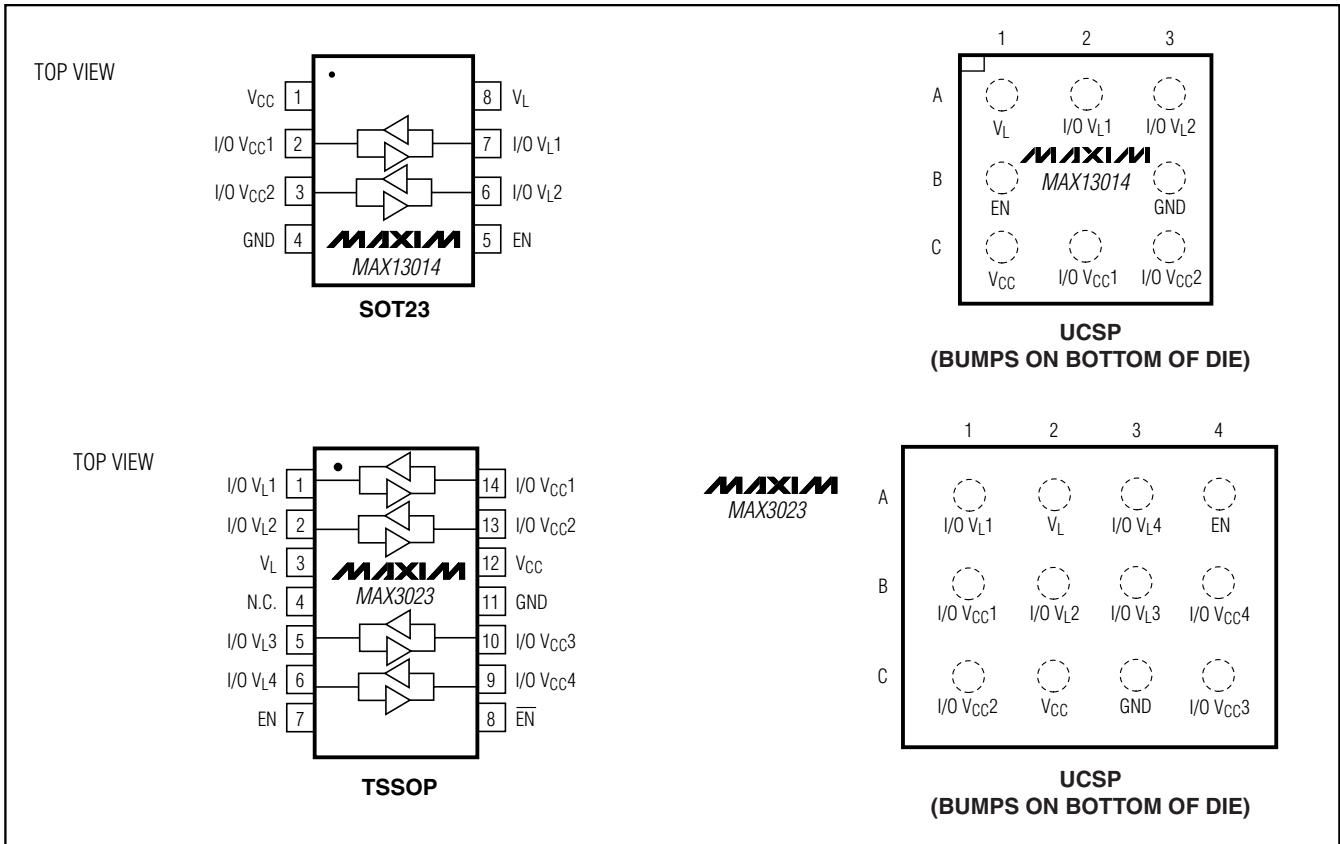
UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profiles, as well as the latest information on reliability testing results, go to Maxim's web site at www.maxim-ic.com/ucsp to find the Application Note: *UCSP—A Wafer-Level Chip-Scale Package*.

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Pin Configurations (continued)



Ordering Information/Selector Guide (continued)

| PART | TEMP RANGE | PIN-PACKAGE | PACKAGE CODE | TOP MARK | NUMBER OF $V_L \rightarrow V_{CC}$ TRANSLATORS | Number of $V_{CC} \rightarrow V_L$ TRANSLATORS | EN | \overline{EN} |
|--------------------|----------------|---------------|--------------|----------|--|--|----|-----------------|
| MAX13013EBT-T | -40°C to +85°C | 3 x 2 UCSP-6 | B6-1 | ADF | 1 | 1 | ✓ | — |
| MAX13014EKA | -40°C to +85°C | 8 SOT23 | — | AEKB | 2 | 2 | ✓ | — |
| MAX13014EBL-T | -40°C to +85°C | 3 x 3 UCSP-9 | B9-2 | AEN | 2 | 2 | ✓ | — |
| MAX3023EUD | -40°C to +85°C | 14 TSSOP | — | — | 4 | 4 | ✓ | ✓ |
| MAX3023EBC-T | -40°C to +85°C | 4 x 3 UCSP-12 | B12-1 | ABW | 4 | 4 | ✓ | — |

Chip Information

TRANSISTOR COUNT:

MAX13013: 261

MAX13014: 444

MAX3023: 791

PROCESS: BiCMOS

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX13013/MAX13014/MAX3023

Top view diagram showing dimensions: D (width), E (height), HE (total height), e (lead pitch), b (lead width), PIN 1 (location), and MARKING (orientation).

Side view diagram showing dimensions: L1 (lead length), L (lead thickness), Q1 (lead width), c (lead width), and DATUM 'A' (reference point).

| COMMON DIMENSIONS | | |
|-------------------|------------|------|
| SYMBOL | MIN | MAX |
| A | 0.80 | 1.10 |
| A1 | 0.00 | 0.10 |
| A2 | 0.80 | 1.00 |
| b | 0.15 | 0.30 |
| c | 0.10 | 0.18 |
| D | 1.80 | 2.20 |
| e | 0.65 BSC. | |
| E | 1.15 | 1.35 |
| HE | 1.80 | 2.40 |
| L | 0.10 | 0.41 |
| L1 | 0.425 TYP. | |
| Q1 | 0.10 | 0.40 |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

Bottom view diagram showing dimensions: A1 (lead thickness), A2 (lead height), and A (total height).

DALLAS SEMICONDUCTOR **MAXIM**

TITLE: PACKAGE OUTLINE, 6L SC70

| | | |
|----------|---------------------------------|------------|
| APPROVAL | DOCUMENT CONTRL. NO. 21-0077 | REV. C 1/1 |
|----------|---------------------------------|------------|

-DRAWING NOT TO SCALE-

SC70, 6LEPS

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

TOP VIEW

| COMMON DIMENSIONS | |
|-------------------|----------------|
| A | 0.62±0.05-0.08 |
| A1 | 0.29±0.02 |
| A2 | 0.33 REF. |
| b | ∅0.35±0.03 |
| D1 | 0.50 BASIC |
| E1 | 1.00 BASIC |
| e | 0.50 BASIC |
| SD | 0.25 BASIC |
| SE | 0.00 BASIC |

| PKG. CODE | VARIABLE DIMENSIONS | | DEPOPULATED SOLDER BALLS |
|-----------|---------------------|-----------|--------------------------|
| | D | E | |
| B6-1 | 1.00±0.05 | 1.52±0.05 | NONE |
| B6-2 | 1.00±0.05 | 1.52±0.05 | B2 |
| B6-3 | 1.05±0.05 | 1.57±0.05 | NONE |
| B6-4 | 1.05±0.05 | 1.57±0.05 | B2 |
| B6-5 | 0.97±0.05 | 1.46±0.05 | NONE |
| B6-6 | 1.16±0.05 | 1.57±0.05 | NONE |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

BOTTOM VIEW

SIDE VIEW

| | | | |
|-----------------------------|----------------------|--------------|-----|
| DALLAS SEMICONDUCTOR | | MAXIM | |
| PROPRIETARY INFORMATION | | | |
| TITLE: | | | |
| PACKAGE OUTLINE, 3x2 UCSP | | | |
| APPROVAL | DOCUMENT CONTROL NO. | REV. | 1/1 |
| | 21-0097 | G | |

6L, UCSPLEFS

+1.2V to +3.6V, 0.1 μ A, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

| SYMBOL | MIN | MAX |
|----------|-------------|-------------|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.28 | 0.45 |
| C | 0.09 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.30 | 0.60 |
| L2 | 0.25 BSC. | |
| e | 0.65 BSC. | |
| e1 | 1.95 REF. | |
| θ | 0 $^\infty$ | 8 $^\infty$ |

SOT23, 8L, EPS

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM \bar{y} MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

| | | | |
|----------|---------------------------------|-----------|-----|
| APPROVAL | DOCUMENT CONTROL NO. 21-0078 | REV. D | 1/1 |
|----------|---------------------------------|-----------|-----|

MAX13013/MAX13014/MAX3023

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

TOP VIEW

BOTTOM VIEW

| COMMON DIMENSIONS | |
|-------------------|----------------|
| A | 0.62±0.05-0.08 |
| A1 | 0.29±0.02 |
| A2 | 0.33 REF. |
| b | ∅0.35±0.03 |
| D1 | 1.00 BASIC |
| E1 | 1.00 BASIC |
| e | 0.50 BASIC |
| SD | 0.00 BASIC |
| SE | 0.00 BASIC |

| PKG. CODE | VARIABLE DIMENSIONS | | DEPOPULATED SOLDER BALLS |
|-----------|---------------------|-----------|--------------------------|
| | D | E | |
| B9-1 | 1.52±0.05 | 1.52±0.05 | NONE |
| B9-2 | 1.52±0.05 | 1.52±0.05 | B2 |
| B9-3 | 1.52±0.05 | 1.52±0.05 | B1, B2, B3 |
| B9-4 | 1.60±0.05 | 1.60±0.05 | NONE |
| B9-5 | 1.60±0.05 | 1.60±0.05 | B2 |
| B9-6 | 1.60±0.05 | 1.60±0.05 | B1, B2, B3 |

NOTES:
 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

SIDE VIEW

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 3x3 UCSP

| | | |
|-----------|---------------------------------|------------|
| APPROVAL: | DOCUMENT CONTROL NO. 21-0093 | REV. 1 1/1 |
|-----------|---------------------------------|------------|

9LUCSP, 3x3.EPS

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX13013/MAX13014/MAX3023

TSSOP4.40mm.EPS

TOP VIEW

BOTTOM VIEW

SIDE VIEW

END VIEW

DETAIL A

LEAD TIP DETAIL

| SYMBOL | COMMON DIMENSIONS | | | |
|----------------|-------------------|------|----------------|------|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | — | 1.10 | — | .043 |
| A ₁ | 0.05 | 0.15 | .002 | .006 |
| A ₂ | 0.85 | 0.95 | .033 | .037 |
| b | 0.19 | 0.30 | .007 | .012 |
| b ₁ | 0.19 | 0.25 | .007 | .010 |
| c | 0.09 | 0.20 | .004 | .008 |
| c ₁ | 0.09 | 0.14 | .004 | .006 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BSC | | .026 BSC | |
| H | 6.25 | 6.55 | .246 | .258 |
| L | 0.50 | 0.70 | .020 | .028 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

| JEDEC | N | VARIATIONS | | | | |
|-------|----|-------------|------|--------|------|------|
| | | MILLIMETERS | | INCHES | | |
| | | MIN. | MAX. | MIN. | MAX. | |
| AB-1 | 14 | D | 4.90 | 5.10 | .193 | .201 |
| AB | 16 | D | 4.90 | 5.10 | .193 | .201 |
| AC | 20 | D | 6.40 | 6.60 | .252 | .260 |
| AD | 24 | D | 7.70 | 7.90 | .303 | .311 |
| AE | 28 | D | 9.60 | 9.80 | .378 | .386 |

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS

△ THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP 4.40mm BODY

| | | |
|----------|---------------------------------|------------|
| APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F 1/1 |
|----------|---------------------------------|------------|

+1.2V to +3.6V, 0.1µA, 100Mbps, Single-/Dual-/Quad-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

TOP VIEW

| COMMON DIMENSIONS | |
|-------------------|----------------|
| A | 0.62±0.05-0.08 |
| A1 | 0.29±0.02 |
| A2 | 0.33 REF. |
| b | ∅0.35±0.03 |
| D1 | 1.00 BASIC |
| E1 | 1.50 BASIC |
| e | 0.50 BASIC |
| SD | 0.00 BASIC |
| SE | 0.25 BASIC |

| PKG. CODE | VARIABLE DIMENSIONS | | DEPOPULATED SOLDER BALLS |
|-----------|---------------------|-----------|--------------------------|
| | D | E | |
| B12-1 | 1.54±0.05 | 2.02±0.05 | NONE |
| B12-2 | 1.54±0.05 | 2.02±0.05 | B3 |
| B12-3 | 1.54±0.05 | 2.12±0.05 | NONE |
| B12-4 | 1.54±0.05 | 2.02±0.05 | B2, B3 |
| B12-5 | 1.64±0.05 | 2.12±0.05 | B2 |
| B12-6 | 1.64±0.05 | 2.12±0.05 | B3 |
| B12-7 | 1.54±0.05 | 2.02±0.05 | B1, B3 |
| B12-8 | 1.54±0.05 | 2.02±0.05 | B2 |
| B12-9 | 1.54±0.05 | 2.12±0.05 | B2, B3 |
| B12-10 | 1.54±0.05 | 2.02±0.05 | B1, B2, B3, B4 |
| B12-11 | 1.54±0.05 | 2.02±0.05 | A2, C3 |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

SIDE VIEW

BOTTOM VIEW

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 4x3 UCSP

| | | |
|----------|---------------------------------|------------|
| APPROVAL | DOCUMENT CONTROL NO. 21-0104 | REV. F 1/1 |
|----------|---------------------------------|------------|

12L UCSP 4x3.EPS

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