

SFP Copper-Cable Preemphasis Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}-0.5V to +6.0V
 Continuous CML Output Current
 at OUT+, OUT-.....-25mA to +25mA
 Voltage at IN+, IN-, LOSLEV, LOS,
 TX_DISABLE, PE0, PE1, OUTLEV.....-0.5V to ($V_{CC} + 0.5V$)

LOS Open Collector Supply Voltage
 with $\geq 4.7k\Omega$ Pullup Resistor.....-0.5V to +5.5V
 Continuous Power Dissipation at +85°C
 (derate 20.8mW/°C above +85°C).....1.35W
 Operating Junction Temperature Range (T_J).....-55°C to +150°C
 Storage Ambient Temperature Range (T_S).....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to +3.6V, $T_A = 0^\circ C$ to +85°C. Typical values are at $T_A = +25^\circ C$ and $V_{CC} = +3.3V$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		TX_DISABLE=low		75	97	mA
Inrush Current		Current beyond steady-state current			10	mA
Power-On-Reset Delay	tPOR		1		40	ms
OPERATING CONDITIONS						
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply-Noise Tolerance		1MHz $\leq f < 2$ GHz		40		mVp-p
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data (Note 1)	1.0		4.25	Gbps
CID		Consecutive identical digits (bits) (Note 1)			10	Bits
CONTROL INPUTS: TX_DISABLE, PE0, PE1, OUTLEV, LOSLEV						
Voltage, Logic High	V_{IH}		2.0			V
Voltage, Logic Low	V_{IL}				0.8	V
Current, Logic High	I_{IH}	$V_{IH} = V_{CC} + 0.5V$			-150	μA
Current, Logic Low	I_{IL}	$V_{IL} = 0.8V$			350	μA
STATUS OUTPUT: LOS						
LOS Open Collector Current Sink		LOS asserted	0		25	μA
		LOS unasserted, $V_{OL} \leq 0.4V$ with 4.7k Ω pullup resistor, pullup supply = 5.5V	1.0			mA
		$V_{CC} = 0V$, pullup supply = 5.5V, external pullup resistor $\geq 4.7k\Omega$	0		25	μA
LOS Assert Level		LOSLEV = high (Note 1)	100			mVp-p
		LOSLEV = low (Note 1)	50			mVp-p
LOS Deassert Level		LOSLEV = high (Note 1)			300	mVp-p
		LOSLEV = low (Note 1)			120	mVp-p
LOS Hysteresis		LOSLEV = high (Note 1)	20			mVp-p
		LOSLEV = low (Note 1)		4		mVp-p
LOS Response Time		Time from IN dropping below assert level, or rising above deassert level to 50% point of LOS			10	μs
LOS Transition Time		Rise-time or fall-time (10% to 90%), external pullup resistor = 4.7k Ω		250		ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C and V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
EQUALIZER AND CABLE DRIVER SPECIFICATIONS								
Input Swing		Measured differentially at point A of Figure 2 (Note 1)		600		2000	mV _{P-P}	
Input Resistance		Measured differentially		85	100	115	Ω	
Input Return Loss		100MHz to 2GHz (Note 1)		10			dB	
Differential Output Swing		Measured differentially at point B of Figure 2 (Notes 1, 2)	TX_DISABLE = low, OUTLEV = high	1450		1800	mV _{P-P}	
			TX_DISABLE = low, OUTLEV = low	1000		1350		
			TX_DISABLE = high	40				
Common-Mode Output		(OUT+) + (OUT-), measured at point B of Figure 2; TX_DISABLE = low, OUTLEV = high (Notes 1, 2)				60	mV _{P-P}	
Output Resistance		OUT+ or OUT- to V _{CC} , single ended		42	50	58	Ω	
Output Return Loss		100MHz to 2GHz (Note 1)		10			dB	
Output Transition Time	t _r , t _f	20% to 80% (Notes 1, 3)			50	80	ps	
Random Jitter		(Notes 1, 3)				1.6	ps _{RMS}	
Output Preemphasis		See Figure 1	PE1	PE0				dB
			0	0	2			
			0	1	4			
			1	0	8			
			1	1	14			
Residual Output Deterministic Jitter at 1.0625Gbps to 2.125Gbps (Notes 1, 4, 5)		Source to IN 6 mil FR4 ≤ 10in	OUT to Load	PE1	PE0	0.10	0.15	UI _{P-P}
			1m, 24AWG	0	0			
			5m, 24AWG	0	1			
			10m, 24AWG	1	0			
			15m, 24AWG	1	1			
Residual Output Deterministic Jitter at 4.25Gbps (Notes 1, 4, 5)		Source to IN 6 mil FR4 ≤ 10in	OUT to Load	PE1	PE0	0.15	0.20	UI _{P-P}
			1m, 24AWG	0	0			
			5m, 24AWG	0	1			
			10m, 24AWG	1	0			
			15m, 24AWG	1	1			

Note 1: Guaranteed by design and characterization.

Note 2: PE1 = PE0 = 1 for maximum preemphasis, load is 50Ω ±1% at each side, and the pattern is 0000011111 at 1Gbps.

Note 3: Measured at point B in Figure 2 using 0000011111 at 1Gbps. PE1 = PE0 = 0 for minimum preemphasis. For transition time, the 0% reference level is the steady-state level after four zeros, just before the transition. The 100% reference level is the maximum voltage of the transition.

Note 4: Tested with CJTPAT, as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5 character).

Note 5: Cables are unequalized, Amphenol Spectra-Strip 24AWG. Residual deterministic jitter is the difference between the source jitter at point A, and load jitter at point D in Figure 2. The deterministic jitter at the output of the transmission line must be from media-induced loss and not from clock-source modulation.

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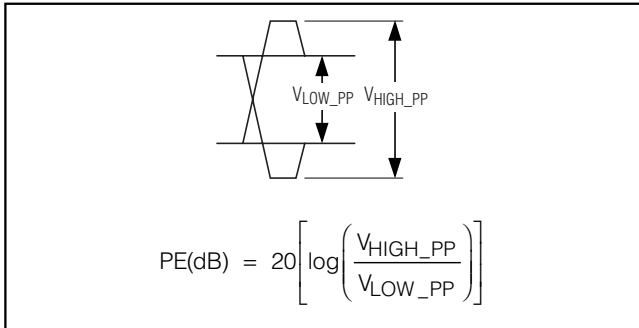


Figure 1. Illustration of Tx Preemphasis in dB

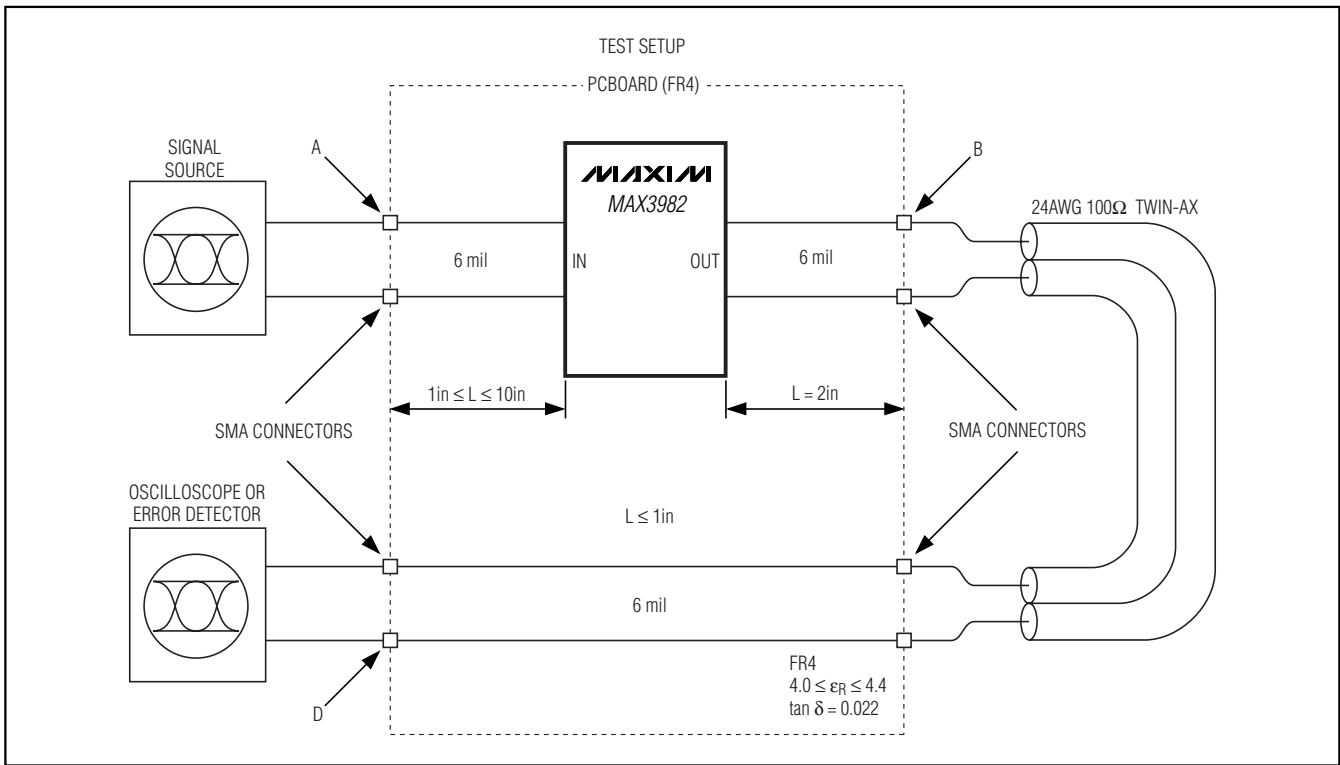


Figure 2. Test Setup. The points labeled A, B, and D are referenced for AC parameter test conditions. Deterministic jitter and eye diagrams measured at point D.

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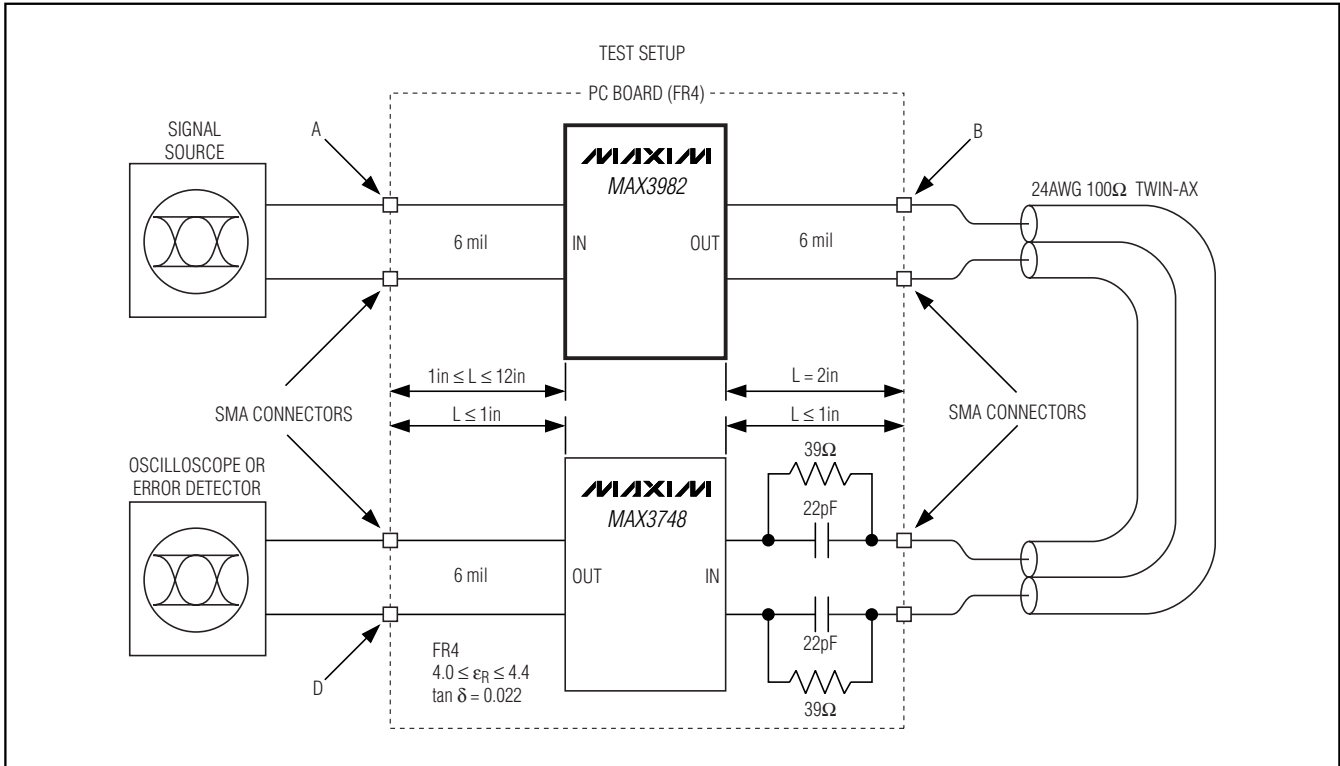
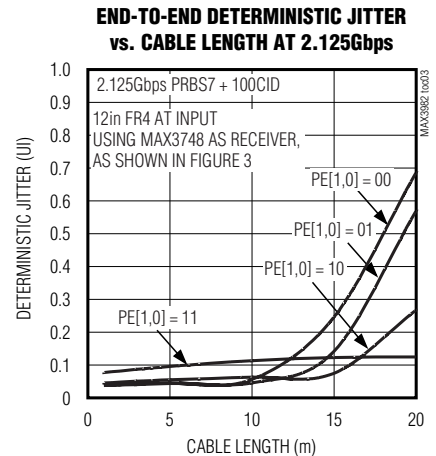
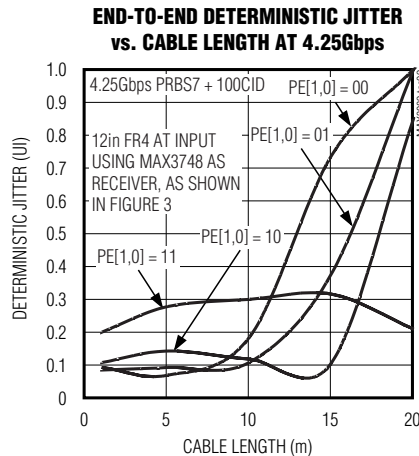
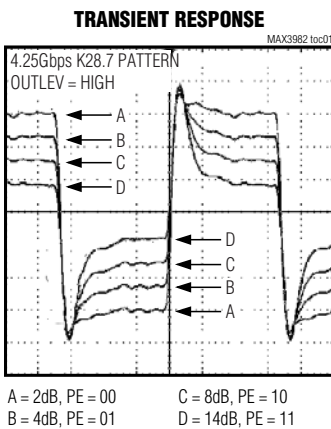


Figure 3. End-to-End Test Setup Using the MAX3748 as a Receiver. Deterministic jitter and eye diagrams measured at point D.

Typical Operating Characteristics

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 27, 100 zeros, 1010, PRBS 27, 100 ones, 0101.)

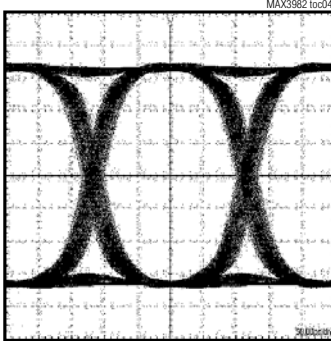


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Typical Operating Characteristics (continued)

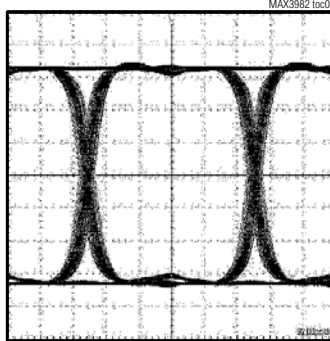
(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2⁷, 100 zeros, 1010, PRBS 2⁷, 100 ones, 0101.)

**END-TO-END EYE DIAGRAM,
20m 24AWG CABLE AT 4.25Gbps**



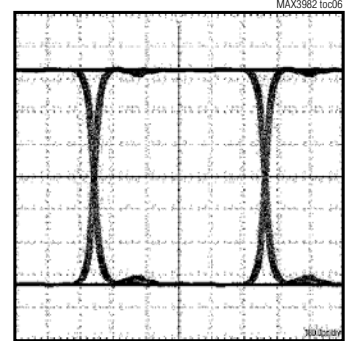
4.25Gbps PRBS7 + 100CID PATTERN,
0in FR4 AT INPUT, USING MAX3748
AS RECEIVER, AS SHOWN IN FIGURE 3

**END-TO-END EYE DIAGRAM,
20m 24AWG CABLE AT 2.125Gbps**



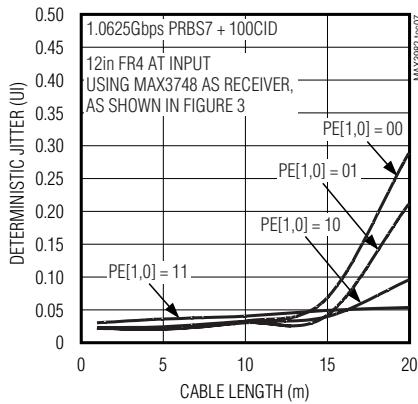
2.125Gbps PRBS7 + 100CID PATTERN,
0in FR4 AT INPUT, USING MAX3748
AS RECEIVER, AS SHOWN IN FIGURE 3

**END-TO-END EYE DIAGRAM,
20m 24AWG CABLE AT 1.0625Gbps**

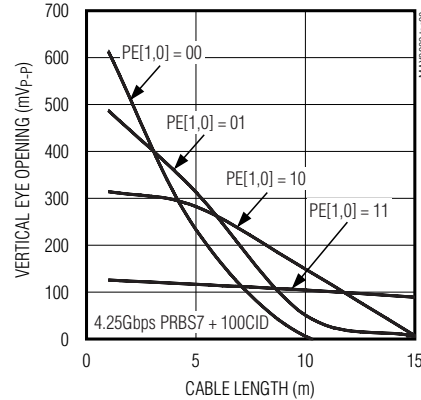


1.0625Gbps PRBS7 + 100CID PATTERN,
0in FR4 AT INPUT, USING MAX3748
AS RECEIVER, AS SHOWN IN FIGURE 3

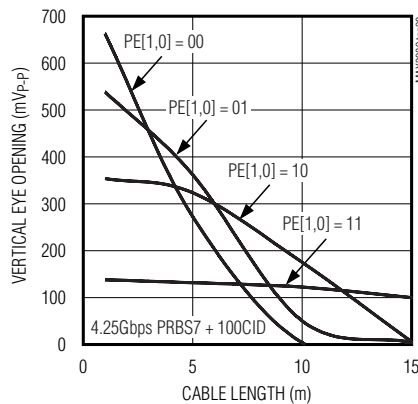
**END-TO-END DETERMINISTIC JITTER
vs. CABLE LENGTH AT 1.0625Gbps**



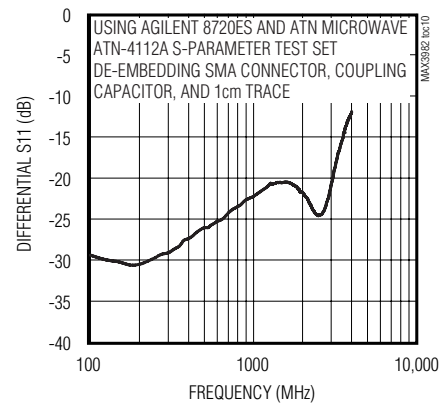
**VERTICAL EYE OPENING
vs. CABLE LENGTH WITH OUTLEV = LOW**



**VERTICAL EYE OPENING
vs. CABLE LENGTH WITH OUTLEV = LOW**



INPUT RETURN LOSS vs. FREQUENCY



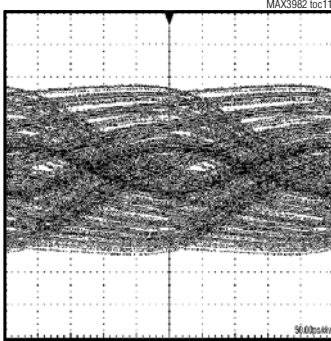
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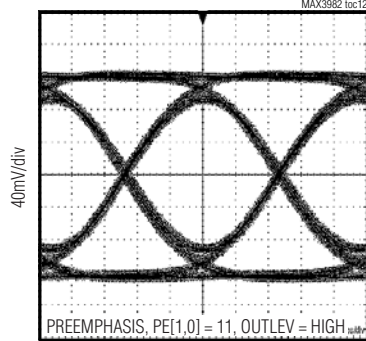
Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7 , 100 zeros, 1010, PRBS 2^7 , 100 ones, 0101.)

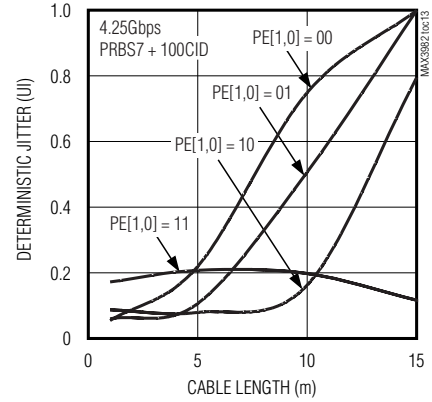
**15m 24AWG CABLE ASSEMBLY
OUTPUT WITHOUT MAX3982,
4.25Gbps CJTPAT**



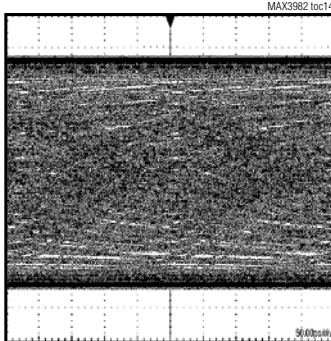
**15m 24AWG CABLE ASSEMBLY
OUTPUT WITH MAX3982
PREEMPHASIS, 4.25Gbps CJTPAT**



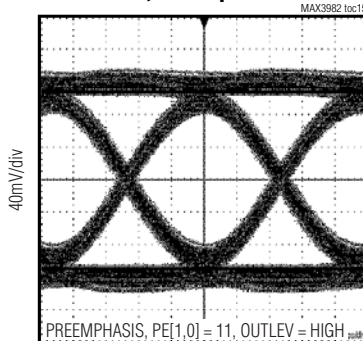
**DETERMINISTIC JITTER
vs. CABLE LENGTH**



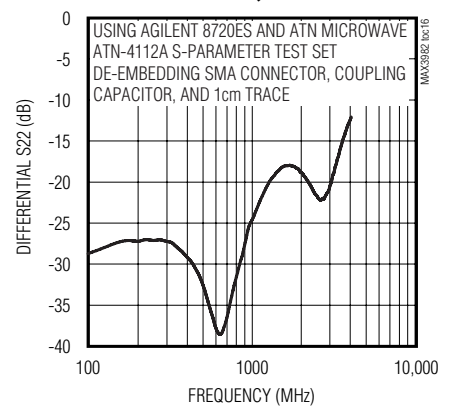
**15m 24AWG CABLE ASSEMBLY
OUTPUT WITHOUT MAX3982,
4.25Gbps PRBS7 + 100CID**



**15m 24AWG CABLE ASSEMBLY
OUTPUT WITH MAX3982
PREEMPHASIS, 4.25Gbps PRBS7 + 100CID**



**OUTPUT RETURN LOSS
vs. FREQUENCY**

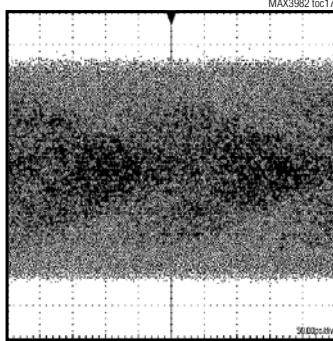


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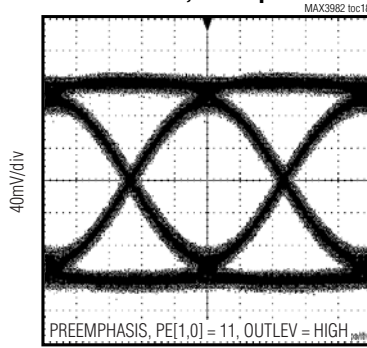
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2⁷, 100 zeros, 1010, PRBS 2⁷, 100 ones, 0101.)

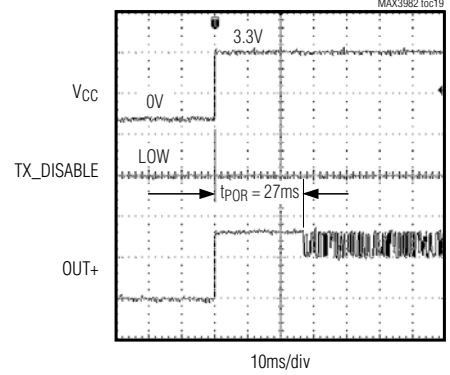
**15m 24AWG CABLE ASSEMBLY
OUTPUT WITHOUT MAX3982,
4.25Gbps PRBS31**



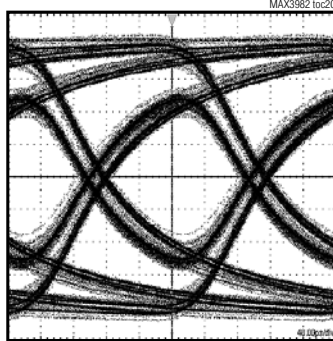
**15m 24AWG CABLE ASSEMBLY
OUTPUT WITH MAX3982
PREEMPHASIS, 4.25Gbps PRBS31**



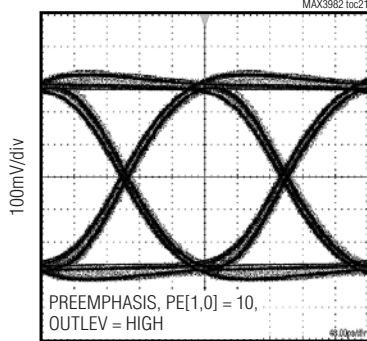
HOT-PLUG WITH TX_DISABLE LOW



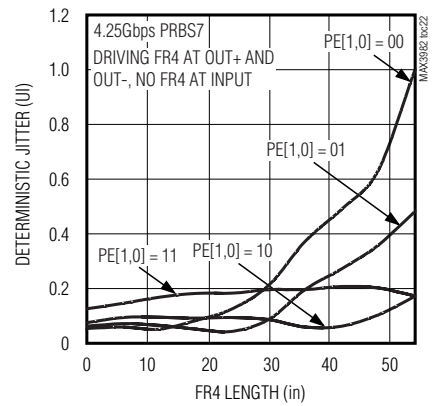
**30in FR4 OUTPUT
WITHOUT MAX3982,
4.25Gbps CJTPAT**



**30in FR4 OUTPUT
WITH MAX3982 PREEMPHASIS,
4.25Gbps CJTPAT**



**DETERMINISTIC JITTER
vs. FR4 LENGTH**



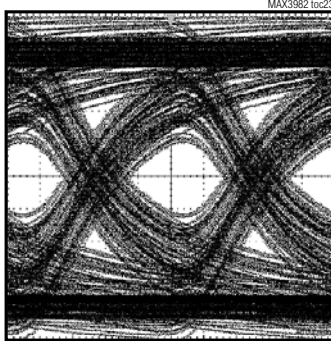
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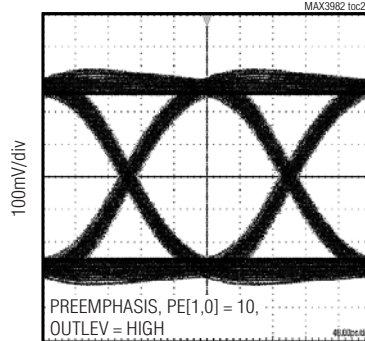
Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7 , 100 zeros, 1010, PRBS 2^7 , 100 ones, 0101.)

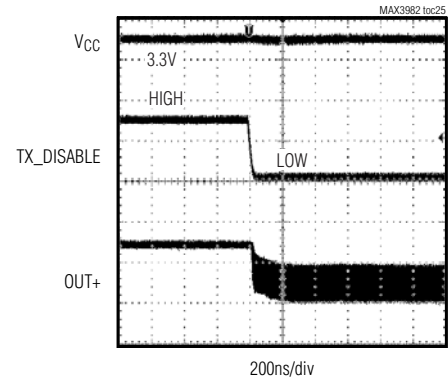
**30in FR4 OUTPUT
WITHOUT MAX3982
4.25Gbps PRBS7 + 100CID**



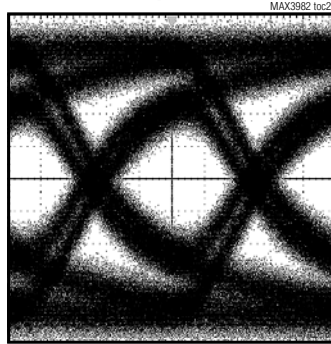
**30in FR4 OUTPUT
WITH MAX3982 PREAMPHASIS,
4.25Gbps PRBS7 + 100CID**



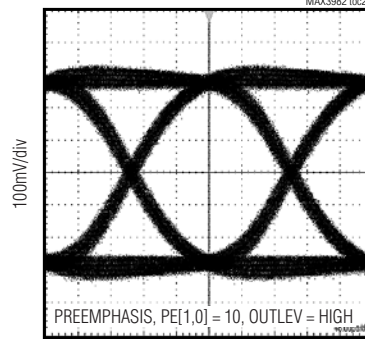
TRANSMITTER ENABLE



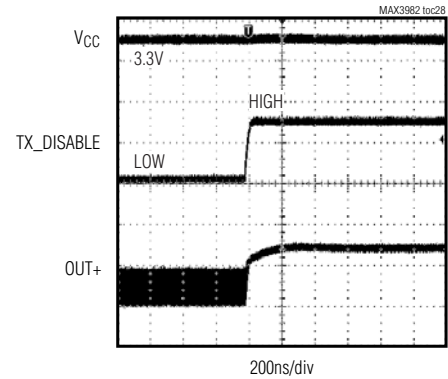
**30in FR4 OUTPUT
WITHOUT MAX3982,
4.25Gbps PRBS31**



**30in FR4 OUTPUT
WITH MAX3982 PREAMPHASIS,
4.25Gbps PRBS31**



TRANSMITTER DISABLE

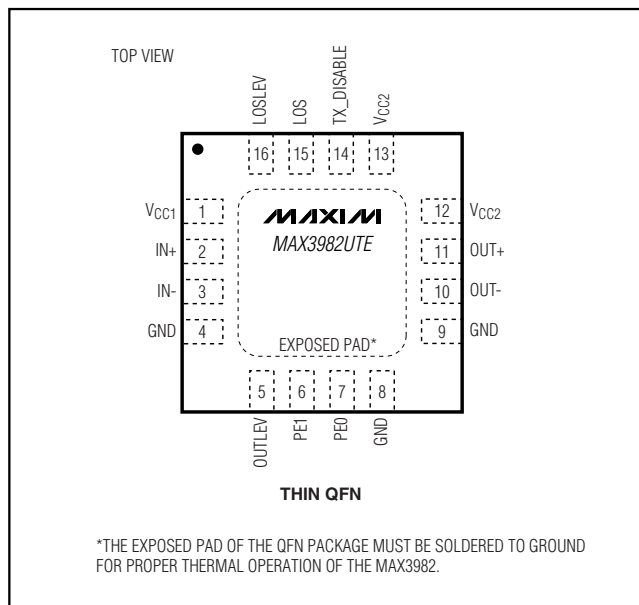


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Pin Description

PIN	NAME	FUNCTION
1	V _{CC1}	Power-Supply Connection for Input. Connect to +3.3V.
2	IN+	Positive Data Input, CML. This input is internally terminated with 50Ω to V _{CC1} .
3	IN-	Negative Data Input, CML. This input is internally terminated with 50Ω to V _{CC1} .
4, 8, 9	GND	Circuit Ground
5	OUTLEV	Output-Swing Control Input, LVTTTL with 40kΩ Internal Pullup. Set to TTL high or open for maximum output swing, or set to TTL low for reduced swing.
6	PE1	Output Preemphasis Control Input, LVTTTL with 10kΩ Internal Pullup. This pin is the most significant bit of the 2-bit preemphasis control. Set high or open to assert this bit.
7	PE0	Output Preemphasis Control Input, LVTTTL with 10kΩ Internal Pullup. This pin is the least significant bit of the 2-bit preemphasis control. Set high or open to assert this bit.
10	OUT-	Negative Data Output, CML. This output is terminated with 50Ω to V _{CC2} .
11	OUT+	Positive Data Output, CML. This output is terminated with 50Ω to V _{CC2} .
12, 13	V _{CC2}	Power-Supply Connection for Output. Connect to +3.3V.
14	TX_DISABLE	Transmitter Disable Input, LVTTTL with 10kΩ Internal Pullup. When high or open, differential output is 40mV _{p-p} . Set low for normal operation.
15	LOS	Loss-of-Signal Detect, TTL Output. This output is open-collector TTL, and therefore requires an external 4.7kΩ to 10kΩ pullup resistor (5.5V maximum). This output sinks current when the input signal level is valid.
16	LOSLEV	LOS Sensitivity Control Input, LVTTTL with 40kΩ Internal Pullup. Set to TTL high or open for less sensitivity (higher assert threshold). Set to TTL low for more sensitivity (lower assert threshold).
EP	EXPOSED PAD	Exposed Pad. For optimal thermal conductivity, this pad must be soldered to the circuit board ground.

Pin Configuration



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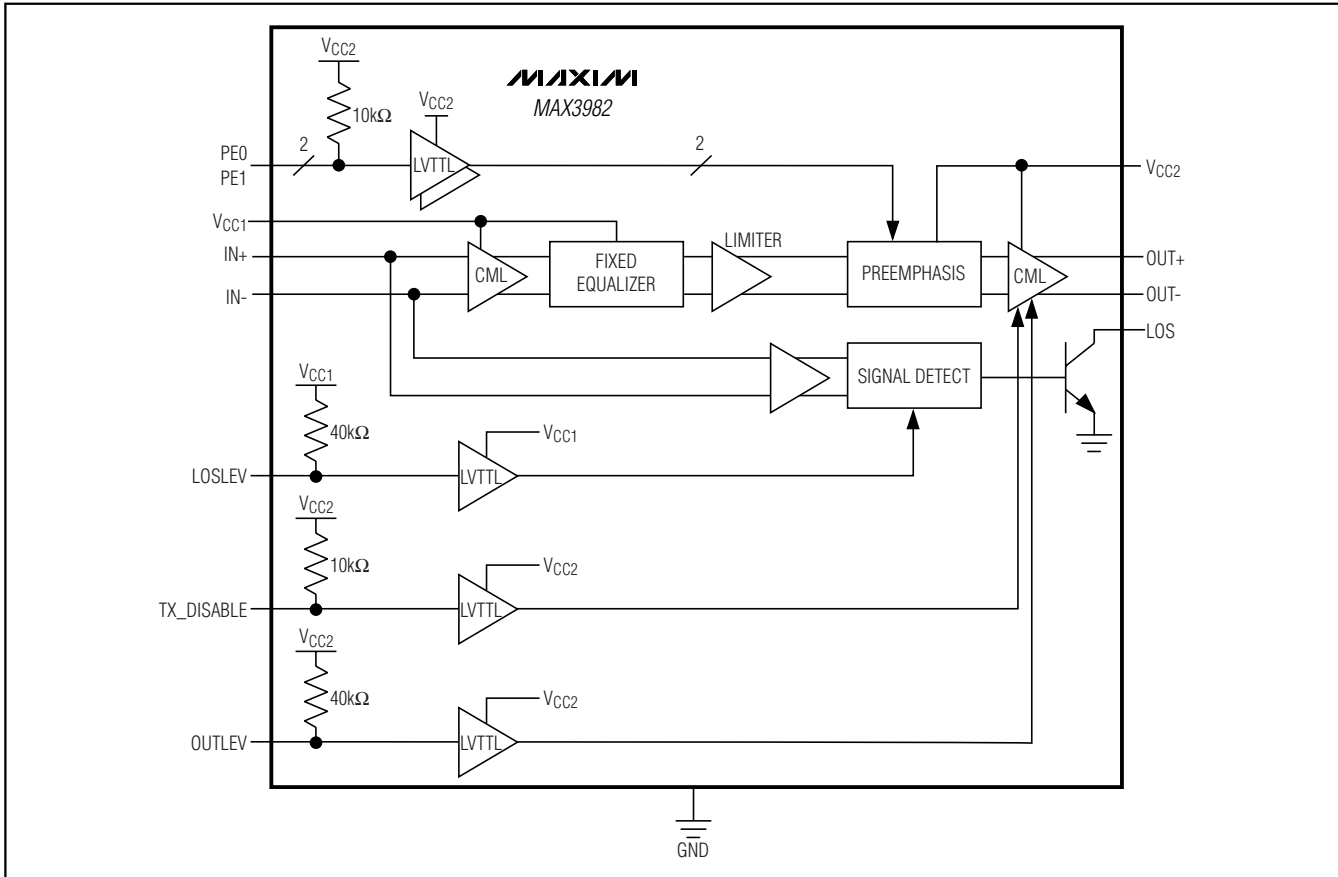


Figure 4. Functional Diagram

Detailed Description

The MAX3982 comprises a PC board receiver, a cable driver, and a loss-of-signal detector with adjustable threshold (Figure 4). Equalization is provided in the receiver. Selectable preemphasis and selectable output amplitude are included in the transmitter. The MAX3982 also includes transmit disable control for the output.

PC Board Receiver and Cable Driver

Data is fed into the MAX3982 through a CML input stage and fixed equalization stage. The fixed equalizer in the receiver corrects for up to 10in of PC board loss on FR4 material at 4.25Gbps.

The cable driver includes four-state preemphasis to compensate for up to 15m of 24AWG, 100Ω balanced cable. Table 1 is provided for easy translation between preemphasis expressions. The OUTLEV pin selects the output amplitude. When OUTLEV is low, the amplitude is 1200mV_{P-P}. When OUTLEV is high, the amplitude is

1600mV_{P-P}. Residual jitter of the MAX3982 is independent of up to 0.20UI_{P-P} source jitter.

Loss-of-Signal (LOS) Output

Loss-of-signal detection is provided on the data input. Pullup resistors should be connected from LOS to a supply in the range of +3.0V to +5.5V. The LOS output is not valid until power-up is complete. Typical LOS response time is 100ns.

The LOS assert and deassert levels are set by the LOSLEV pin. When LOSLEV is LVTTTL high or open, the LOS assert threshold is 180mV_{P-P}. When LOSLEV is LVTTTL low, the LOS assert threshold is 85mV_{P-P}.

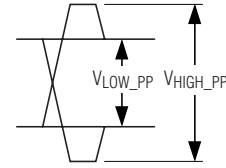
TX Disable

Transmit disable is provided to turn off the output when desired. The TX_DISABLE pin can be connected to LOS to automatically squelch the output when the incoming signal is below the threshold set by LOSLEV (see the *Autodetect* section).

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Table 1. Preemphasis Translation

Ratio	α	10Gbase-CX4	IN dB
$\frac{V_{HIGH_PP}}{V_{LOW_PP}}$	$\frac{V_{HIGH_PP} - V_{LOW_PP}}{V_{HIGH_PP} + V_{LOW_PP}}$	$1 - \frac{V_{LOW_PP}}{V_{HIGH_PP}}$	$20 \left[\log \left(\frac{V_{HIGH_PP}}{V_{LOW_PP}} \right) \right]$
1.26	0.11	0.21	2
1.58	0.23	0.37	4
2.51	0.43	0.6	8
5.01	0.67	0.8	14



Applications Information

Autodetect

The MAX3982 can automatically detect an incoming signal and enable the data outputs. Autodetect can be accomplished by connecting the LOS pin to TX_DISABLE. TX_DISABLE has a 10k Ω internal pullup resistor. If a loss-of-signal is detected, the TX_DISABLE pin is forced high and disables the outputs. Leaving the inputs to the MAX3982 open (i.e., floating) is not recommended as noise amplification may occur and create undesirable output signals. Autodetect is recommended to eliminate noise amplification or possible oscillation. For periods much greater than 100ns without data transitions, autodetect disables the output.

Layout Considerations

Circuit board layout and design can significantly affect the performance of the MAX3982. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on the data signals. Power-supply decoupling should also be placed as close to the VCC pins as possible. This should be sufficient supply filtering. Always connect all VCC pins to a power plane. Take care to isolate the input from the output signals to reduce feedthrough.

Exposed Pad Package

The exposed-pad, 16-pin QFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX3982 must be soldered to the circuit board for proper thermal performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Interface Schematics

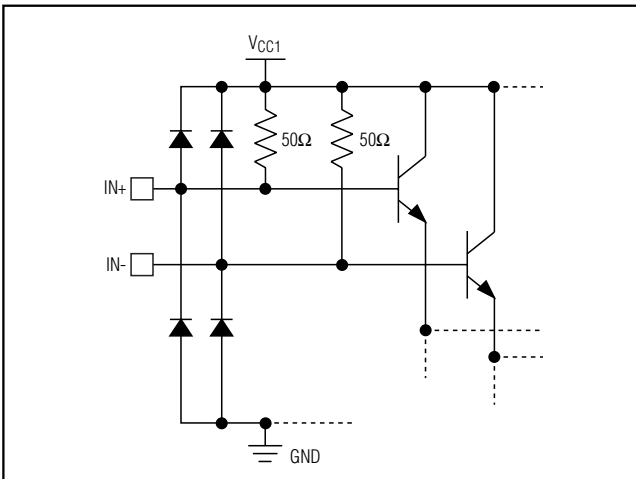


Figure 5. IN+/IN- Equivalent Input Structure

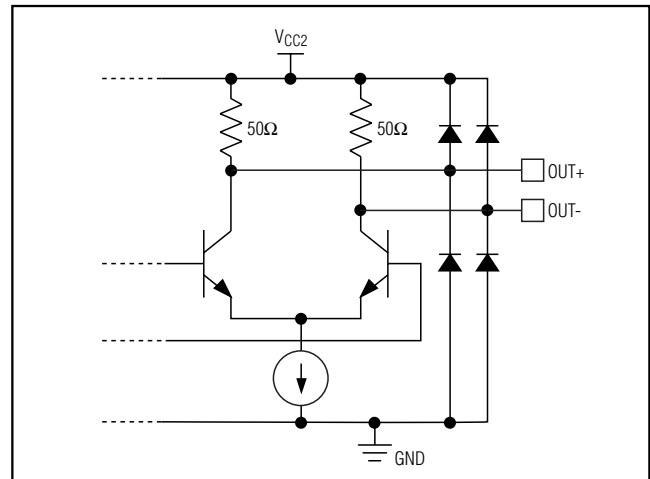


Figure 6. OUT+/OUT- Equivalent Output Structure

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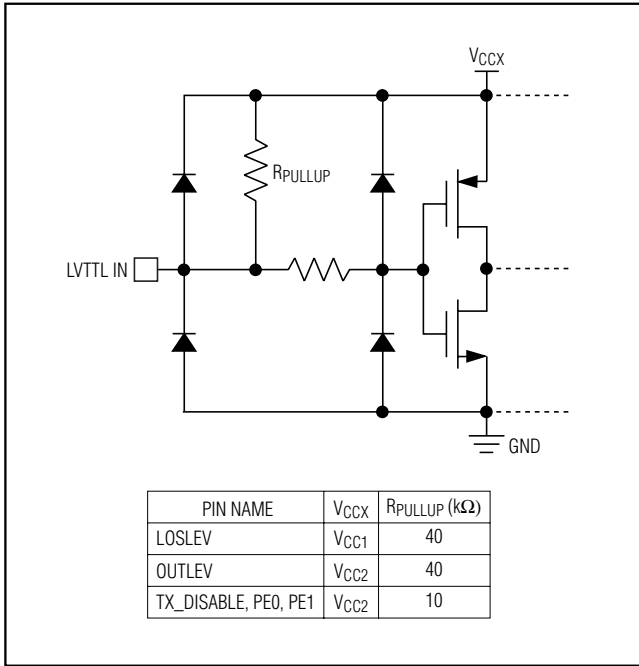


Figure 7. LVTTTL Equivalent Input Structure

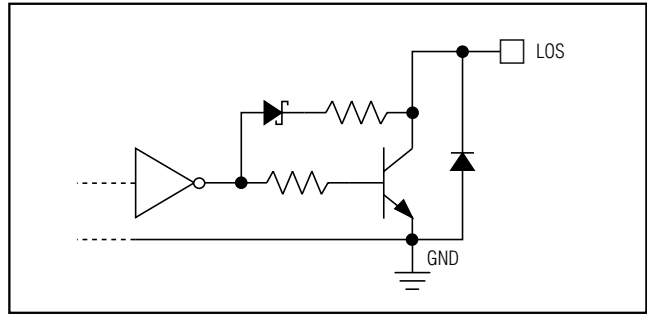


Figure 8. Loss-of-Signal Equivalent Output Structure

Chip Information

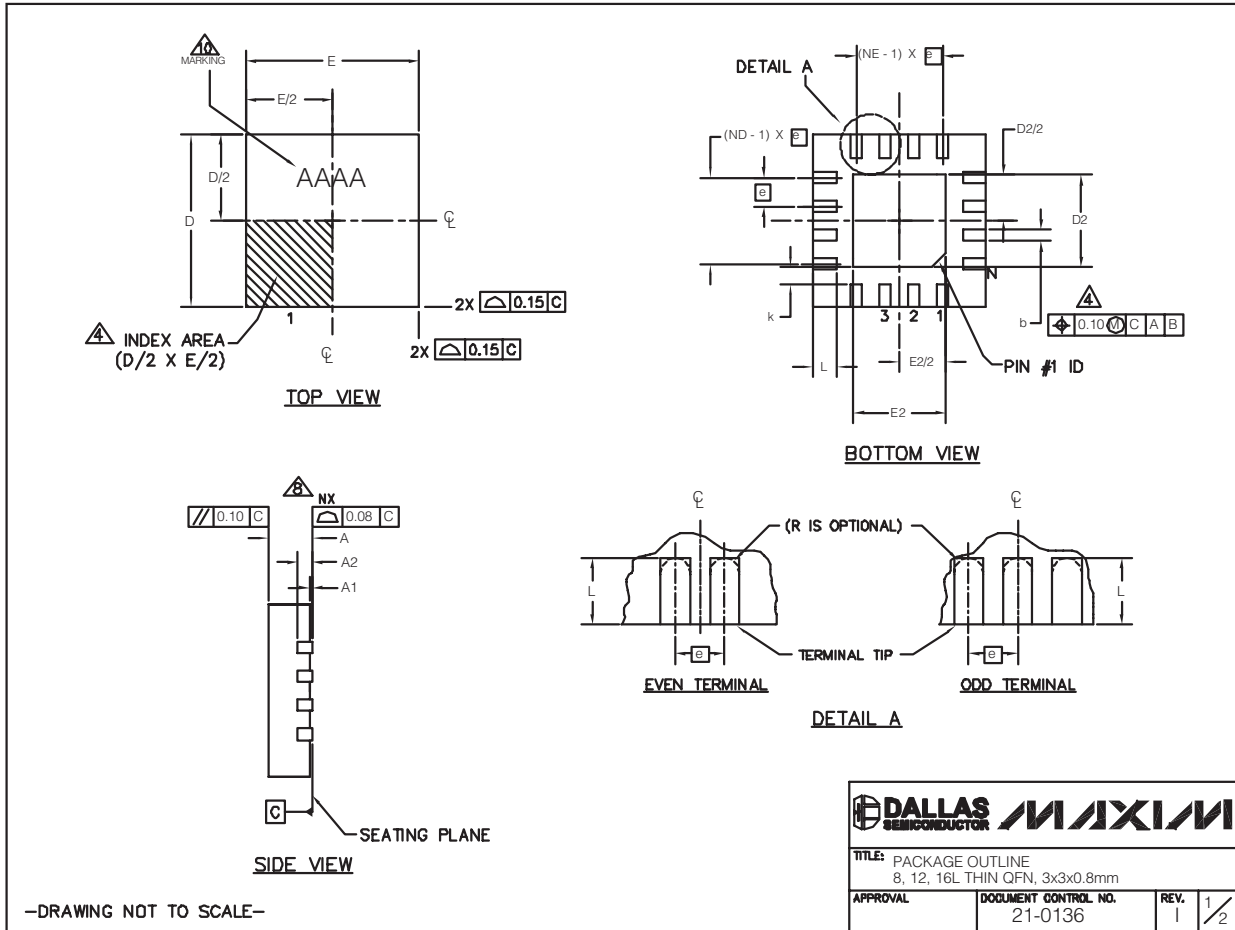
TRANSISTOR COUNT: 2957

PROCESS: SiGe Bipolar

SFP Copper-Cable Preemphasis Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. 1 1/2

SFP Copper-Cable Preemphasis Driver

MAX3982

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

PKG CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- WARPAGE NOT TO EXCEED 0.10mm.

—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. 1 2/2

Revision History

Rev 2; 2/06: Added lead-free package to Ordering Information table (page 1); updated package outline (pages 14, 15).

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