Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUTA, OUTB to GND.....-0.3V to (V_{DD} + 0.3V)
REFIN, $\overline{CS}$/AO, DOUT/AI, SPI/$\overline{I2C}$, FSADJA,
FSADJB to GND.....-0.3V to (V_{DD} + 0.3V)
SCLK/SCL, DIN/SDA.....-0.3V to +6V
Continuous Power Dissipation (T_A = +85°C)
16-Pin Thin QFN (derate 17.5mW/°C above +70°C)..1398.6mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, GND = 0, V_{REFIN} = +1.25V, internal reference, $R_{FSADJ\_}$ = 20kΩ; compliance voltage = (V_{DD} - 0.6V), $V_{SCLK/SCL}$ = 0, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION							
Resolution				10			Bits
Integral Nonlinearity	INL	$I_{OUT\_}$ = 1mA to 30mA (Note 2)			±2		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset	I_{OS}			-50	-16		LSB
Zero-Scale Error		$I_{OUT\_}$ = 1mA to 30mA, code = 0x000				1	µA
Full-Scale Error		$I_{OUT\_}$ = 1mA to 30mA, code = 0x3FF, includes offset			-16		LSB
REFERENCE							
Internal Reference Range				1.21	1.25	1.29	V
Internal Reference Tempco					30		ppm/°C
External Reference Range				0.5		1.5	V
External Reference Input Current					108	225	µA
DAC OUTPUTS							
Full-Scale Current		(Note 3)		1		30	mA
Output Current Leakage in Shutdown						±1	µA
Output Capacitance					10		pF
Current Source Dropout Voltage (V_{DD} - $V_{OUT\_}$)		$I_{OUT\_}$ = 30mA		1			V
		$I_{OUT\_}$ = 20mA	T_A = +25°C	0.55			
			T_A = -40°C to +85°C	0.6			
Output Impedance at Full-Scale Current					100		kΩ
Capacitive Load to Ground	C_{LOAD}				10		nF
Series Inductive Load	L_{LOAD}				100		nH
Maximum FSADJ_ Capacitive Load	$C_{FSADJ\_}$				75		pF
DYNAMIC PERFORMANCE							
Settling Time	tS	C_{LOAD} = 24pF, L_{LOAD} = 27nH (Note 4)			30		µs
Digital Feedthrough					2		nVs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, GND = 0, V_{REFIN} = +1.25V, internal reference, $R_{FSADJ\_}$ = 20kΩ; compliance voltage = (V_{DD} - 0.6V), $V_{SCLK/SCL}$ = 0, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-to-Analog Glitch Impulse				40		nVs
DAC-to-DAC Current Matching				2		%
Wake-Up Time		V_{DD} = +3V		400		µs
		V_{DD} = +5V		10		
POWER SUPPLIES						
Supply Voltage	V_{DD}		+2.70		+5.25	V
Supply Current	I_{DD}	V_{DD} = +5.25V, no load		3	6	mA
Shutdown Current					1.2	µA
LOGIC AND CONTROL INPUTS						
Input High Voltage (Note 5)	V_{IH}	+2.7V ≤ V_{DD} ≤ +3.4V	0.7 x V_{DD}			V
		+3.4V < V_{DD} ≤ +5.25V	2.4			
Input Low Voltage	V_{IL}	(Note 5)			0.8	V
Input Hysteresis	V_{HYS}			0.1 x V_{DD}		V
Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}				±1	µA
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.6	V
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
I²C TIMING CHARACTERISTICS (Figure 2)						
SCL Clock Frequency	f_{SCL}				400	kHz
Setup Time for START Condition	$t_{SU:STA}$		600			ns
Hold Time for START Condition	$t_{HD:STA}$		600			ns
SCL Pulse-Width Low	t_{LOW}		130			ns
SCL Pulse-Width High	t_{HIGH}		600			ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0		70	ns
SCL Rise Time	t_{RCL}		20 + 0.1 x C_B		300	ns
SCL Fall Time	t_{FCL}		20 + 0.1 x C_B		300	ns
SDA Rise Time	t_{RDA}		20 + 0.1 x C_B		300	ns
SDA Fall Time	t_{FDA}		20 + 0.1 x C_B		300	ns

Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, GND = 0, V_{REFIN} = +1.25V, internal reference, $R_{FSADJ\_}$ = 20kΩ; compliance voltage = (V_{DD} - 0.6V), $V_{SCLK/SCL}$ = 0, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.0V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Setup Time for STOP Condition	$t_{SU:STO}$		160			ns
Maximum Capacitive Load for Each Bus Line	C_B			400		pF
SPI TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		25			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		50			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Transition	t_{DO1}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{CSE}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Rise to DOUT Disable	t_{CSD}	C_{LOAD} = 30pF			40	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		50			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns
SPI TIMING CHARACTERISTICS FOR DAISY CHAINING (Figure 6)						
SCLK Clock Period	t_{CP}		200			ns
SCLK Pulse-Width High	t_{CH}		80			ns
SCLK Pulse-Width Low	t_{CL}		80			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		25			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		50			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Transition	t_{DO1}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{CSE}	C_{LOAD} = 30pF			40	ns
$\overline{CS}$ Rise to DOUT Disable	t_{CSD}	C_{LOAD} = 30pF			40	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		50			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns

Note 1: 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: INL linearity is guaranteed from code 60 to code 1024.

Note 3: Connect a resistor from FSADJ_ to GND to adjust the full-scale current. See the *Reference Architecture and Operation* section.

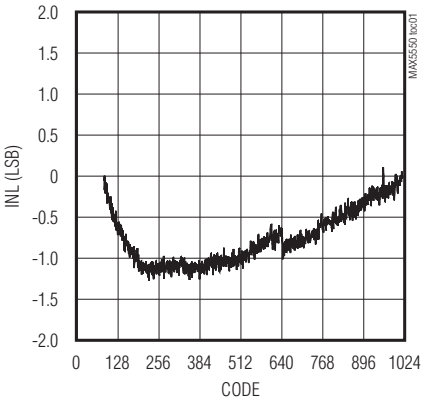
Note 4: Settling time is measured from (0.25 x full scale) to (0.75 x full scale).

Note 5: The device draws higher supply current when the digital inputs are driven with voltages between (V_{DD} - 0.5V) and (GND + 0.5V). See the Supply Current vs. Digital Input Voltage graph in the *Typical Operating Characteristics*.

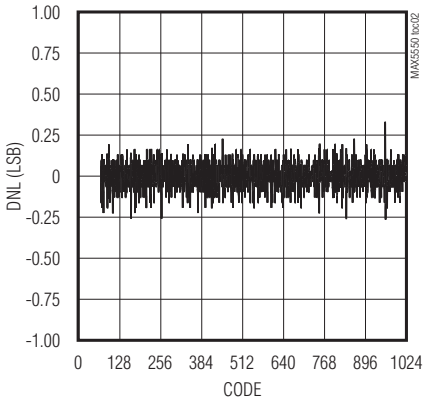
Typical Operating Characteristics

(V_{DD} = +3.0V, GND = 0, V_{REFIN} = +1.25V, internal reference, $R_{FSADJ\_}$ = 20kΩ, T_A = +25°C. unless otherwise noted).

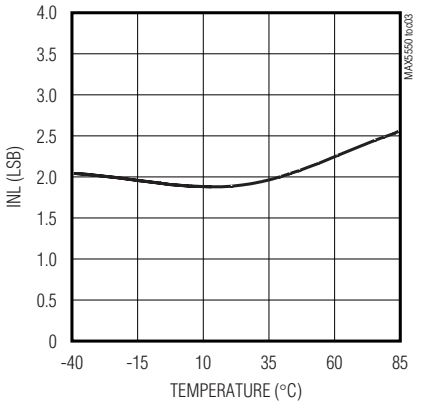
INL vs. CODE



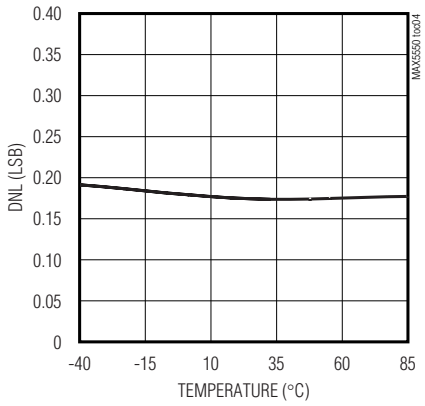
DNL vs. CODE



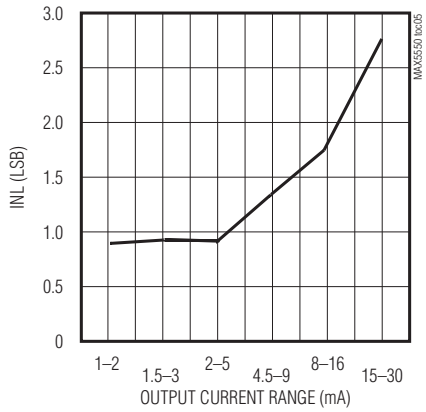
INL vs. TEMPERATURE



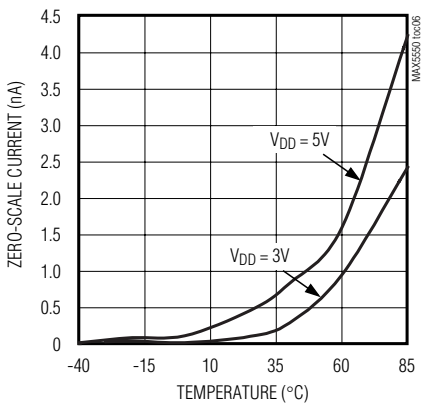
DNL vs. TEMPERATURE



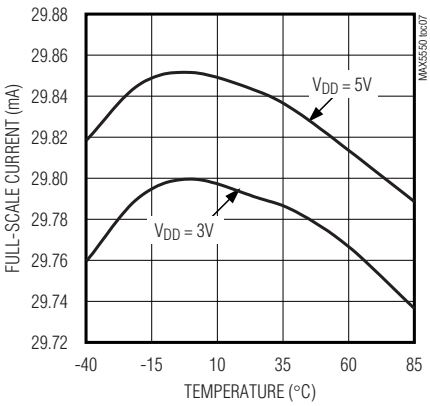
MAXIMUM INL ERROR vs. OUTPUT CURRENT RANGES



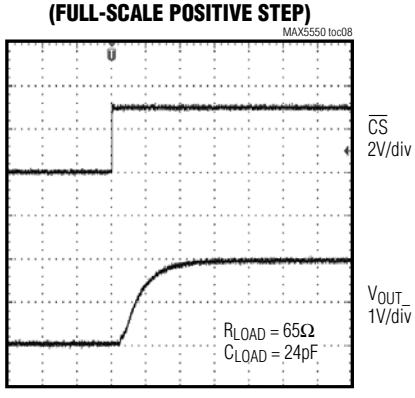
ZERO-SCALE OUTPUT CURRENT vs. TEMPERATURE



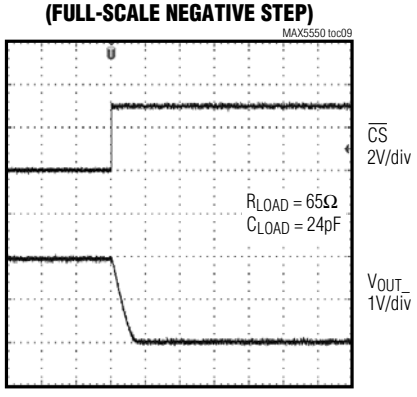
FULL-SCALE CURRENT vs. TEMPERATURE



SETTLING TIME (FULL-SCALE POSITIVE STEP)



SETTLING TIME (FULL-SCALE NEGATIVE STEP)

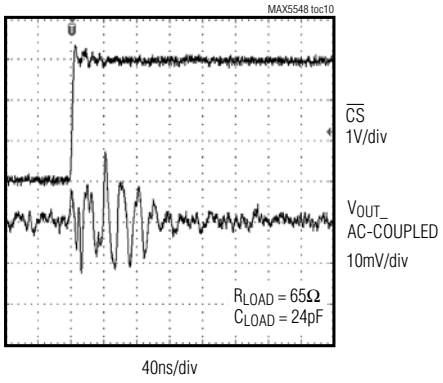


Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

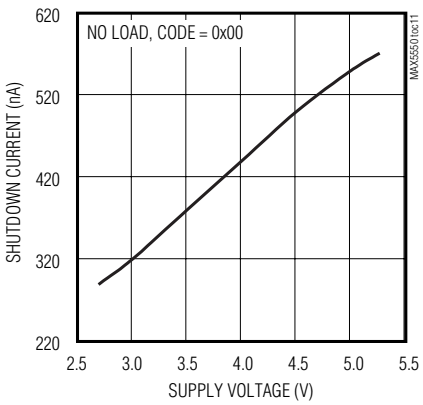
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V, GND = 0, V_{REFIN} = +1.25V, internal reference, $R_{FSADJ\_}$ = 20kΩ, T_A = +25°C. unless otherwise noted).

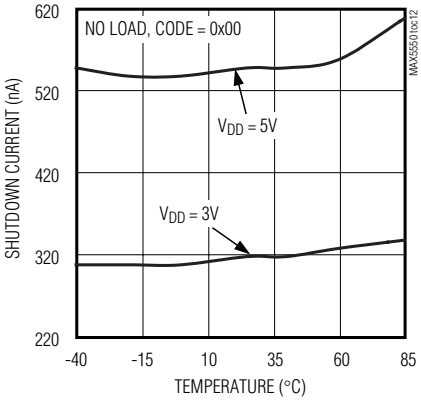
GLITCH IMPULSE



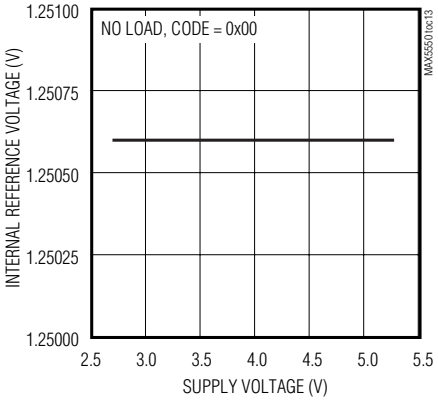
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



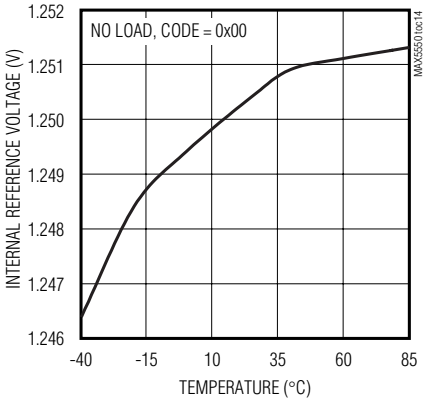
SHUTDOWN CURRENT vs. TEMPERATURE



INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



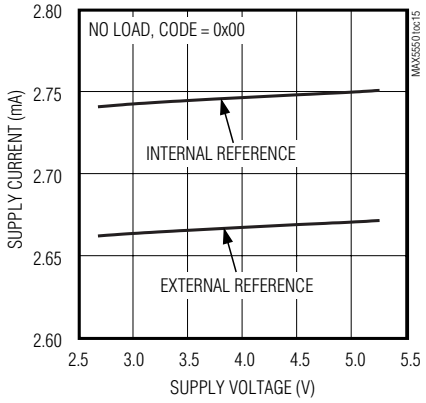
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



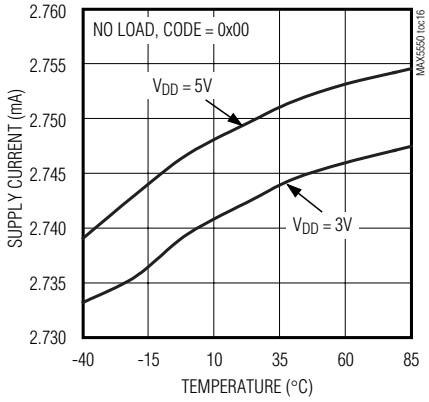
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V, GND = 0, V_{REFIN} = +1.25V, internal reference, $R_{FSADJ\_}$ = 20kΩ, T_A = +25°C. unless otherwise noted).

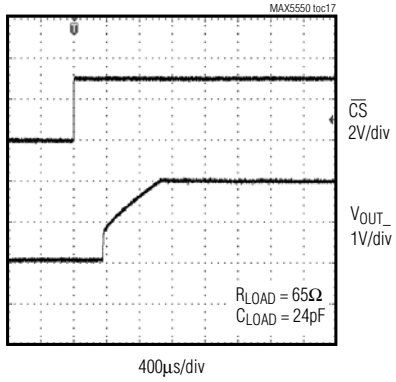
SUPPLY CURRENT vs. SUPPLY VOLTAGE



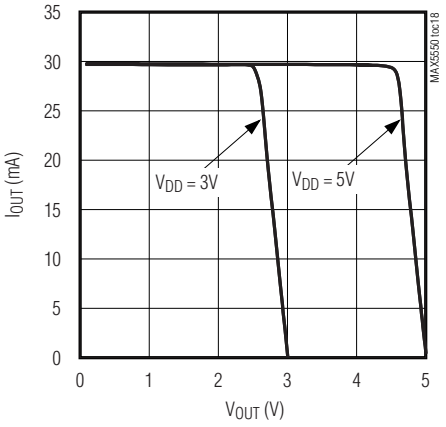
SUPPLY CURRENT vs. TEMPERATURE



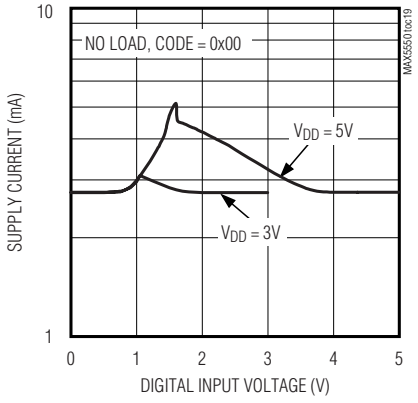
WAKE-UP TIME



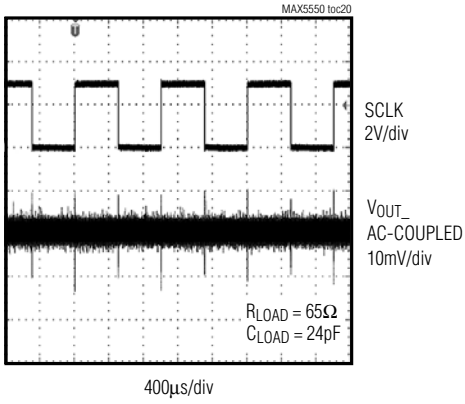
IOUT vs. VOUT



SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



DIGITAL FEEDTHROUGH



Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

Pin Description

PIN	NAME	FUNCTION
1	SCLK/SC	Serial Clock Input. Connect SCL to V_{DD} through a 2.4kΩ resistor in I²C mode.
2	DIN/SDA	Serial Data Input. Connect SDA to V_{DD} through a 2.4kΩ resistor in I²C mode.
3	$\overline{CS}$/A0	Chip-Select Input in SPI Mode/Address Select 0 in I²C Mode. $\overline{CS}$ is an active-low input. Connect A0 to V_{DD} or GND to set the device address in I²C mode.
4	SPI/$\overline{I2C}$	SPI/$\overline{I2C}$ Select Input. Connect SPI/$\overline{I2C}$ to V_{DD} to select SPI mode, or connect SPI/$\overline{I2C}$ to GND to select I²C mode.
5	DOUT/A1	Serial Data Output in SPI Mode/Address Select 1 in I²C Mode. Use DOUT to daisy chain the MAX5550 to other devices or to read back in SPI mode. The digital data is clocked out on SCLK's falling edge. Connect A1 to V_{DD} or GND to set the device address in I²C mode.
6, 13, 15	N.C.	No Connection. Leave unconnected or connect to GND.
7	REFIN	Reference Input. Drive REFIN with an external reference source between +0.5V and +1.5V. Leave REFIN unconnected in internal reference mode. Bypass with a 0.1µF capacitor to GND as close to the device as possible.
8, 16	GND	Ground
9	OUTB	DACB Output. OUTB provides up to 30mA of output current.
10	FSADJB	DACB Full-Scale Adjust Input. For maximum full-scale output current, connect a 20kΩ resistor between FSADJB and GND. For minimum full-scale current, connect a 40kΩ resistor between FSADJB and GND.
11	FSADJA	DACA Full-Scale Adjust Input. For maximum full-scale output current, connect a 20kΩ resistor between FSADJA and GND. For minimum full-scale current, connect a 40kΩ resistor between FSADJA and GND.
12	OUTA	DACA Output. OUTA provides up to 30mA of output current.
14	V_{DD}	Power Supply Input. Connect V_{DD} to a +2.7 to +5.25V power supply. Bypass V_{DD} to GND with a 0.1µF capacitor as close to the device as possible.
—	EP	Exposed Pad. Connect to GND. Do not use as a substitute ground connection.

Detailed Description

Architecture

The MAX5550 10-bit, dual current-steering DAC (see the *Functional Diagram*) operates with DAC update rates up to 10Msps in SPI mode and 400ksps in I²C mode. The converter consists of a 16-bit shift register and input DAC registers, followed by a current-steering array. The current-steering array generates full-scale currents up to 30mA per DAC. An integrated +1.25V bandgap reference, control amplifier, and an external resistor determine each data converter's full-scale output range.

Reference Architecture and Operation

The MAX5550 provides an internal +1.25V bandgap reference or accepts an external reference voltage source between +0.5V and +1.5V. REFIN serves as the input for an external low-impedance reference source. Leave REFIN unconnected in internal reference mode. Internal or external reference mode is software selectable through the SPI/I²C serial interface.

The MAX5550's reference circuit (Figure 1) employs a control amplifier to regulate the full-scale current (I_{FS}) for the current outputs of the DAC. This device has a software-selectable full-scale current range (see the command summary in Table 4). After selecting a current range, an external resistor ($R_{FSADJ\_}$) sets the full-scale current. See Table 1 for a matrix of I_{FS} and R_{FSADJ} selections.

During startup, when the power is first applied, the MAX5550 defaults to the external reference mode, and to the 1mA–2mA full-scale current-range mode.

DAC Data

The 10-bit DAC data is decoded as offset binary, MSB first, with 1 LSB = I_{FS} / 1024, and converted into the corresponding current as shown in Table 2.

Serial Interface

The MAX5550 features a pin-selectable SPI/I²C serial interface. Connect SPI/$\overline{I2C}$ to GND to select I²C mode, or connect SPI/$\overline{I2C}$ to V_{DD} to select SPI mode. SDA and SCL (I²C mode) and DIN, SCLK, and $\overline{CS}$ (SPI mode) facilitate communication between the MAX5550 and the master. The serial interface remains active in shutdown.

I²C Compatibility (SPI/$\overline{I2C}$ = GND)

The MAX5550 is compatible with existing I²C systems (Figure 2). SCL and SDA are high-impedance inputs; SDA has an open-drain output that pulls the data line low during the ninth clock pulse. SDA and SCL require pullup resistors (2.4kΩ or greater) to V_{DD}. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals. The communication protocol supports standard I²C 8-bit communications. The device's address is compatible with 7-bit I²C addressing protocol only. Ten-bit address formats are not supported. Only write commands are accepted by the MAX5550.

Note: I²C readback is not supported.

Bit Transfer

One data bit transfers during each SCL rising edge. The MAX5550 requires nine clock cycles to transfer data into or out of the DAC register. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high.

START and STOP Conditions

The master initiates a transmission with a START condition (S), (a high-to-low transition on SDA with SCL high). The master terminates a transmission with a STOP condition (P), (a low-to-high transition on SDA while SCL is high) (Figure 3). A START condition from the master signals the beginning of a transmission to the MAX5550. The master terminates transmission by issuing a STOP condition. The STOP condition frees the bus. If a repeated START condition (S_r) is generated instead of a STOP condition, the bus remains active.

Table 1. Full-Scale Output Current and $R_{FSADJ\_}$ Selection Based on a +1.25V (typ) Reference Voltage

FULL-SCALE OUTPUT CURRENT (mA)*						R_{FSADJ} (kΩ)	
1mA–2mA	1.5mA–3mA	2.5mA–5mA	4.5mA–9mA	8mA–16mA	15mA–30mA	Calculated	1% EIA Std
1.00	1.500	2.500	4.500	8.00	15.00	40	40.2
1.25	1.875	3.125	5.625	10.00	18.75	35	34.8
1.50	2.250	3.750	6.750	12.00	22.50	30	30.1
1.75	2.625	4.375	7.875	14.00	26.25	25	24.9
2.00	3.000	5.000	9.000	16.00	30.00	20	20.0

**See the command summary in Table 4.*

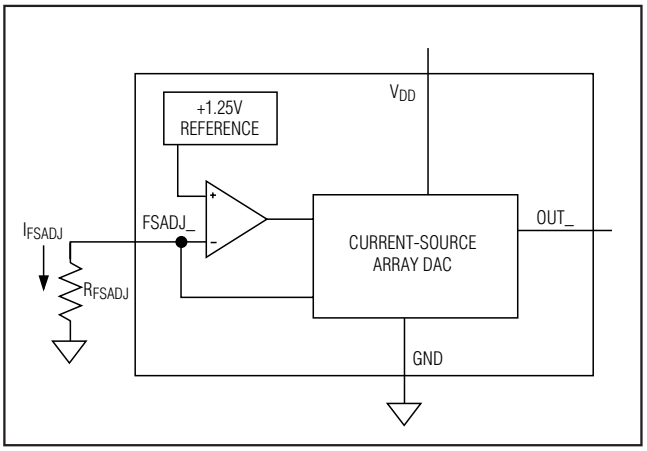


Figure 1. Reference Architecture and Output Current Adjustment

Table 2. DAC Output Code Table

DAC CODE	$I_{OUT\_}$
11 1111 1111	$1023 \times \frac{I_{FS}}{1024} - \lvert I_{OS} \rvert$
10 0000 0000	$512 \times \frac{I_{FS}}{1024} - \lvert I_{OS} \rvert$
00 0000 0001*	$\frac{I_{FS}}{1024} - \lvert I_{OS} \rvert$
00 0000 0000	0

**Negative output current values = 0*

Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

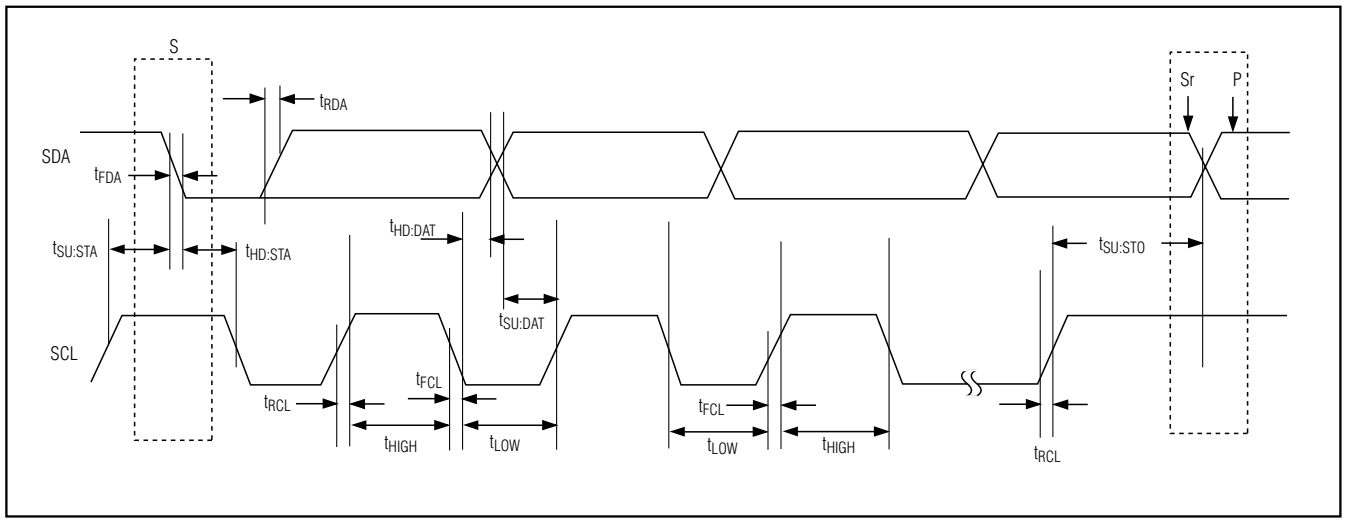


Figure 2. I²C Serial-Interface Timing Diagram

Early STOP Conditions

The MAX5550 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 4). This condition is not allowed in the I²C format.

Repeated START Conditions

A repeated START (S_r) condition is used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX5550's serial interface supports continuous write operations with an S_r condition separating them.

Acknowledge Bit (ACK)

Successful data transfers are acknowledged with an acknowledge bit (ACK). Both the master and the MAX5550 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 5).

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

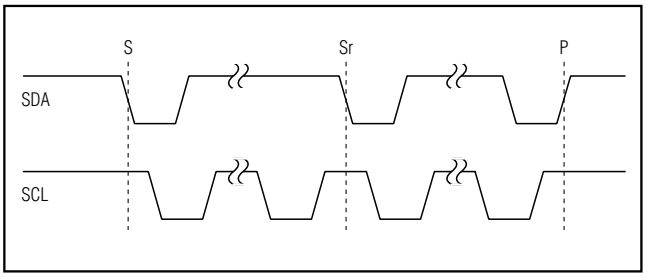


Figure 3. START and STOP Conditions

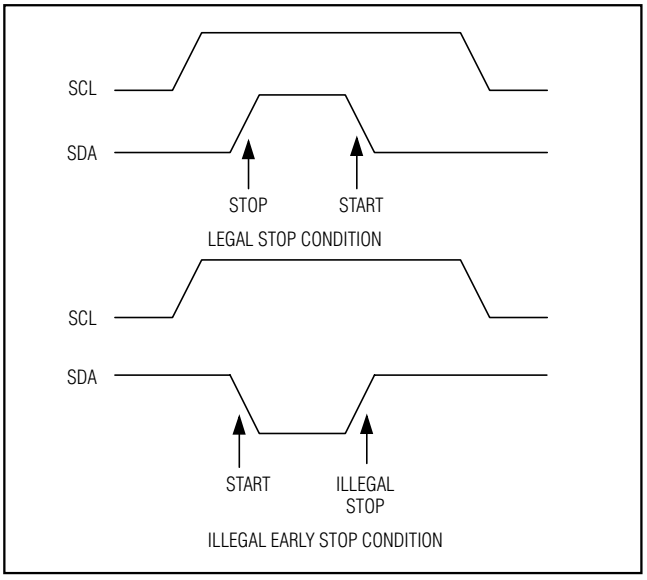


Figure 4. Early STOP Conditions

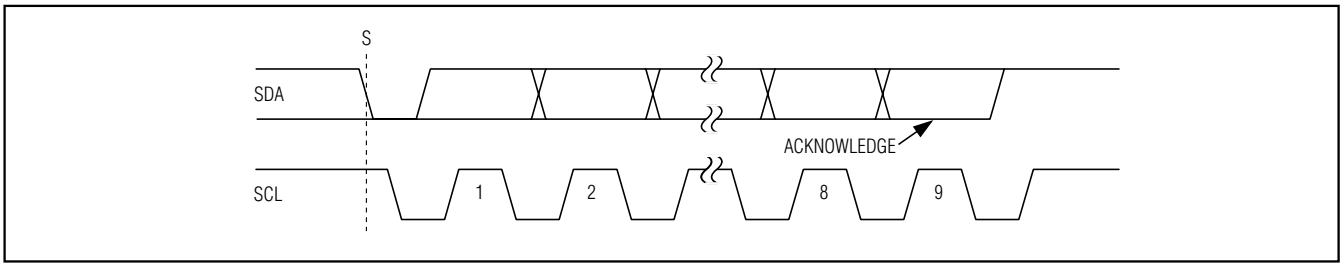


Figure 5. Acknowledge Condition

Table 3. Write Operation

	START	ADDRESS BYTE							R/$\overline{W}$*		COMMAND/DATA BYTE									DATA BYTE								STOP
Master SDA	S	0	1	1	0	0	A1	A0	0		C5	C4	C3	C2	C1	C0	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0		P
Slave SDA										ACK									ACK								ACK	

**Read operation not supported.*

Slave Address

A master initiates communication with a slave device by issuing a START condition followed by a slave address (see Table 3). The slave address consists of 7 address bits and a read/write bit (R/$\overline{W}$). When idle, the device continuously waits for a START condition followed by its slave address. When the device recognizes its slave address, it acquires the data and executes the command. The first 5 bits (MSBs) of the slave address have been factory programmed and are always 01100. Connect A1 and A0 to V_{DD} or GND to program the remaining 2 bits of the slave address. Set the least significant bit (LSB) of the address byte (R/$\overline{W}$) to zero to write to the MAX5550. After receiving the address, the MAX5550 (slave) issues an acknowledge by pulling SDA low for one clock cycle. I^2C read commands (R/$\overline{W}$ = 1) are not acknowledged by the MAX5550.

Write Cycle

The write command requires 27 clock cycles. In write mode (R/$\overline{W}$ = 0), the command/data byte that follows the address byte controls the MAX5550 (Table 3). The registers update on the rising edge of the 26th SCL pulse. Prematurely aborting the write cycle does not update the DAC. See Table 4 for a command summary.

SPI Compatibility (SPI/$\overline{I2C}$ = V_{DD})

The MAX5550 is compatible with the 3-wire SPI serial interface (Figure 6). This interface mode requires three inputs: chip-select ($\overline{CS}$), data clock (SCLK), and data in (DIN). Drive $\overline{CS}$ low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge.

The MAX5550 requires 16 clock cycles to clock in 6 command bits (C5–C0) and 10 data bits (D9–D0) (Figure 7). After loading data into the shift register, drive $\overline{CS}$ high to latch the data into the appropriate DAC register and disable the serial interface. Keep $\overline{CS}$ low during the entire serial data stream to avoid corruption of the data. See Table 4 for a command summary.

Shutdown Mode

The MAX5550 has a software shutdown mode that reduces the supply current to less than 1µA. Shutdown mode disables the DAC outputs. The serial interface remains active in shutdown. This provides the flexibilty to update the registers while in shut down. Recycling the power supply resets the device to the default settings.

Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

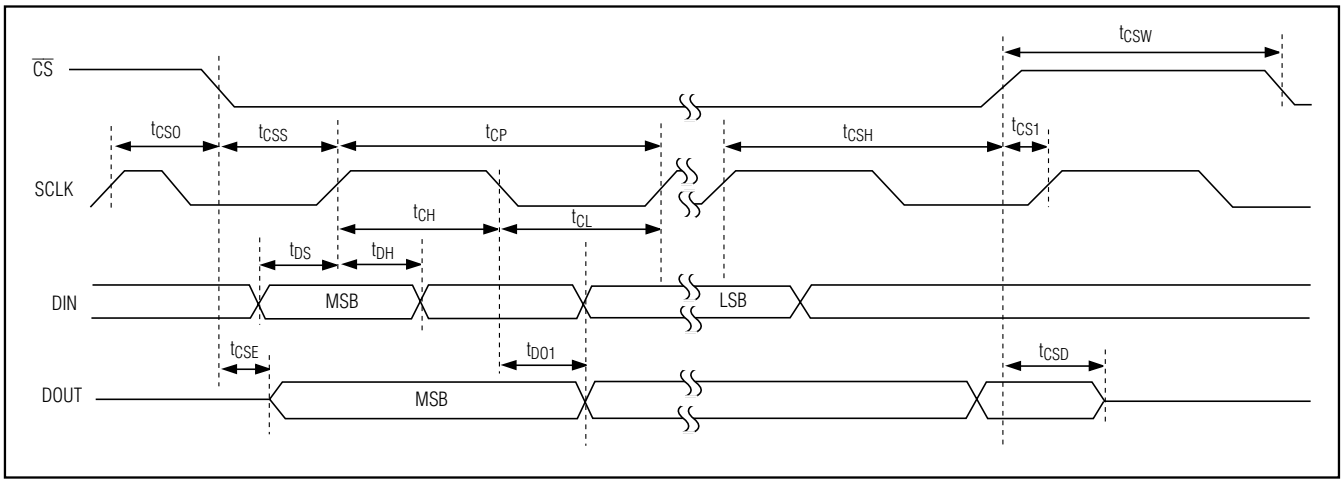


Figure 6. SPI-Interface Timing Diagram

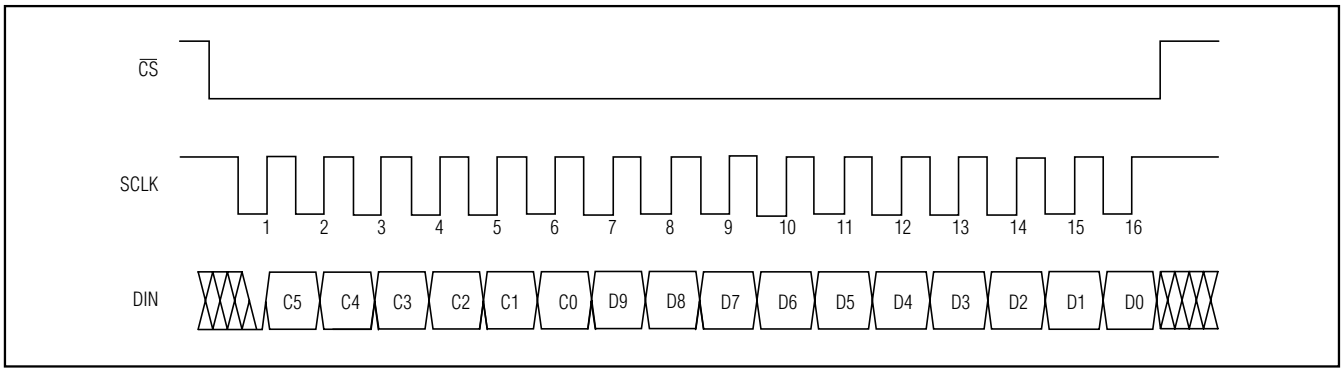


Figure 7. SPI-Interface Format

Applications Information

Daisy Chaining (SPI/$\overline{I2C}$ = VDD)

In standard SPI-/QSPI™-/MICROWIRE™-compatible systems, a microcontroller (µC) communicates with its slave devices through a 3- or 4-wire serial interface. The typical interface includes a chip-select signal ($\overline{CS}$), a serial clock (SCLK), a data input signal (DIN), and sometimes a data signal output (DOUT). In this system, the µC allots an independent slave-select signal ($\overline{SS\_}$) to each slave device so that they can be addressed individually. Only the slaves with their $\overline{CS}$ inputs asserted low acknowledge and respond to the activity on the serial clock and data lines. This is simple to implement when there are very few slave devices in the system. An alternative method is daisy chaining. Daisy chaining, in serial-interface applications, is the method of propagating commands through devices connected in series (see Figure 8).

Daisy chain devices by connecting the DOUT of one device to the DIN of the next. Connect the SCLK of all devices to a common clock and connect the $\overline{CS}$ of all devices to a common slave-select line. Data shifts out of DOUT 16.5 clock cycles after it is shifted into DIN on the falling edge of SCLK. In this configuration, the µC only needs three signals ($\overline{SS}$, SCK, and MOSI) to control all of the slaves in the network. The SPI-/QSPI-/MICROWIRE-compatible serial interface normally works at up to 10MHz, but must be slowed to 5MHz if daisy chaining. DOUT is high impedance when $\overline{CS}$ is high.

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Table 4. Command Summary

SERIAL DATA INPUT							FUNCTIONS
C5	C4	C3	C2	C1	C0	D9–D0	
0	0	0	0	0	0	XXXXXXXXXX	No operation.
0	0	0	0	0	1	10-bit DAC data	Load DAC data to both DAC registers and both input registers from the shift register.
0	0	0	0	1	0	10-bit DAC data	Load DAC register A and input register A from the shift register.
0	0	0	0	1	1	10-bit DAC data	Load DAC register B and input register B from the shift register.
0	0	0	1	0	0	10-bit DAC data	Load both channel input registers from the shift register, both DAC registers are unchanged.
0	0	0	1	0	1	10-bit DAC data	Load input register A from the shift register; DAC register A is unchanged.
0	0	0	1	1	0	10-bit DAC data	Load input register B from the shift register; DAC register B is unchanged.
0	0	0	1	1	1	XXXXXXXXXX	Update both DAC registers from their corresponding input registers.
0	0	1	0	0	1	XXXXXXXXXX	Update DAC register A from input register A.
0	0	1	0	1	0	XXXXXXXXXX	Update DAC register B from input register B.
0	0	1	0	1	1	XXXXXXXXXX	Internal reference mode.
0	0	1	1	0	0	XXXXXXXXXX	External reference mode (default mode at power-up).
0	0	1	1	0	1	XXXXXXXXXX	Shut down both DACs.
0	0	1	1	1	0	XXXXXXXXXX	Shut down DACA.
0	0	1	1	1	1	XXXXXXXXXX	Shut down DACB.
0	1	0	0	0	0	XXXXXXXXXX	DACA 1mA–2mA full-scale current range mode (default mode at power-up)
0	1	0	0	0	1	XXXXXXXXXX	DACA 1.5mA–3mA full-scale current range mode.
0	1	0	0	1	0	XXXXXXXXXX	DACA 2.5mA–5mA full-scale current range mode.
0	1	0	0	1	1	XXXXXXXXXX	DACA 4.5mA–9mA full-scale current range mode.
0	1	0	1	0	0	XXXXXXXXXX	DACA 8mA–16mA full-scale current range mode.
0	1	0	1	0	1	XXXXXXXXXX	DACA 15mA–30mA full-scale current range mode.
1	0	1	1	0	1	XXXXXXXXXX	Power up both DACs.
1	0	1	1	1	0	XXXXXXXXXX	Power up DACA.
1	0	1	1	1	1	XXXXXXXXXX	Power up DACB.
1	1	0	0	0	0	XXXXXXXXXX	DACB 1mA–2mA full-scale current range mode (default mode at power-up)
1	1	0	0	0	1	XXXXXXXXXX	DACB 1.5mA–3mA full-scale current range mode.
1	1	0	0	1	0	XXXXXXXXXX	DACB 2.5mA–5mA full-scale current range mode.
1	1	0	0	1	1	XXXXXXXXXX	DACB 4.5mA–9mA full-scale current range mode.
1	1	0	1	0	0	XXXXXXXXXX	DACB 8mA–16mA full-scale current range mode.
1	1	0	1	0	1	XXXXXXXXXX	DACB 15mA–30mA full-scale current range mode.

Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

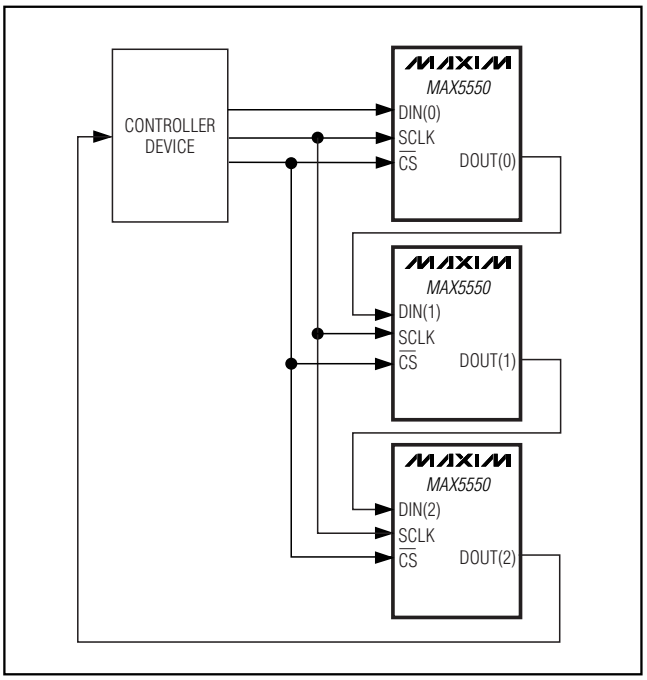


Figure 8. Daisy-Chain Configuration

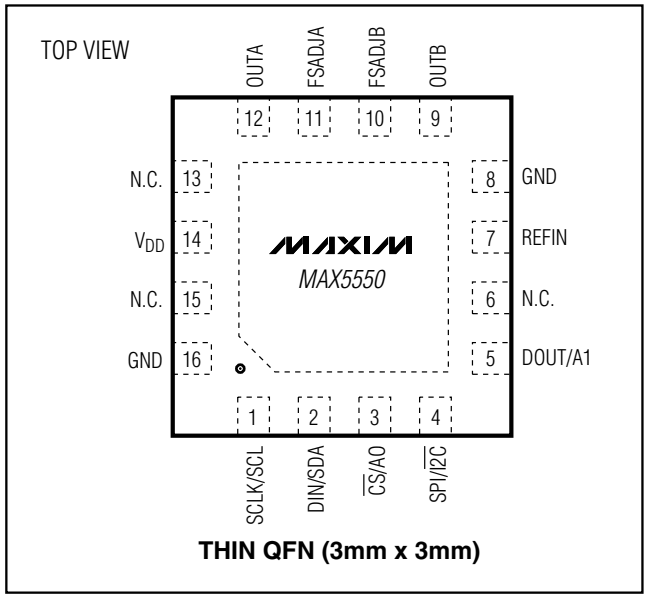
Power Sequencing

Ensure that the voltage applied to REFIN does not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REFIN and V_{DD} to ensure compliance with the absolute maximum ratings.

Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND create noise at the analog output. Return GND to the highest quality ground plane available. For extremely noisy environments, bypass REFIN and V_{DD} to GND with 1µF and 0.1µF capacitors with the 0.1µF capacitor as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

Pin Configuration



Chip Information

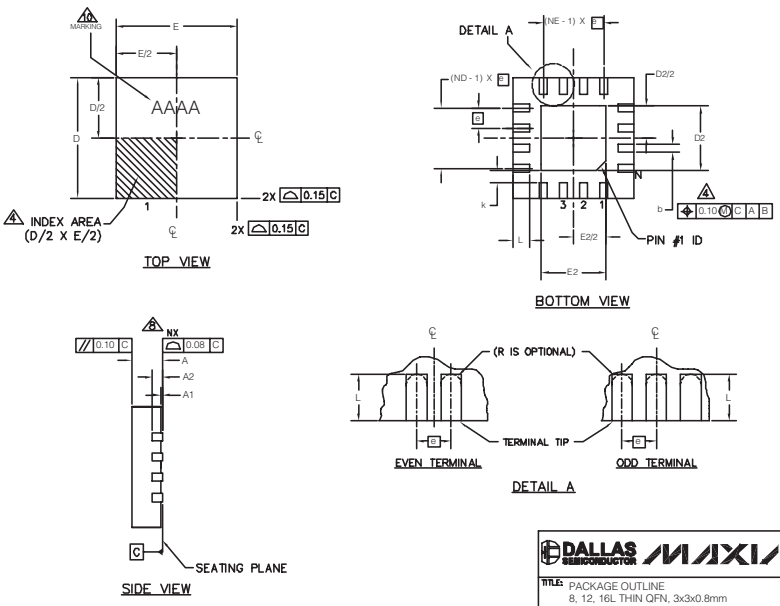
PROCESS: BiCMOS

Dual, 10-Bit, Programmable, 30mA High-Output-Current DAC

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. I | 1/2

–DRAWING NOT TO SCALE–

PKG.	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS .
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

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