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# 1 Block diagram and pin descriptions

Figure 1. Block diagram

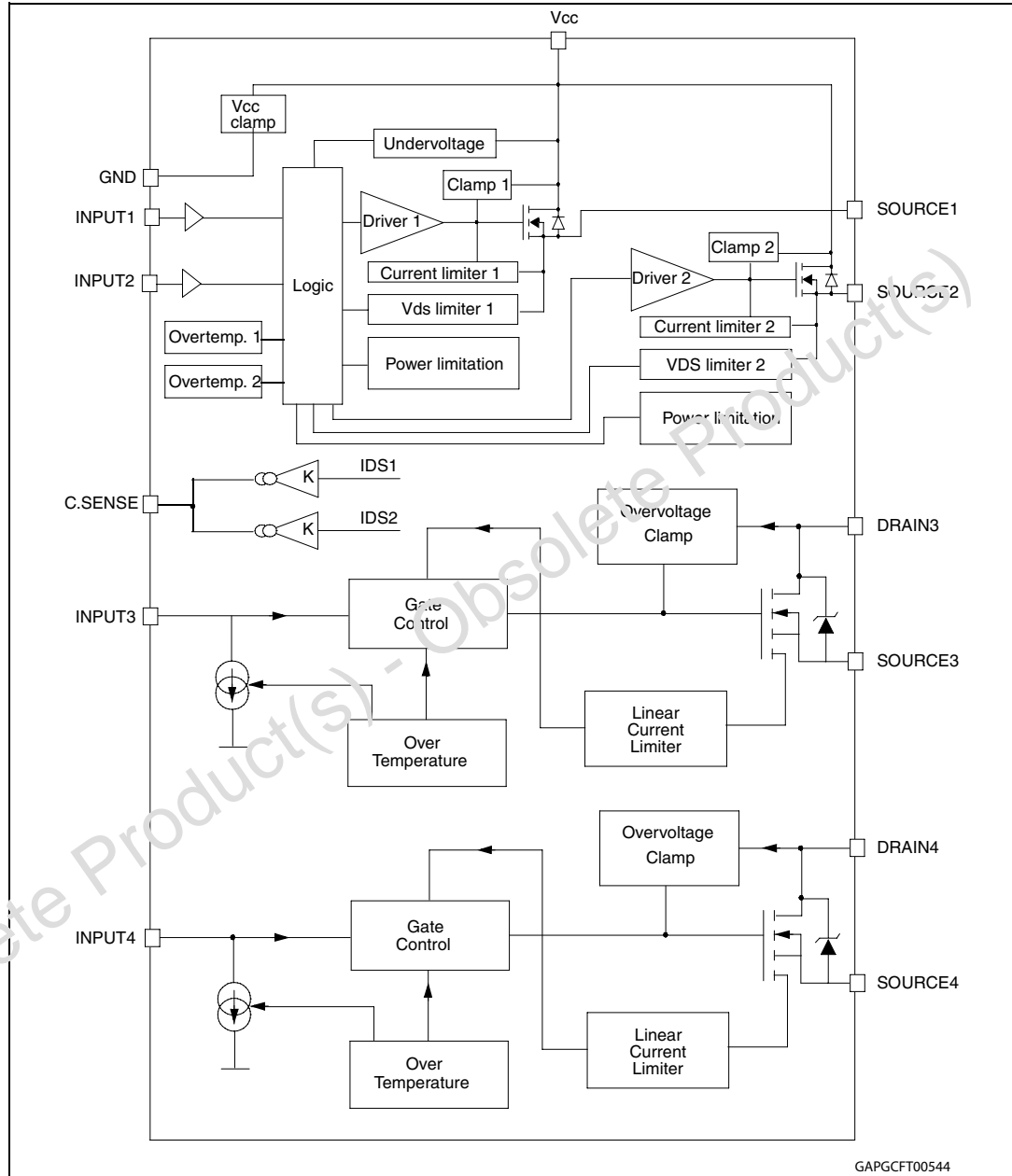


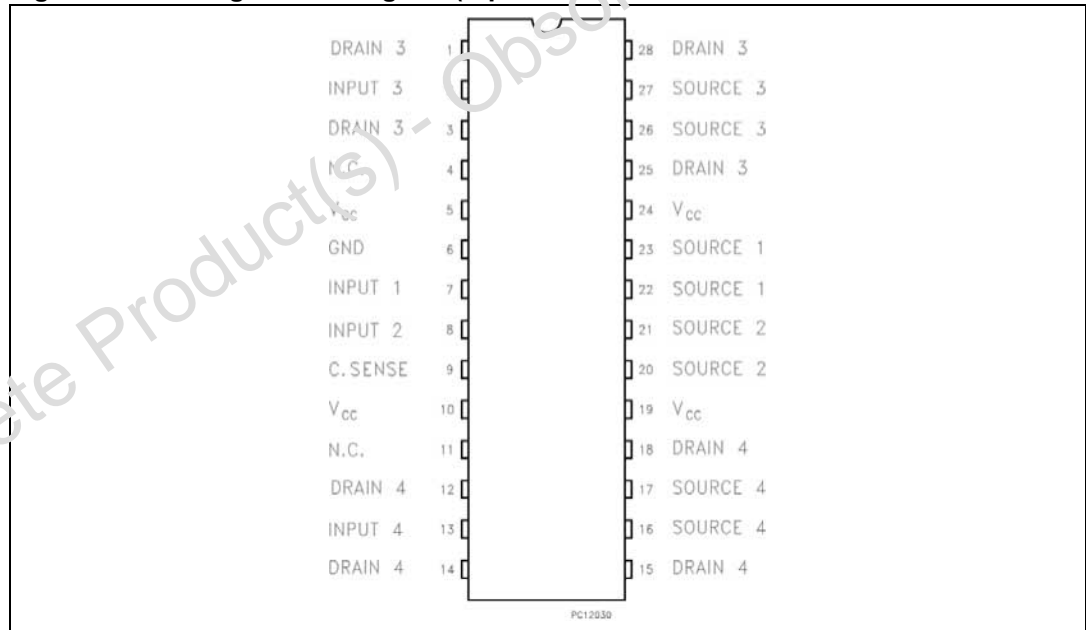
Table 1. Pin descriptions

No	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of Switch 3 (low-side switch)
2	INPUT 3	Input of Switch 3 (low-side switch)
4, 11	N.C.	Not Connected

**Table 1. Pin descriptions (continued)**

No	Name	Function
5, 10, 19, 24	V <sub>CC</sub>	Drain of Switches 1 and 2 (high-side switches) and Power Supply Voltage
6	GND	Ground of Switches 1 and 2 (high-side switches)
7	INPUT 1	Input of Switch 1 (high-side switches)
8	INPUT 2	Input of Switch 2 (high-side switch)
9	CURRENT SENSE	Analog current sense pin, it delivers a current proportional to the load current
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of Switch 4 (low-side switch)
16, 17	SOURCE 4	Source of Switch 4 (low-side switch)
20, 21	SOURCE 2	Source of Switch 2 (high-side switch)
22, 23	SOURCE 1	Source of Switch 1 (high-side switch)
26, 27	SOURCE 3	Source of Switch 3 (low-side switch)

**Figure 2. Configuration diagram (top view)**



**Table 2. Thermal data**

Symbol	Parameter	Max value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-lead (high-side switch)	10	°C/W
R <sub>thj-case</sub>	Thermal resistance junction-lead (low-side switch)	7	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	See <a href="#">Figure 39</a>	°C/W

## 2 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) and [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in [Section 2.1: Absolute maximum ratings](#) for extended periods may affect device reliability.

### 2.1 Absolute maximum ratings

**Table 3. Dual high-side switch**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-12	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current	-1 to 10	mA
$V_{CSSENSE}$	Current sense maximum voltage	$V_{CC}-41$	V
		$+V_{CC}$	V
$E_{MAX}$	Maximum switching energy (single pulse) ( $L = 3.7\text{mH}$ ; $R_L = 0\Omega$ ; $V_{bat} = 13.5\text{V}$ ; $T_{jstart} = 150^\circ\text{C}$ ; $I_{OUT} = I_{lim}(typ.)$ )	32	mJ
$V_{ESD}$	Electrostatic Discharge (Human Body Model: $R = 1.5\text{K}\Omega$ ; $C = 100\text{pF}$ )		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
$V_{ESD}$	Charge device model (CDM-AEC-Q100-011)	5000	V
		750	V
$T_j$	Junction operating temperature	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

Table 4. Low-side switch

Symbol	Parameter	Value	Unit
$V_{DSn}$	Drain-source voltage ( $V_{INn} = 0V$ )	Internally clamped	V
$V_{INn}$	Input voltage	Internally clamped	V
$I_{INn}$	Input current	+/-20	mA
$R_{IN\ MINn}$	Minimum input series impedance	220	$\Omega$
$I_{Dn}$	Drain current	Internally limited	A
$I_{Rn}$	Reverse DC output current	-12	A
$V_{ESD1}$	Electrostatic discharge ( $R = 1.5K\Omega$ , $C = 100pF$ )	4000	V
$V_{ESD2}$	Electrostatic discharge on output pins only ( $R = 330\Omega$ , $C = 150pF$ )	16500	V
$P_{tot}$	Total dissipation at $T_c = 25^\circ C$	4	W
$T_j$	Operating junction temperature	Internally limited	$^\circ C$
$T_c$	Case operating temperature	Internally limited	$^\circ C$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ C$

### 3 Electrical characteristics

#### 3.1 Electrical characteristics for dual high-side switch

Values specified in this section are for  $8V < V_{CC} < 36V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise specified (for each channel).

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	36	V
$V_{USD}$	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
$R_{ON}$	On state resistance	$I_{OUT} = 3A$ ; $T_j = 25^{\circ}C$			160	m $\Omega$
		$I_{OUT} = 3A$ ; $T_j = 150^{\circ}C$			320	m $\Omega$
		$I_{OUT} = 3A$ ; $V_{CC} = 5V$ ; $T_j = 25^{\circ}C$			210	m $\Omega$
$V_{clamp}$	Clamp voltage	$I_S = 20\text{ mA}$	41	46	52	V
$I_S$	Supply current	Off State; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$ ; $V_{IN} = V_{OUT} = V_{SENSE} = 0V$		2 <sup>(1)</sup>	5 <sup>(1)</sup>	$\mu A$
		On State; $V_{CC} = 13V$ ; $V_{IN} = 5V$ ; $I_{OUT} = 0A$		3	6	mA
$I_{L(off)}$	Off state output current <sup>(2)</sup>	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$	0		3	$\mu A$
		$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 125^{\circ}C$	0		5	$\mu A$
$V_F$	Output - $V_{CC}$ diode voltage <sup>(2)</sup>	$-I_{OUT} = 3A$ ; $T_j = 150^{\circ}C$			0.7	V

1. PowerMOS leakage included

2. For each channel

**Table 6. Switching ( $V_{CC} = 13V$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 4.3\Omega$ (see <a href="#">Figure 3</a> )	—	15	—	$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 4.3\Omega$ (see <a href="#">Figure 3</a> )	—	10	—	$\mu s$
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 4.3\Omega$	—	See <a href="#">Figure 15</a>	—	V/ $\mu s$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 4.3\Omega$	—	See <a href="#">Figure 17</a>	—	V/ $\mu s$
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 4.3\Omega$ (see <a href="#">Figure 3</a> )	—	0.16	—	mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 4.3\Omega$ (see <a href="#">Figure 3</a> )	—	0.08	—	mJ



**Table 7. Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9V$	1			$\mu A$
$V_{IH}$	Input high level voltage		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1V$			10	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$	5.5		7	V
		$I_{IN} = -1mA$		-0.7		V

**Table 8. Protection and diagnostics<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC Short circuit current	$V_{CC} = 13V$	6	8.5	12	A
		$5V < V_{CC} < 36V$			12	A
$I_{limL}$	Short circuit current during thermal cycling	$V_{CC} = 13V; T_R < T_J < T_{TSD}$		3.5		A
$T_{TSD}$	Shutdown temperature		150	175	200	$^{\circ}C$
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
$T_{RS}$	Thermal reset of STATUS		135			$^{\circ}C$
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		$^{\circ}C$
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 1A; V_{IN} = 0; L = 20mH$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.03A; T_j = -40^{\circ}C$ to $150^{\circ}C$ (see <a href="#">Figure 4</a> )		25		mV

<sup>(1)</sup> To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

**Table 9. Current sense (8V<V<sub>CC</sub><16V)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K <sub>0</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.08 A; V <sub>SENSE</sub> = 0.5 V; T <sub>j</sub> = -40°C to 150°C	1266	1900	3100	
K <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.35 A; V <sub>SENSE</sub> = 0.5V; T <sub>j</sub> = -40°C to 150°C T <sub>j</sub> = 25°C to 150°C	840 980	1360 1360	2000 1740	
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 3A; V <sub>SENSE</sub> = 4V; T <sub>j</sub> = -40°C to 150°C	1200	1270	1350	
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 4A; V <sub>SENSE</sub> = 4V; T <sub>j</sub> = -40°C to 150°C	1200	1270	1350	
I <sub>SENSE0</sub>	Analog sense current	I <sub>OUT</sub> = 0A; V <sub>SENSE</sub> = 0V; V <sub>IN</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	0		1	μA
		I <sub>OUT</sub> = 0A; V <sub>SENSE</sub> = 0V; V <sub>IN</sub> = 5V; T <sub>j</sub> = -40°C to 150°C	0		2	μA
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> = 5A; R <sub>SENSE</sub> = 3.9KΩ	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in overtemperature condition	V <sub>CC</sub> = 13V; R <sub>SENSE</sub> = 3.9KΩ		9		V
I <sub>SENSEH</sub>	Analog sense output current in overtemperature condition	V <sub>CC</sub> = 13V		8		mA
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> < 4V; 0.35A < I <sub>out</sub> < 5A; I <sub>SENSE</sub> = 90% of I <sub>SENSE</sub> max (see <a href="#">Figure 5</a> )		70	300	μs
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> < 4V; 0.35A < I <sub>out</sub> < 5A; I <sub>SENSE</sub> = 10% of I <sub>SENSE</sub> max (see <a href="#">Figure 5</a> )		100	250	μs

**Figure 3. Switching time waveforms**

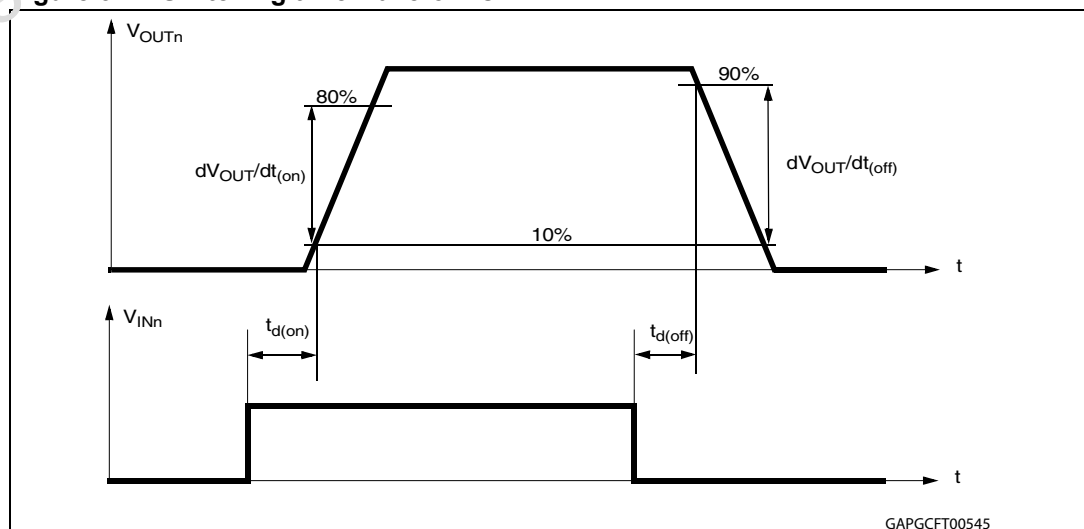


Figure 4. Output voltage drop limitation

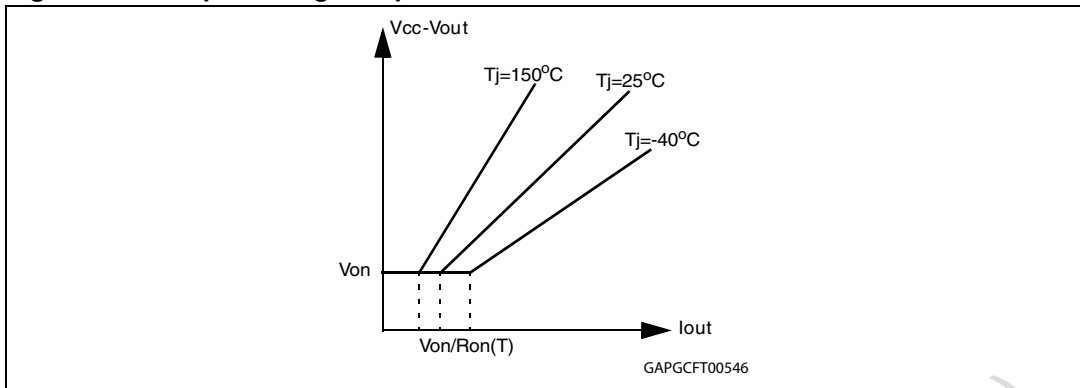
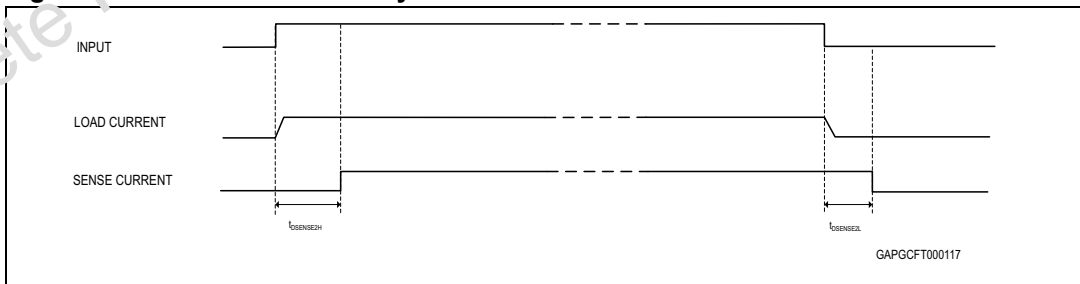


Table 10. Truth table

Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	0
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Figure 5. Current sense delay characteristics



### 3.2 Electrical characteristics curves for dual high-side switch

Figure 6. Off-state output current

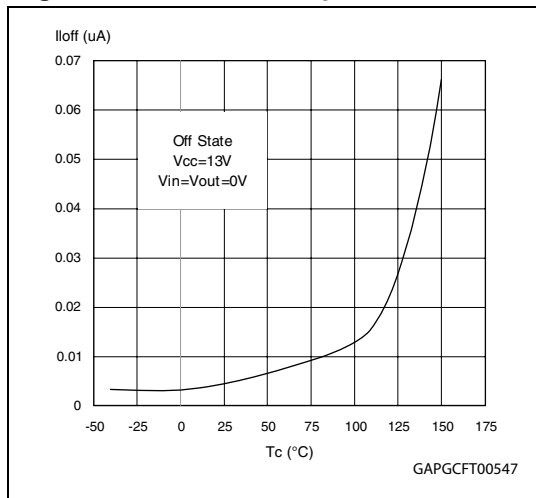


Figure 7. High level input current

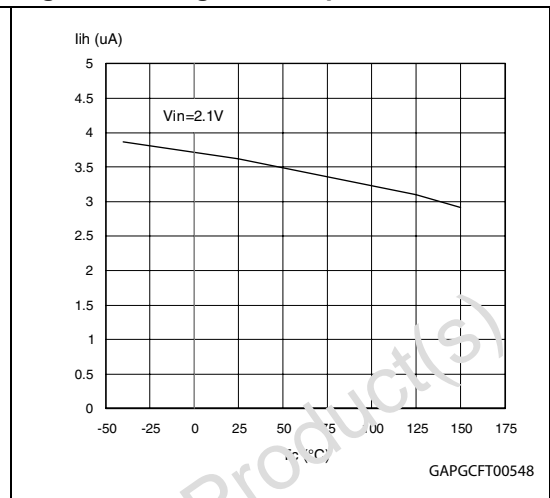


Figure 8. Input clamp voltage

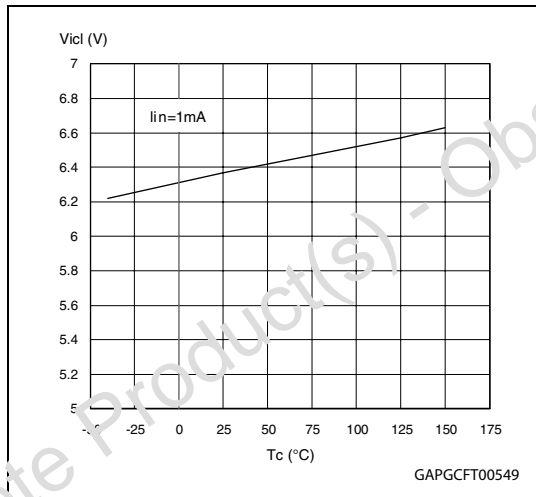


Figure 9. Input low level

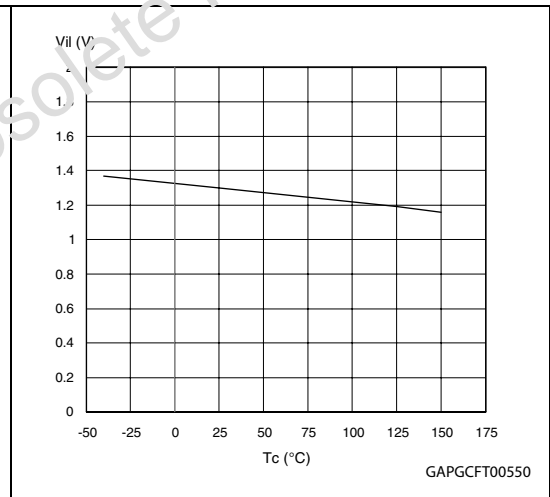


Figure 10. Input high level

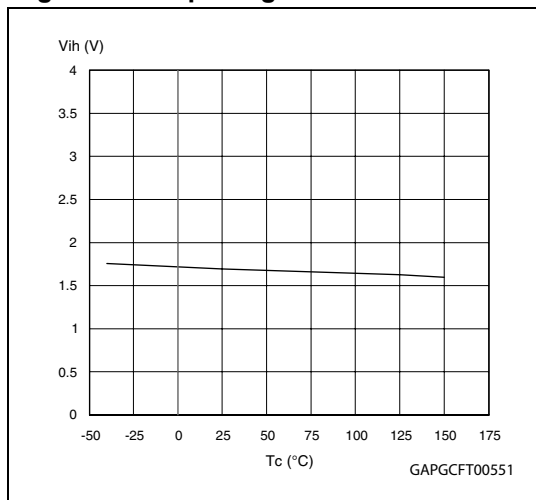


Figure 11. Input hysteresis voltage

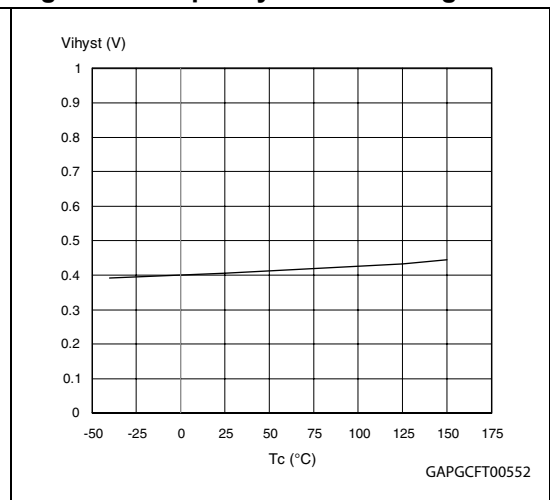


Figure 12. On-state resistance vs  $T_{case}$

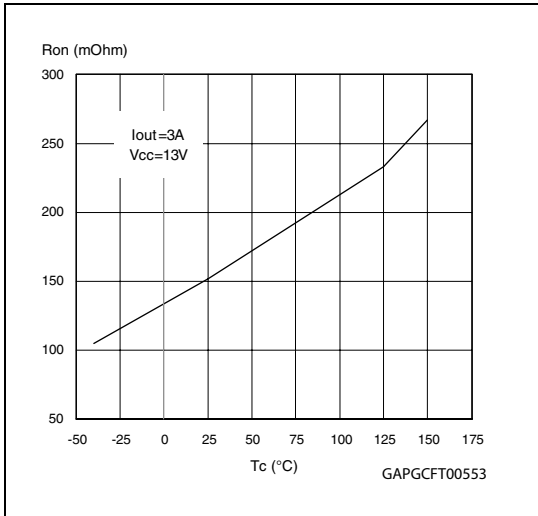


Figure 13. On-state resistance vs  $V_{CC}$

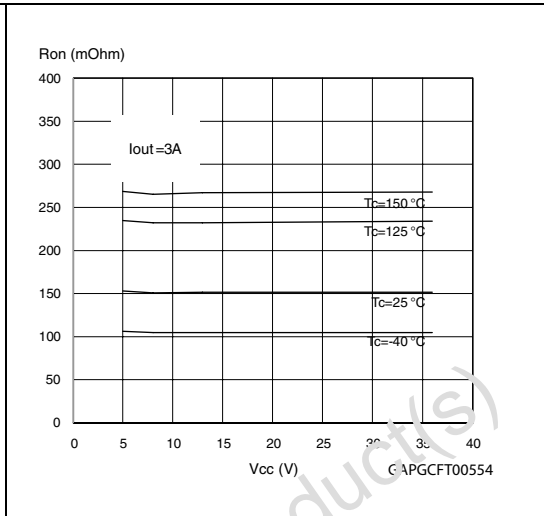


Figure 14. Undervoltage shutdown

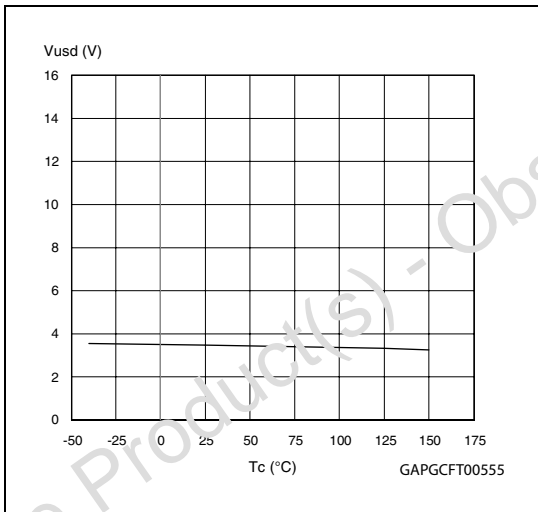


Figure 15. Turn-on voltage slope

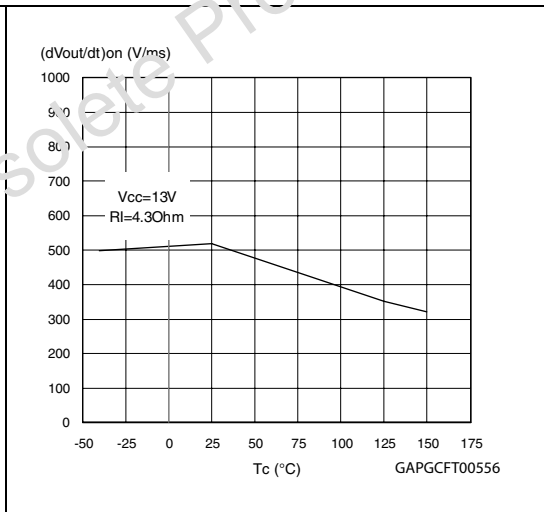


Figure 16.  $I_{LIMH}$  vs  $T_{case}$

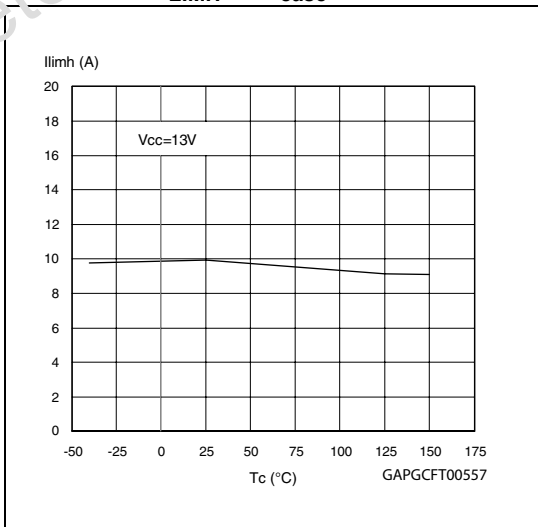
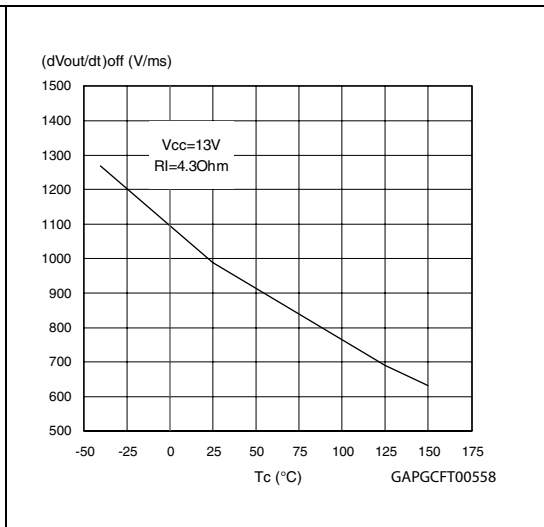


Figure 17. Turn-off voltage slope



### 3.3 Electrical characteristics for low-side switches

Values specified in this section are for  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$ , unless otherwise specified

**Table 11. Off**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{\text{CLAMP}}$	Drain-source clamp voltage	$V_{\text{IN}}=0\text{V}; I_{\text{D}} = 1.5\text{A}$	40	45	55	V
$V_{\text{CLTH}}$	Drain-source clamp threshold voltage	$V_{\text{IN}} = 0\text{V}; I_{\text{D}} = 2\text{mA}$	36			V
$V_{\text{INTH}}$	Input threshold voltage	$V_{\text{DS}} = V_{\text{IN}}; I_{\text{D}} = 1\text{mA}$	0.5		2.5	V
$I_{\text{ISS}}$	Supply current from input pin	$V_{\text{DS}}=0\text{V}; V_{\text{IN}} = 5\text{V}$		100	150	$\mu\text{A}$
$V_{\text{INCL}}$	Input-source clamp voltage	$I_{\text{IN}} = 1\text{mA}$	6	6.8	7	V
		$I_{\text{IN}} = -1\text{mA}$	-1.0		-0.3	V
$I_{\text{DSS}}$	Zero input voltage drain current ( $V_{\text{IN}} = 0\text{V}$ )	$V_{\text{DS}} = 13\text{V}; V_{\text{IN}} = 0\text{V}; T_j = 25^{\circ}\text{C}$			30	$\mu\text{A}$
		$V_{\text{DS}} = 25\text{V}; V_{\text{IN}} = 0\text{V}$			75	$\mu\text{A}$

**Table 12. On**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{\text{DS(on)}}$	Static drain-source on resistance	$V_{\text{IN}} = 5\text{V}; I_{\text{D}} = 3\text{A}; T_j = 25^{\circ}\text{C}$	—	—	120	$\text{m}\Omega$
		$V_{\text{IN}} = 5\text{V}; I_{\text{D}} = 3\text{A}$	—	—	240	$\text{m}\Omega$

**Table 13. Dynamic ( $T_j = 25^{\circ}\text{C}$ , unless otherwise specified)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$g_{\text{fs}}$	Forward transconductance	$V_{\text{DD}} = 13\text{V}; I_{\text{D}} = 1.5\text{A}$	—	2.5	—	S
$C_{\text{OSS}}$	Output capacitance	$V_{\text{DS}} = 13\text{V}; f = 1\text{MHz}; V_{\text{IN}} = 0\text{V}$	—	150	—	pF

**Table 14. Switching ( $T_j = 25^{\circ}\text{C}$ , unless otherwise specified)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 15\text{V}; I_{\text{D}} = 3\text{A}; V_{\text{gen}} = 5\text{V}; R_{\text{gen}} = R_{\text{IN MINn}} = 220\Omega$	—	200	400	ns
$t_{\text{r}}$	Rise time		—	1.2	2.5	$\mu\text{s}$
$t_{\text{d(off)}}$	Turn-off delay time		—	600	1350	ns
$t_{\text{f}}$	Fall time		—	400	1000	ns
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 15\text{V}; I_{\text{D}} = 3\text{A}; V_{\text{gen}} = 5\text{V}; R_{\text{gen}} = 2.2\text{K}\Omega$	—	0.80	2.5	$\mu\text{s}$
$t_{\text{r}}$	Rise time		—	3.7	7.5	$\mu\text{s}$
$t_{\text{d(off)}}$	Turn-off delay time		—	2.6	7.5	$\mu\text{s}$
$t_{\text{f}}$	Fall time		—	2.3	7.0	$\mu\text{s}$

**Table 14. Switching ( $T_j = 25^\circ\text{C}$ , unless otherwise specified) (continued)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{V}; I_D = 3\text{A}; V_{gen} = 5\text{V}; R_{gen} = R_{IN\ MINn} = 220\Omega$	—	3.0		A/ $\mu\text{s}$
$Q_i$	Total input charge	$V_{DD} = 12\text{V}; I_D = 3\text{A}; V_{IN} = 5\text{V}; I_{gen} = 2.13\text{mA}$	—	9.0		nC

**Table 15. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=1.5\text{A}; V_{IN}=0\text{V}$	—	0.8	—	V
$t_{rr}$	Reverse recovery time	$I_{SD}=1.5\text{A}; di/dt=12\text{A/ms}; V_{DD}=30\text{V}; L=200\mu\text{H}$	—	400	—	ns
$Q_{rr}$	Reverse recovery charge		—	200	—	nC
$I_{RRM}$	Reverse recovery current		—	1.0	—	A

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

**Table 16. Protection and diagnostics ( $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise specified)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{lim}$	Drain current limit	$V_{IN}=5\text{V}; V_{DS}=13\text{V}$	6	8.5	12	A
$t_{dlim}$	Step response current limit	$V_{IN} = 5\text{V}; V_{DS}=13\text{V}$		10		$\mu\text{s}$
$T_{jsh}$	Overtemperature shutdown		150	175	200	$^\circ\text{C}$
$T_{jrs}$	Overtemperature reset		135			$^\circ\text{C}$
$I_{gf}$	Fault sink current	$V_{IN} = 5\text{V}; V_{DS} = 13\text{V}; T_j = T_{jsh}$	10	15	20	mA
$E_{as}$	Single pulse avalanche energy	Starting $T_j = 25^\circ\text{C}; V_{DD} = 24\text{V}; V_{IN} = 5\text{V}; R_{gen} = R_{IN\ MINn} = 220\Omega; L = 24\text{mH}$	100			mJ

### 3.4 Electrical characteristics for low-side switches

Figure 18. Static drain source on resistance

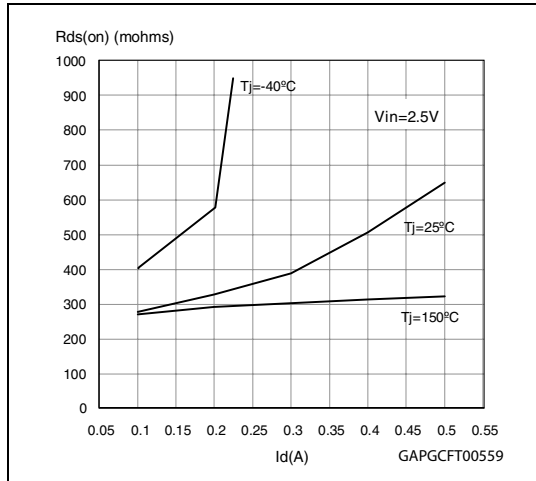


Figure 19. Derating curve

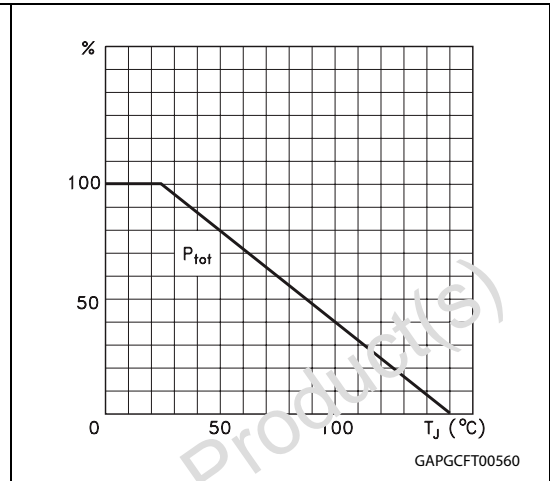


Figure 20. Transconductance

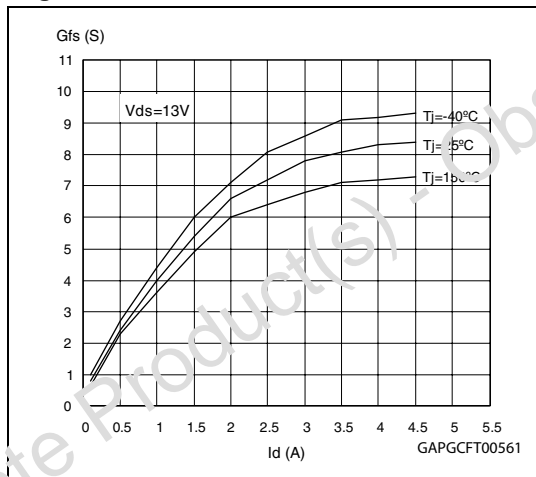


Figure 21. Transfer characteristics

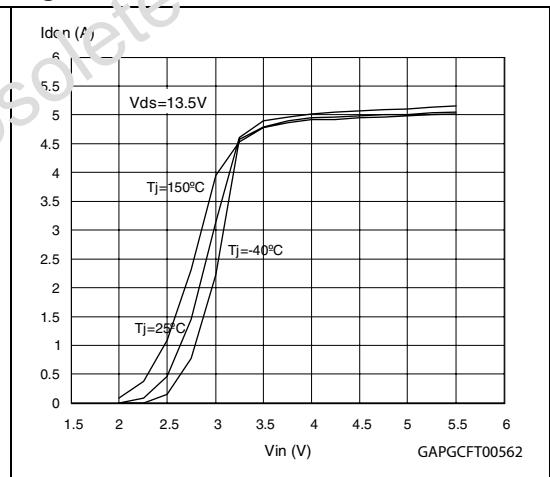


Figure 22. Input voltage vs input charge

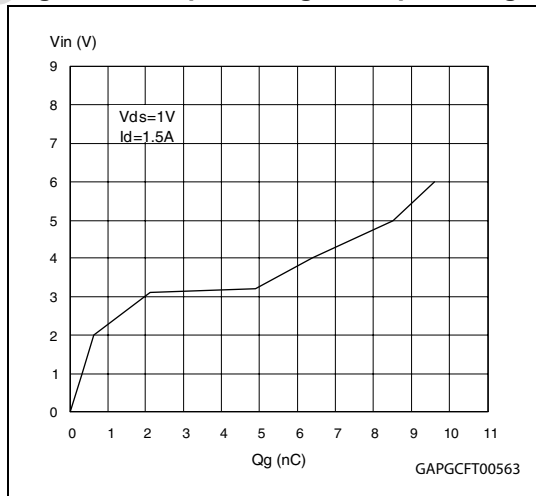


Figure 23. Capacitance variations

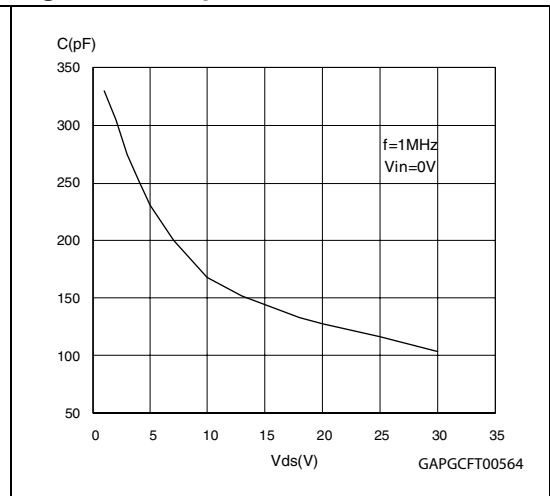




Figure 24. Output characteristics

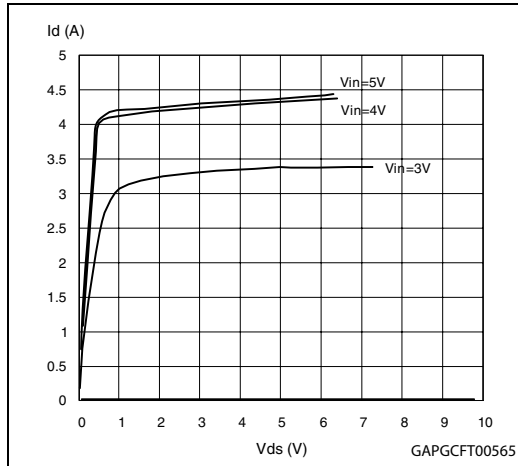


Figure 25. Step response current limit

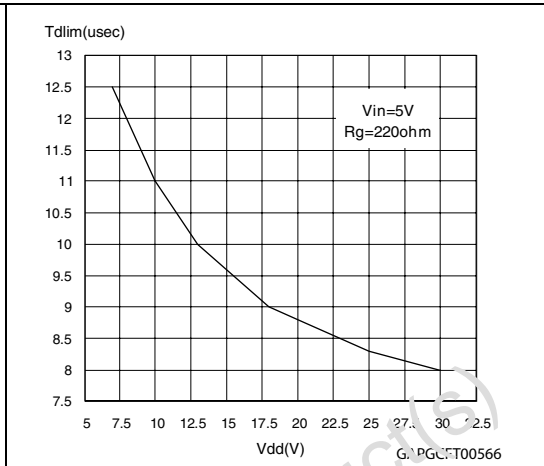


Figure 26. Source-drain diode forward characteristics

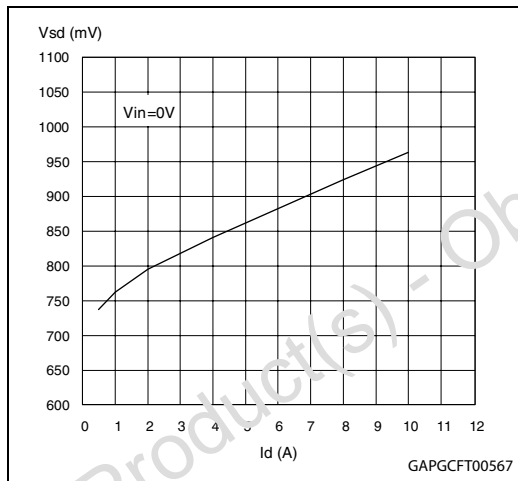


Figure 27. Static drain-source on resistance vs Id

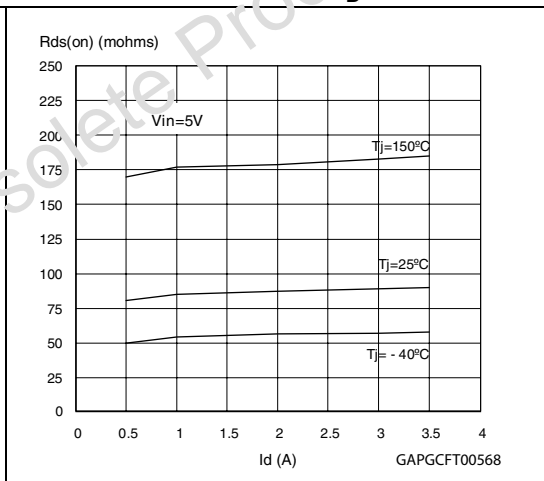


Figure 28. Static drain-source on resistance vs input voltage (part 1)

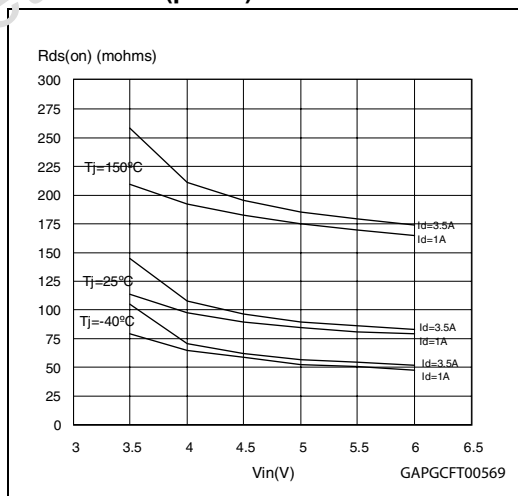
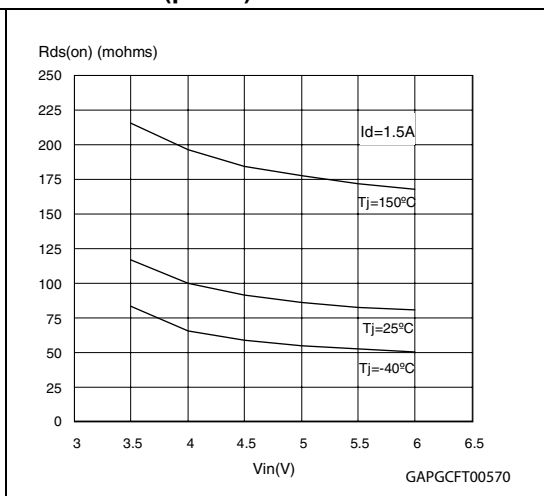
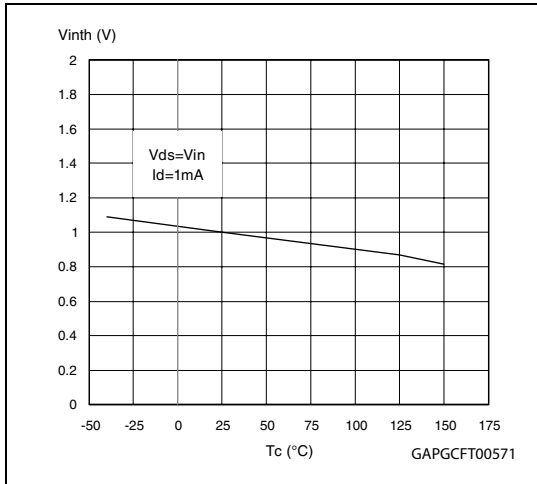


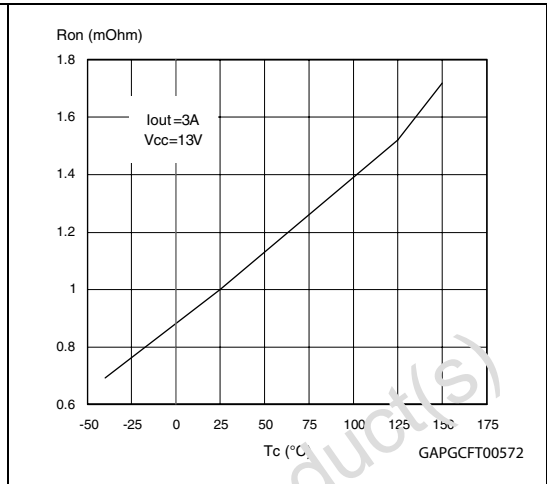
Figure 29. Static drain-source on resistance vs input voltage (part 2)



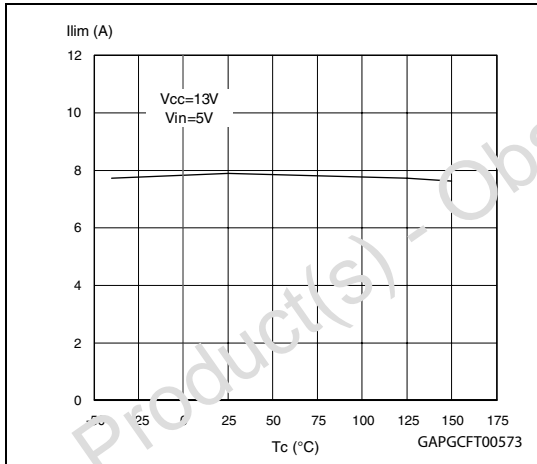
**Figure 30. Normalized input threshold voltage vs temperature**



**Figure 31. Normalized on resistance vs temperature**



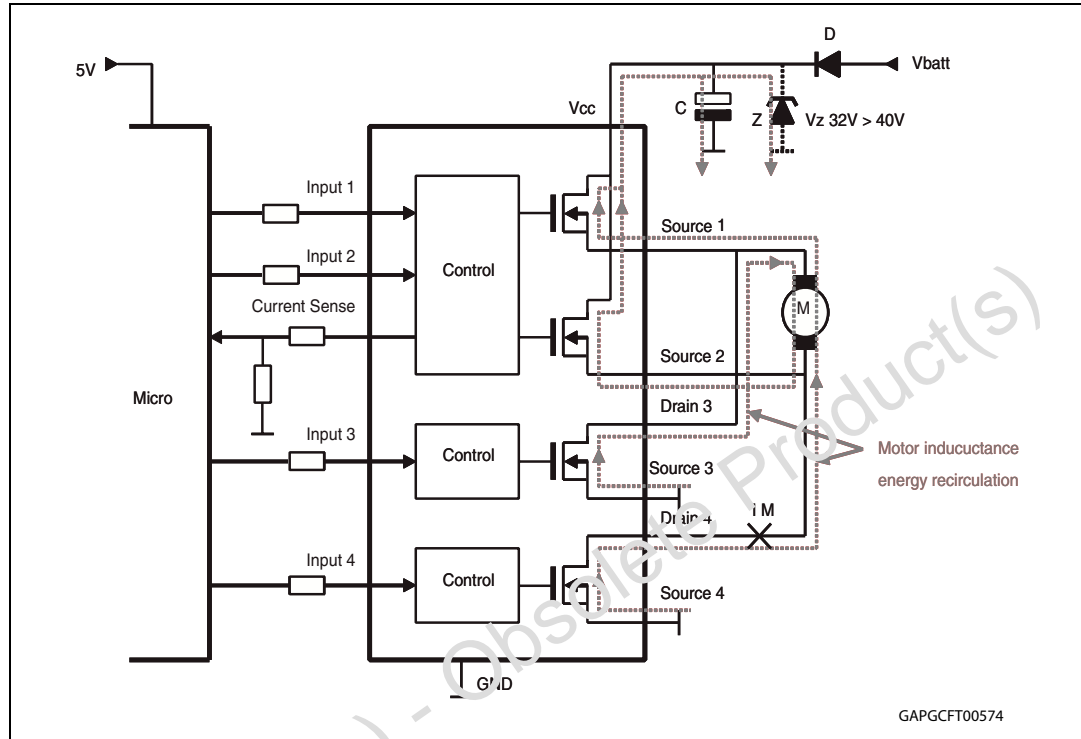
**Figure 32. Current limit vs junction temperature**



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## 4 Application information

Figure 33. Typical application schematic



**Note:** Mostly motor bridge drivers use a reverse battery protection diode (D) inside supply rail. This diode prevents a reverse current flow back to Vbatt in case the bridge gets disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (Vcc), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50µF per 1A load current is recommended. In alternative, also a Zener protection (Z) is suitable. Even if a reverse polarity diode is not present, it is recommended to use a capacitor or zener at Vcc because a similar problem appears in case supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while motor is operating.

Figure 34. Recommended motor operation

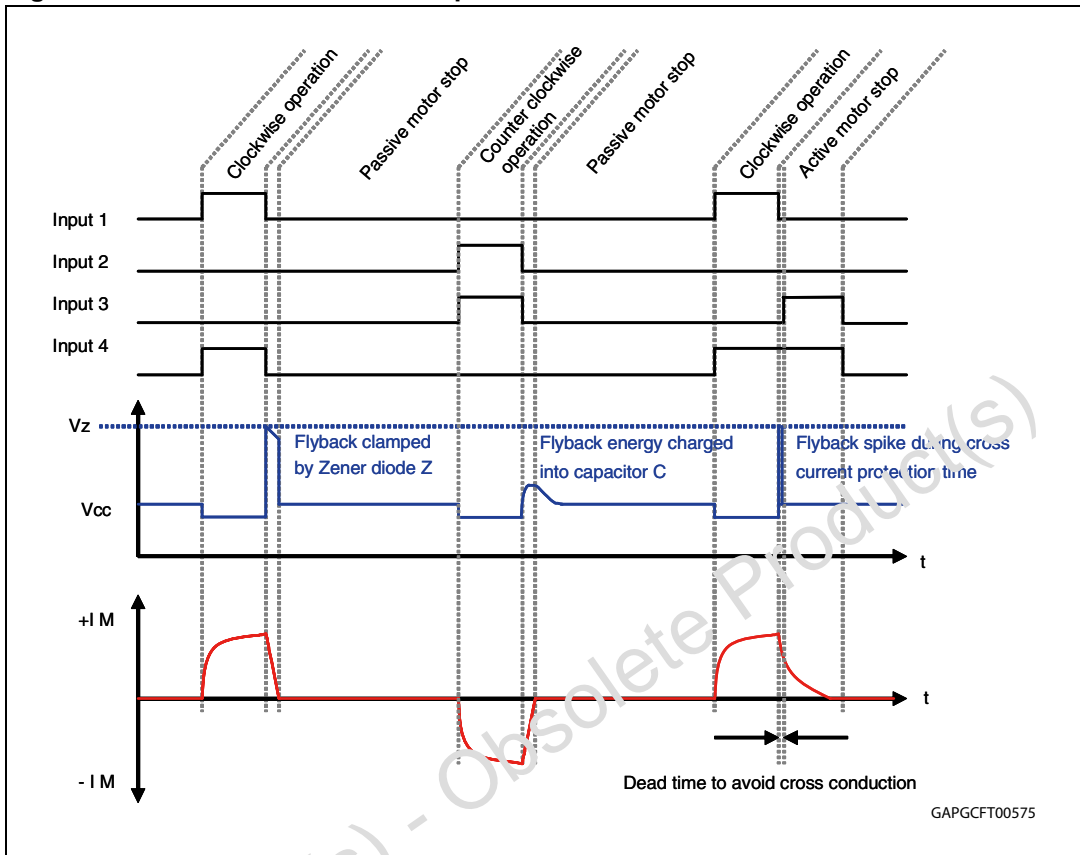
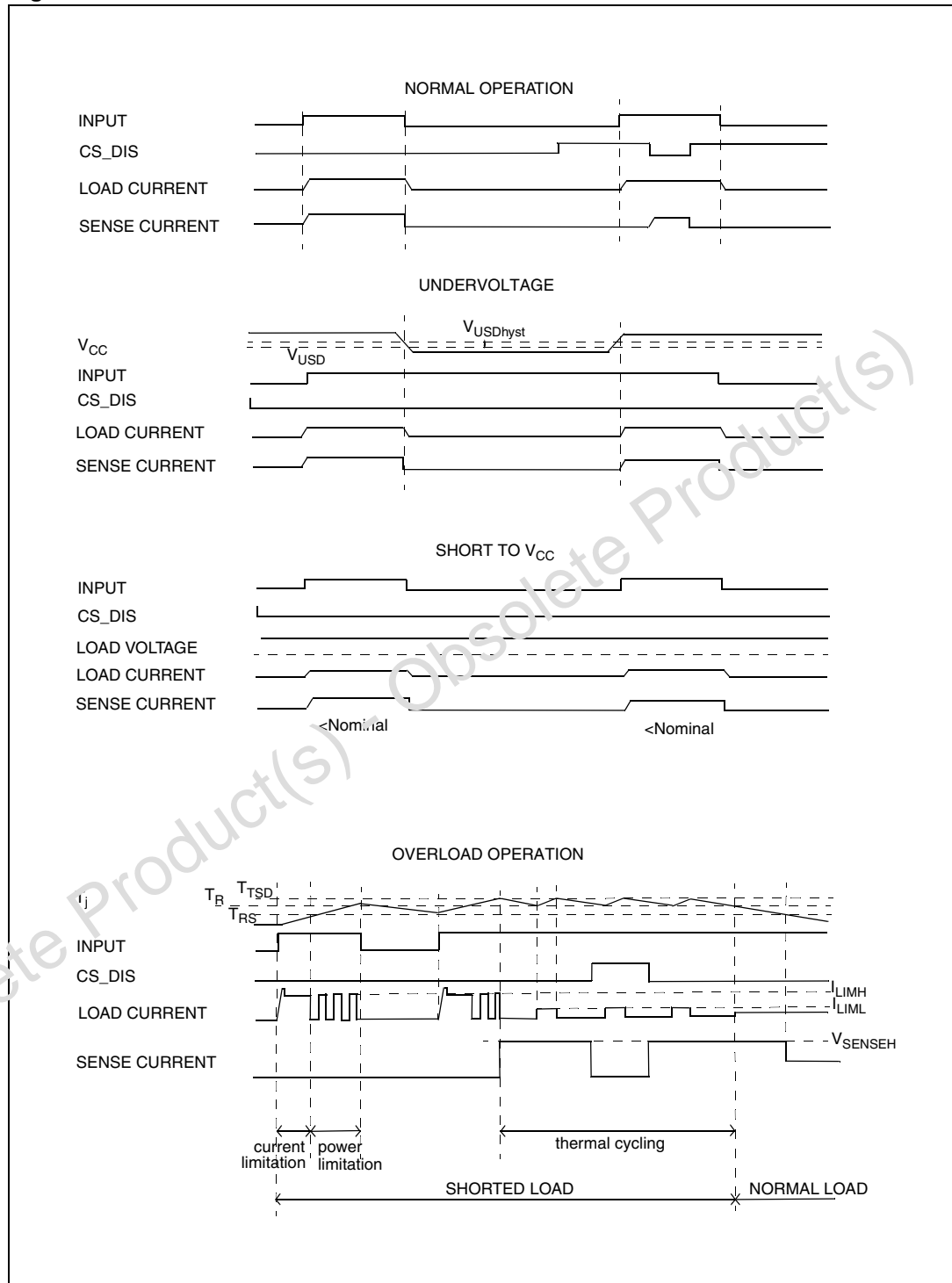
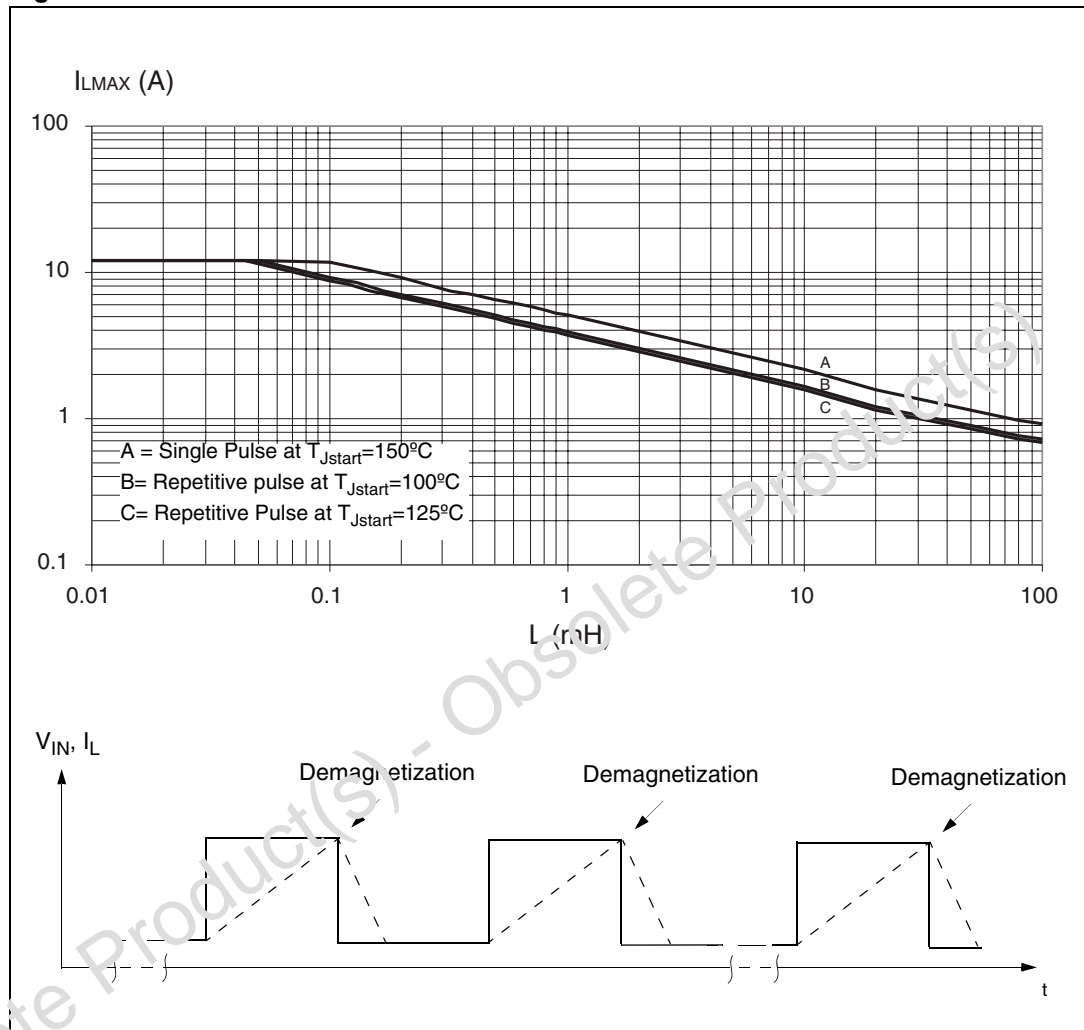


Figure 35. Waveforms



### 4.1 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 36. Maximum turn off current versus load inductance



Note: Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

## 5 Package and thermal data

### 5.1 SO-28 thermal data

Figure 37. SO-28 PC board

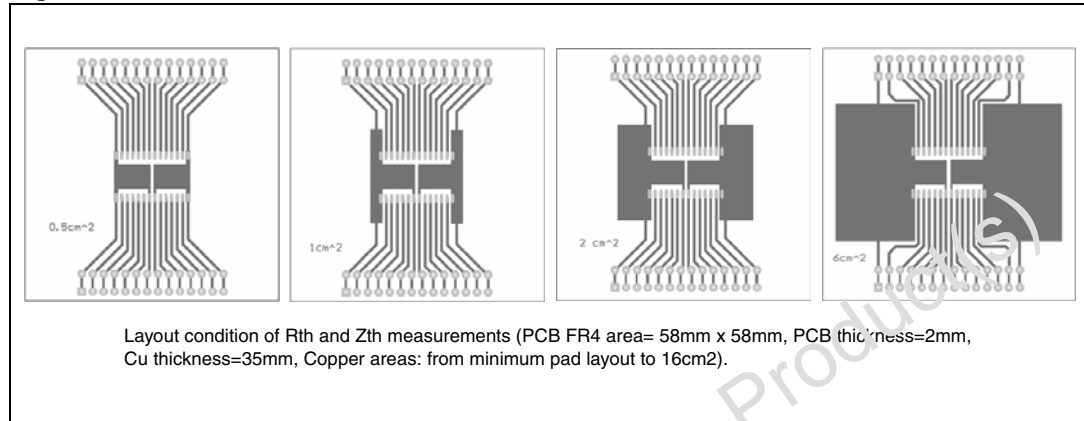


Figure 38. Chipset configuration

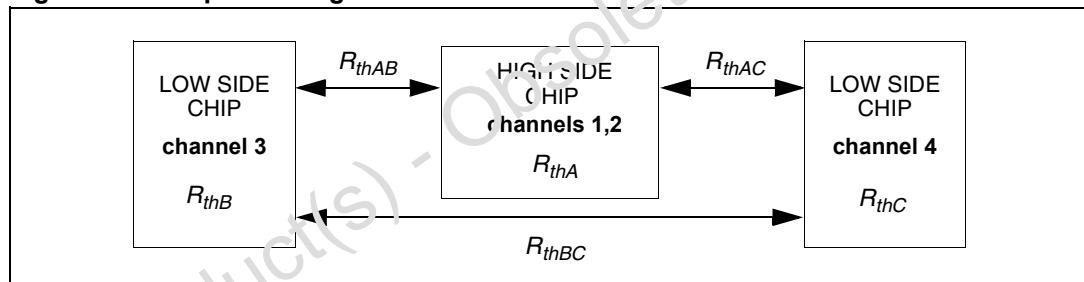
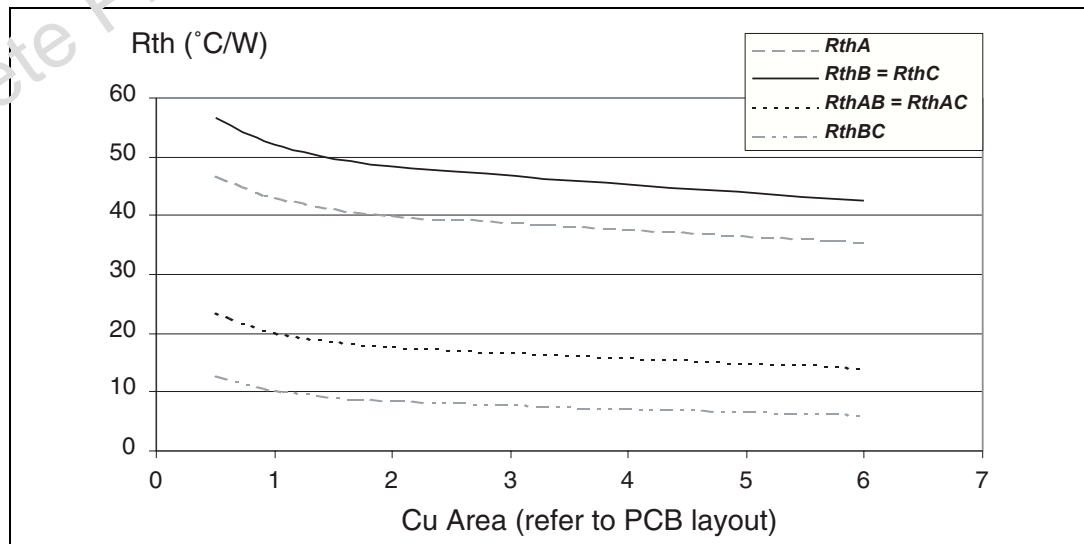


Figure 39. Auto and mutual  $R_{thj-amb}$  vs PCB copper area in open box free air condition<sup>(a)</sup>



**Table 17. Thermal calculations in clockwise and anti-clockwise operation in steady-state mode**

HS <sub>1</sub>	HS <sub>2</sub>	LS <sub>3</sub>	LS <sub>4</sub>	T <sub>jHS12</sub>	T <sub>jLS3</sub>	T <sub>jLS4</sub>
ON	OFF	OFF	ON	$P_{dHS1} \times R_{thHS} + P_{dLS4} \times R_{thHSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHS2} \times R_{thHS} + P_{dLS3} \times R_{thHSLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLSLS} + T_{amb}$

**Table 18. Thermal resistances definitions<sup>(1)</sup>**

$R_{thHS} = R_{thHS1} = R_{thHS2}$	High-side chip thermal resistance junction to ambient (HS <sub>1</sub> or HS <sub>2</sub> in ON state)
$R_{thLS} = R_{thLS3} = R_{thLS4}$	Low-side chip thermal resistance junction to ambient
$R_{thHSLS} = R_{thHS1LS4} = R_{thHS2LS3}$	Mutual thermal resistance junction to ambient between high-side and low-side chips
$R_{thLSLS} = R_{thLS3LS4}$	Mutual thermal resistance junction to ambient between low-side chips

1. values dependent on PCB heatsink area

**Table 19. Single pulse thermal impedance definitions<sup>(1)</sup>**

$Z_{thHS}$	High-side chip thermal impedance junction to ambient
$Z_{thLS} = Z_{thLS3} = Z_{thLS4}$	Low-side chip thermal impedance junction to ambient
$Z_{thHSLS} = Z_{thHS12LS3} = Z_{thHS2LS4}$	Mutual thermal impedance junction to ambient between high-side and low-side chips
$Z_{thLSLS} = Z_{thLS3LS4}$	Mutual thermal impedance junction to ambient between low-side chips

1. values dependent on PCB heatsink area

**Table 20. Thermal calculations in transient mode<sup>(1)</sup>**

T <sub>jHS12</sub>	$Z_{thHS} \times P_{dHS12} + Z_{thHSLS} \times (P_{dLS3} + P_{dLS4}) + T_{amb}$
T <sub>jLS3</sub>	$Z_{thHSLS} \times P_{dHS12} + Z_{thLS} \times P_{dLS3} + Z_{thLSLS} \times P_{dLS4} + T_{amb}$
T <sub>jLS4</sub>	$Z_{thHSLS} \times P_{dHS12} + Z_{thLSLS} \times P_{dLS3} + Z_{thLS} \times P_{dLS4} + T_{amb}$

1. Calculation is valid in any dynamic operating condition. Pd values set by user.

a. See [Figure 38](#). For more detailed information see [Table 17](#) and [Table 18](#).



Figure 40. SO-28 HSD thermal impedance junction ambient single pulse

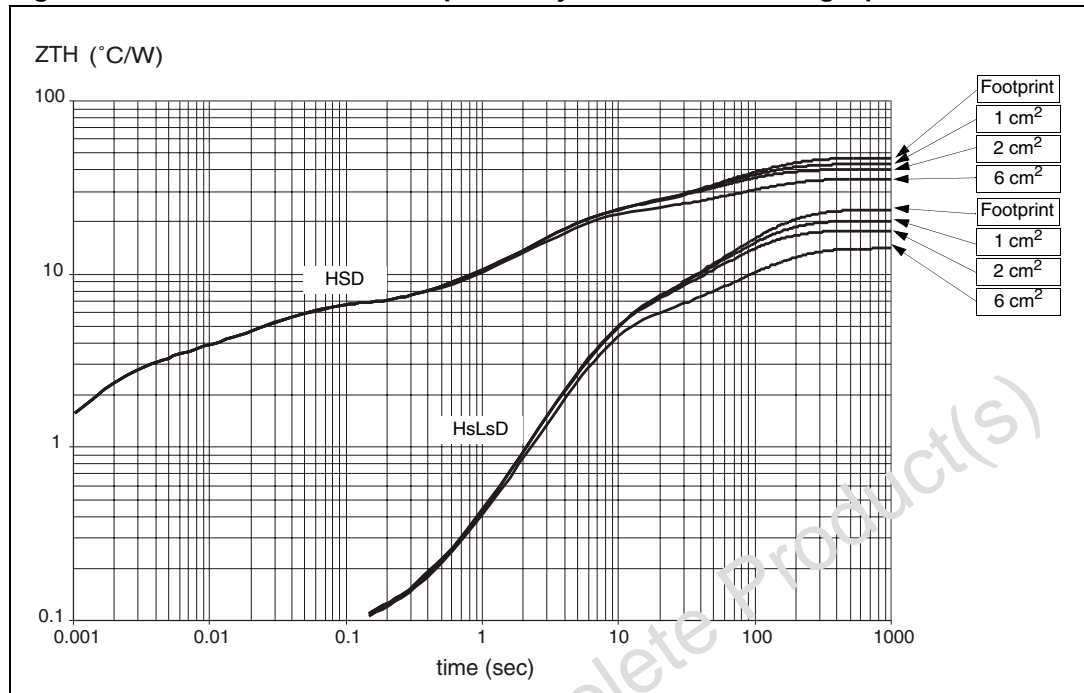
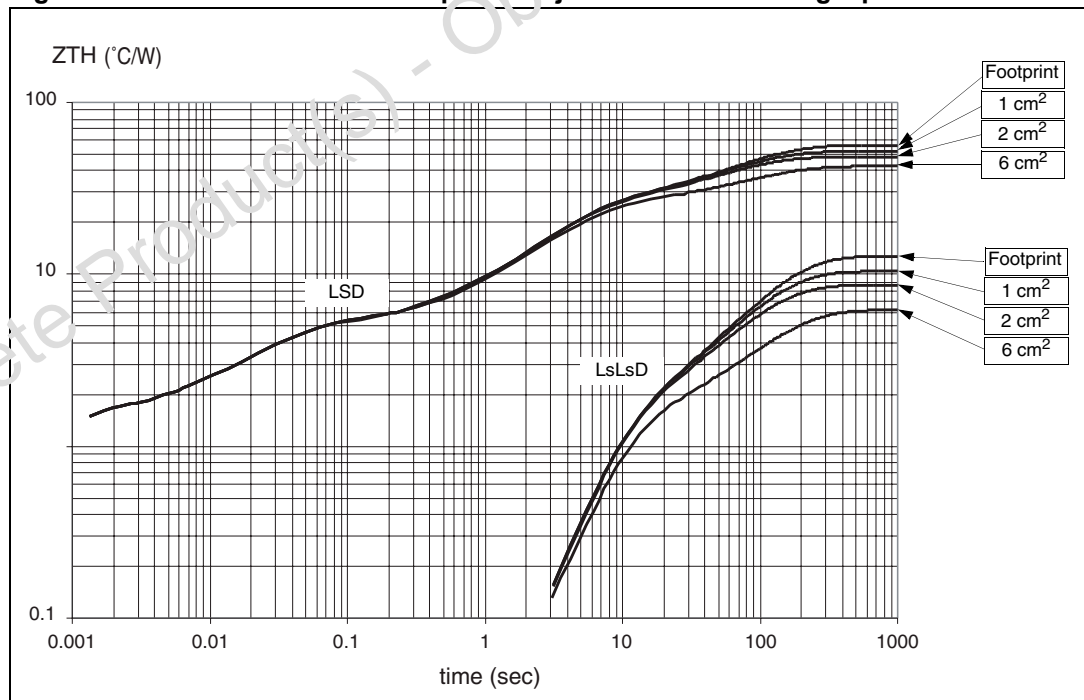


Figure 41. SO-28 LSD thermal impedance junction ambient single pulse

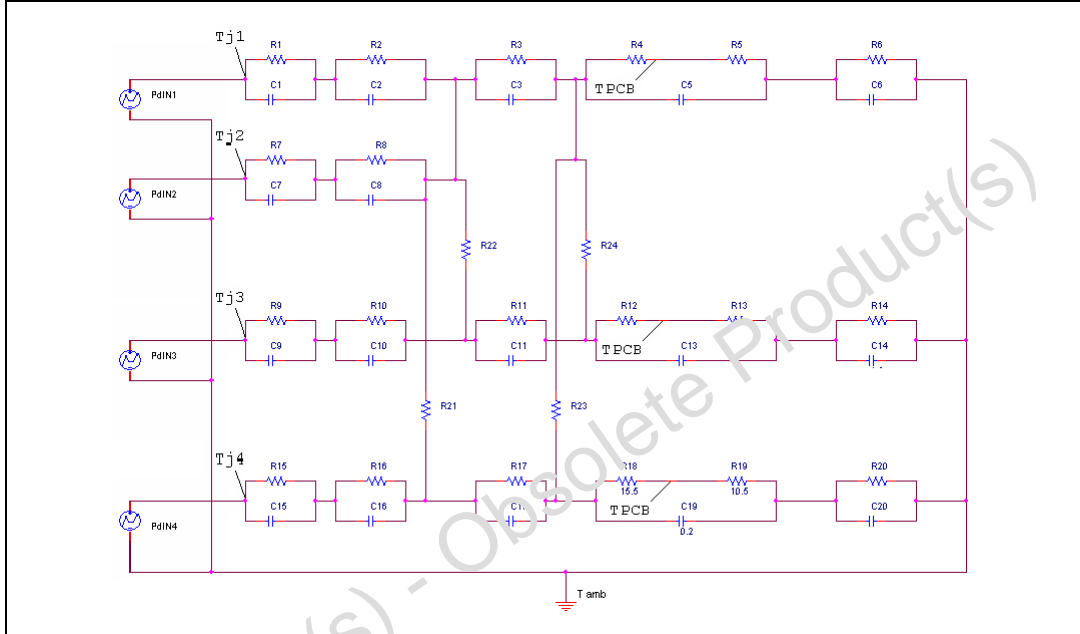


**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Figure 42. Thermal fitting model of an H-Bridge in SO-28**



**Table 21. Thermal parameters<sup>(1)</sup>**

Area/island (cm <sup>2</sup> )	Footprint	1	2	6
R1 (°C/W)	1			
R2 (°C/W)	1.8			
R3 (°C/W)	3.5			
R4 (°C/W)	13.5			
R5 (°C/W)	10.5			
R6 (°C/W)	62.28	52.28	44.28	32.28
R7 (°C/W)	1			
R8 (°C/W)	1.8			
R9 (°C/W)	0.24			
R10 (°C/W)	1.2			
R11 (°C/W)	3.5			
R12 (°C/W)	15.2			
R13 (°C/W)	10.5			
R14 (°C/W)	62.28	52.28	44.28	32.28

Table 21. Thermal parameters<sup>(1)</sup> (continued)

Area/island (cm <sup>2</sup> )	Footprint	1	2	6
R15 (°C/W)	0.24			
R16 (°C/W)	1.2			
R17 (°C/W)	3.5			
R18 (°C/W)	15.5			
R19 (°C/W)	10.5			
R20 (°C/W)	62.28	52.28	44.28	32.28
R21 (°C/W)	150			
R22 (°C/W)	150			
R23 (°C/W)	150			
R24 (°C/W)	150	52.28	44.28	32.28
C1 (W·s/°C)	0.0008			
C2 (W·s/°C)	0.001			
C3 (W·s/°C)	0.008			
C5 (W·s/°C)	0.2			
C6 (W·s/°C)	1.6	1.61	1.7	3.25
C7 (W·s/°C)	0.0008			
C8 (W·s/°C)	0.001			
C9 (W·s/°C)	0.00015			
C10 (W·s/°C)	0.0005			
C11 (W·s/°C)	0.008			
C13 (W·s/°C)	0.2			
C14 (W·s/°C)	1.6	1.61	1.7	3.25
C15 (W·s/°C)	0.00015			
C16 (W·s/°C)	0.0005			
C17 (W·s/°C)	0.008			
C19 (W·s/°C)	0.2			
C20 (W·s/°C)	1.6	1.61	1.7	3.25

1. A blank space means that the value is the same as the previous one

## 6 Package and packing information

### 6.1 ECOPACK®

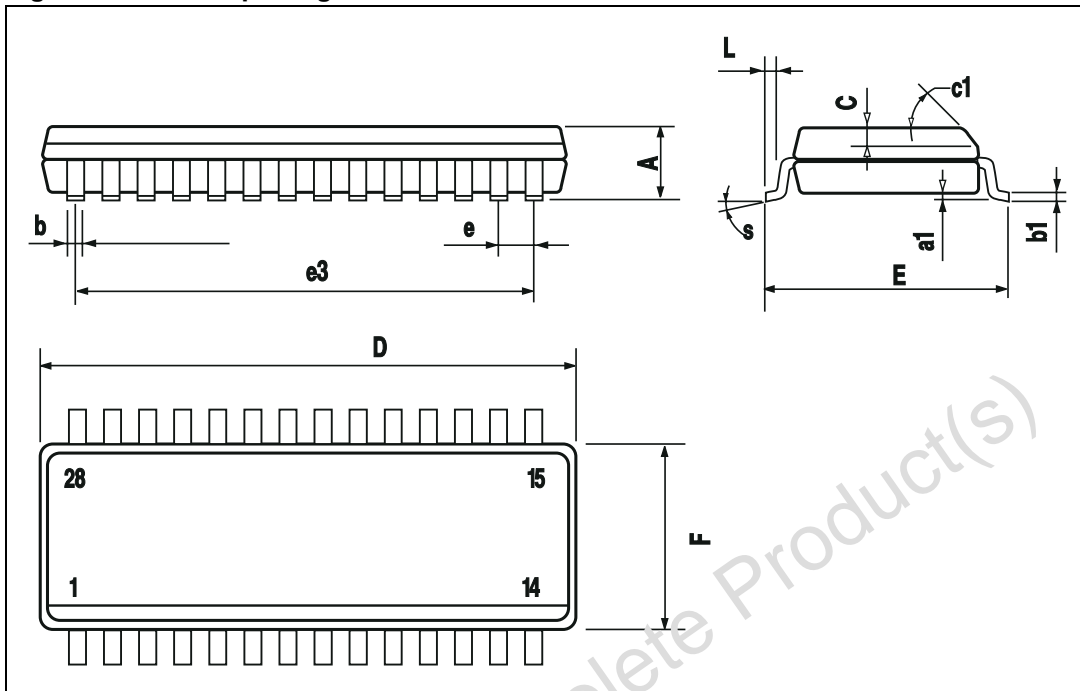
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 6.2 SO-28 package information

Table 22. SO-28 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1	45° (typ.)		
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S	8° (max.)		

Figure 43. SO-28 package dimensions



Obsolete Product(s) - Obsolete Product(s)

### 6.3 SO-28 packing information

Figure 44. SO-28 tube shipment (no suffix)

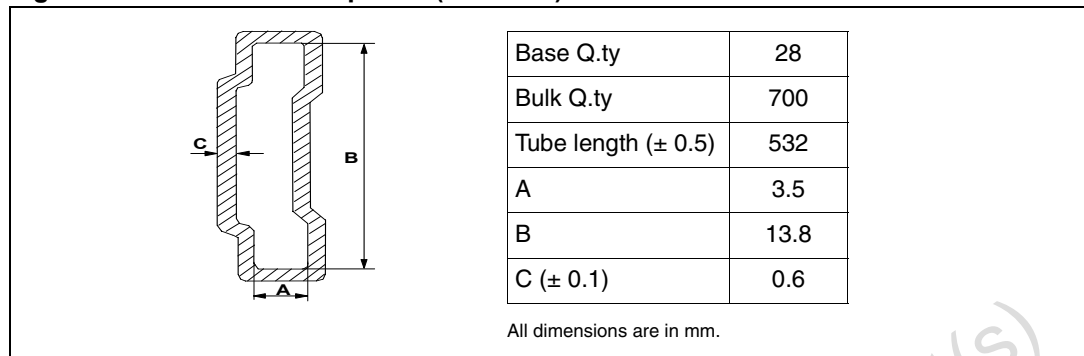
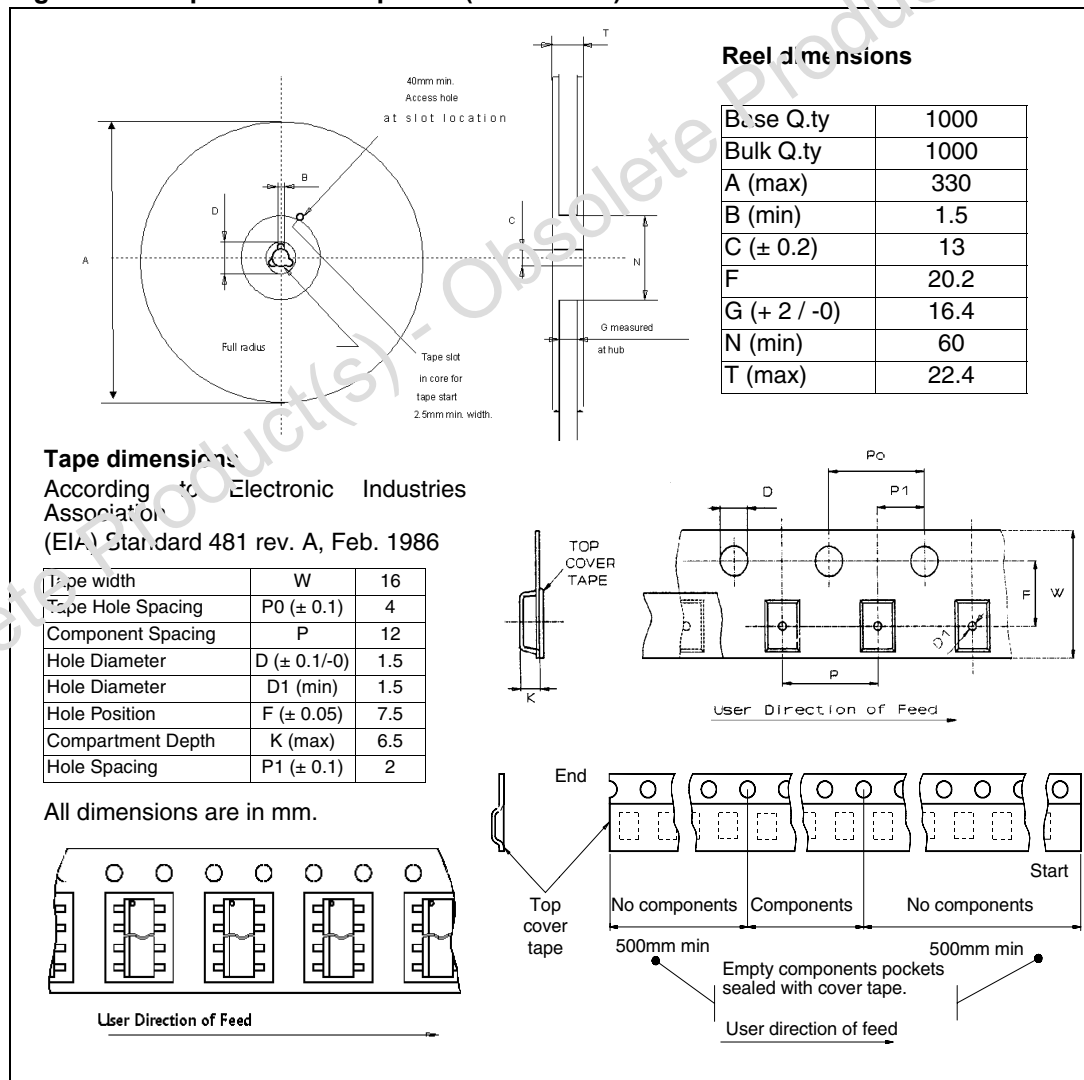


Figure 45. Tape and reel shipment (suffix "TR")



## 7 Order codes

**Table 23. Device summary**

Package	Order codes	
	Tube	Tape and reel
SO-28	VN5770AK-E	VN5770AKTR-E

Obsolete Product(s) - Obsolete Product(s)

## 8 Revision history

**Table 24. Document revision history**

Date	Revision	Changes
June-2006	1	Initial release.
15-Feb-2007	2	<p>Reformatted.</p> <p><i>Table 5: Power section</i> updated.</p> <p><i>Table 6: Switching (VCC = 13V)</i> updated.</p> <p><i>Table 9: Current sense (8V&lt;VCC&lt;16V)</i> updated.</p> <p><i>Table 12: On</i> updated.</p> <p><i>Table 14: Switching (T<sub>j</sub> = 25°C, unless otherwise specified)</i> updated.</p> <p>Characteristic curves for high-side and low-side switches added.</p> <p><i>Figure 38: Chipset configuration</i> updated.</p> <p><i>Figure 39: Auto and mutual R<sub>thj-amb</sub> vs PCB copper area in open box free air condition</i> added.</p> <p><i>Figure 40: SO-28 HSD thermal impedance junction ambient single pulse, Figure 41: SO-28 LSD thermal impedance junction ambient single pulse and Figure 42: Thermal fitting model of an H-Bridge in SO-28</i> added.</p> <p><i>Figure 21: Thermal parameters</i> added.</p> <p>High-side and low-side characteristic curves added.</p> <p><i>Figure 35: Waveforms</i> added.</p> <p><i>Section 4.1: Maximum demagnetization energy (V<sub>CC</sub> = 13.5V)</i> added.</p> <p><i>Figure 33: Typical application schematic</i> added.</p>
02-Jul-2007	3	<i>Table 9: Current sense (8V&lt;VCC&lt;16V)</i> updated
24-Jul-2007	4	<i>Table 9: Current sense (8V&lt;VCC&lt;16V)</i> - K <sub>0</sub> , K <sub>1</sub> and K <sub>3</sub> values modified
04-Jan-2012	5	<i>Table 9: Current sense (8V&lt;VCC&lt;16V)</i> - K <sub>0</sub> values modified
12-Feb-2012	6	Update <i>Figure 2: Configuration diagram (top view)</i> and <i>Figure 33: Typical application schematic</i>



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