

Function Select Table

S ₂	S ₁	S ₀	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Pin Descriptions

Pin Names	Description
CP	Clock Pulse Input
$\overline{\text{CEP}}$	Count Enable Parallel Input (Active LOW)
$\overline{\text{D}_0/\text{CET}}$	Serial Data Input/Count Enable
	Trickle Input (Active LOW)
S ₀ -S ₂	Select Inputs
MR	Master Reset Input
P ₀ -P ₃	Preset Inputs
D ₃	Serial Data Input
TC	Terminal Count Output
Q ₀ -Q ₃	Data Outputs
$\overline{\text{Q}_0}$ - $\overline{\text{Q}_3}$	Complementary Data Outputs

Truth Table

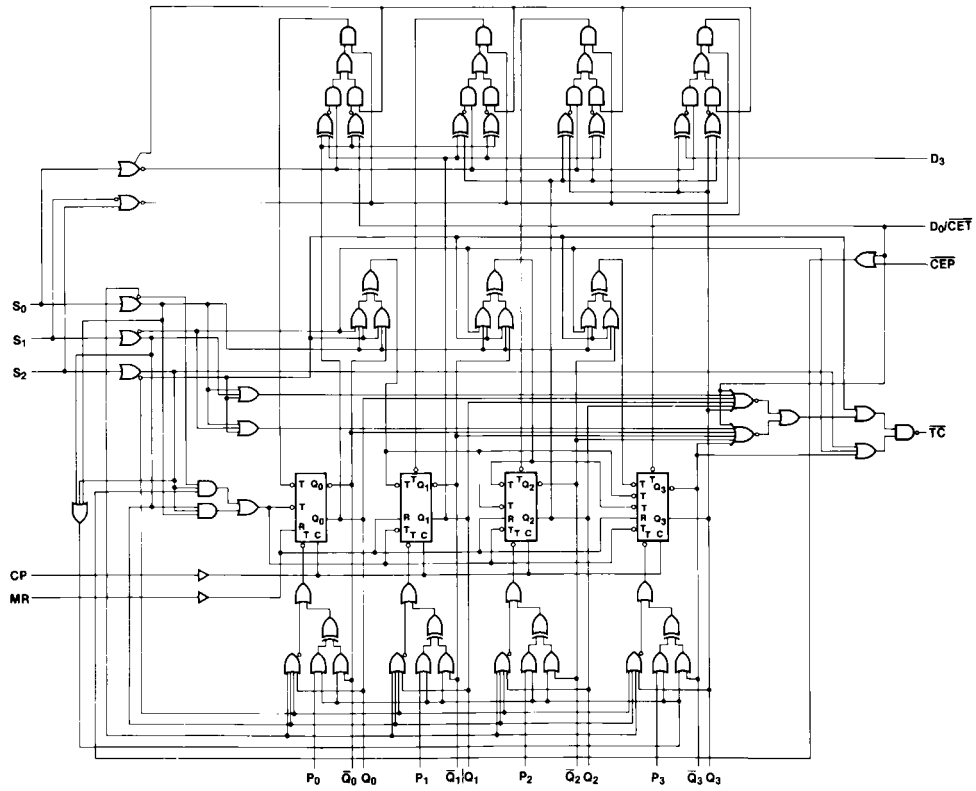
Q₀ = LSB

Inputs								Outputs						Mode
MR	S ₂	S ₁	S ₀	$\overline{\text{CEP}}$	$\overline{\text{D}_0/\text{CET}}$	D ₃	CP	Q ₃	Q ₂	Q ₁	Q ₀	$\overline{\text{TC}}$		
L	L	L	L	X	X	X	↘	P ₃	P ₂	P ₁	P ₀	L	Preset (Parallel Load)	
L	L	L	H	X	X	X	↘	$\overline{\text{Q}_3}$	$\overline{\text{Q}_2}$	$\overline{\text{Q}_1}$	$\overline{\text{Q}_0}$	L	Invert	
L	L	H	L	X	X	X	↘	D ₃	Q ₃	Q ₂	Q ₁	D ₃	Shift to LSB	
L	L	H	H	X	X	X	↘	Q ₂	Q ₁	Q ₀	D ₀	Q ₃ (Note 1)	Shift to MSB	
L	H	L	L	L	L	X	↘	(Q ₀₋₃) minus 1				1	Count Down	
L	H	L	L	H	L	X	X	Q ₃	Q ₂	Q ₁	Q ₀	1	Count Down with $\overline{\text{CEP}}$ not active	
L	H	L	L	X	H	X	X	Q ₃	Q ₂	Q ₁	Q ₀	H	Count Down with $\overline{\text{CET}}$ not active	
L	H	L	H	X	X	X	↘	L	L	L	L	H	Clear	
L	H	H	L	L	L	X	↘	(Q ₀₋₃) plus 1				2	Count Up	
L	H	H	L	H	L	X	X	Q ₃	Q ₂	Q ₁	Q ₀	2	Count Up with $\overline{\text{CEP}}$ not active	
L	H	H	L	X	H	X	X	Q ₃	Q ₂	Q ₁	Q ₀	H	Count Up with $\overline{\text{CET}}$ not active	
L	H	H	H	X	X	X	X	Q ₃	Q ₂	Q ₁	Q ₀	H	Hold	
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset	
H	L	L	H	X	X	X	X	L	L	L	L	L		
H	L	H	L	X	X	X	X	L	L	L	L	L		
H	L	H	H	X	X	X	X	L	L	L	L	L		
H	H	L	L	X	L	X	X	L	L	L	L	L		
H	H	L	L	X	H	X	X	L	L	L	L	H		
H	H	L	H	X	X	X	X	L	L	L	L	H		
H	H	H	L	X	X	X	X	L	L	L	L	H		
H	H	H	H	X	X	X	X	L	L	L	L	H		
H	H	H	H	X	X	X	X	L	L	L	L	H		

1 = L if Q₀-Q₃ = LLLL
 H if Q₀-Q₃ ≠ LLLL
 2 = L if Q₀-Q₃ = HHHH
 H if Q₀-Q₃ ≠ HHHH
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↘ = LOW-to-HIGH Transition
Note 1: Before the clock, $\overline{\text{TC}}$ is Q₃
 After the clock, $\overline{\text{TC}}$ is Q₂

Logic Diagram

100336



Absolute Maximum Ratings (Note 2)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 3)	$\geq 2000V$

Recommended Operating Conditions

Case Temperature (T_C)	Commercial	0°C to +85°C
	Industrial	-40°C to +85°C
Supply Voltage (V_{EE})		-5.7V to -4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version**DC Electrical Characteristics** (Note 4)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50 Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50 Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610	mV		
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL} (Min)$	
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH} (Max)$	
I_{EE}	Power Supply Current	-165		-80		Inputs Open	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued) DIP AC Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Shift Frequency	300		300		300		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, \overline{Q}_n	1.00	2.00	1.00	2.00	1.00	2.00	ns	Figures 1, 3 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay CP to \overline{TC} (Shift)	2.10	3.50	2.10	3.50	2.10	3.70	ns	Figures 1, 7, 8 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay CP to \overline{TC} (Count)	2.40	4.40	2.40	4.40	2.60	4.70	ns	Figures 1, 9 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, \overline{Q}_n	1.40	2.50	1.40	2.50	1.50	2.60	ns	Figures 1, 4 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay MR to \overline{TC} (Count)	2.80	5.10	2.90	5.20	3.10	5.50	ns	Figures 1, 12 (Note 5)
t_{PHL}	Propagation Delay MR to \overline{TC} (Shift)	2.40	4.00	2.40	4.00	2.50	4.10	ns	Figures 1, 10, 11 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay D_0/\overline{CET} to \overline{TC}	1.80	3.10	1.80	3.10	1.90	3.30	ns	Figures 1, 5 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay S_n to \overline{TC}	1.90	4.10	1.90	4.10	2.10	4.40	ns	(Note 5)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 3
t_S	Setup Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n MR (Release Time)	1.00 1.50 1.30 1.40 3.40 2.60		1.00 1.50 1.30 1.40 3.40 2.60		1.00 1.50 1.30 1.40 3.40 2.60		ns	Figures 6, 4
t_H	Hold Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n	0.40 0.30 0.30 0.20 0.10		0.40 0.30 0.30 0.20 0.10		0.40 0.30 0.30 0.20 0.10		ns	Figure 6
$t_{PW(H)}$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3, 4

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

SOIC and PLCC AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Shift Frequency	350		350		350		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n , \overline{Q}_n	1.00	1.80	1.00	1.80	1.00	1.80	ns	Figures 1, 2 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay CP to \overline{TC} (Shift)	2.10	3.30	2.10	3.30	2.10	3.50	ns	Figures 1, 7, 8 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay CP to \overline{TC} (Count)	2.40	4.20	2.40	4.20	2.60	4.50	ns	Figures 1, 9 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n , \overline{Q}_n	1.40	2.30	1.40	2.30	1.50	2.40	ns	Figures 1, 4 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay MR to \overline{TC} (Count)	2.80	4.90	2.90	5.00	3.10	5.30	ns	Figures 1, 12 (Note 6)
t_{PHL}	Propagation Delay MR to \overline{TC} (Shift)	2.40	3.80	2.40	3.80	2.50	3.90	ns	Figures 1, 10, 11 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay D_0/\overline{CET} to \overline{TC}	1.80	2.90	1.80	2.90	1.90	3.10	ns	Figures 1, 5 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay S_n to \overline{TC}	1.90	3.90	1.90	3.90	2.10	4.20	ns	(Note 6)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	Figures 1, 3
t_S	Setup Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n MR (Release Time)	0.90 1.40 1.20 1.30 3.30 2.50		0.90 1.40 1.20 1.30 3.30 2.50		0.90 1.40 1.20 1.30 3.30 2.50		ns	Figures 4, 6
t_H	Hold Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n	0.30 0.20 0.20 0.10 0.00		0.30 0.20 0.20 0.10 0.00		0.30 0.20 0.20 0.10 0.00		ns	Figure 6
$t_{PW(H)}$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3, 4
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PLCC Only (Note 7)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PLCC Only (Note 7)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		230		230		230	ps	PLCC Only (Note 7)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		245		245		245	ps	PLCC Only (Note 7)

Note 6: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Note 7: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design

Industrial Version

PLCC DC Electrical Characteristics (Note 8)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH} (Max)$	Loading with 50Ω to $-2.0V$
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620	mV	or $V_{IL} (Min)$	
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH} (Min)$	Loading with 50Ω to $-2.0V$
V_{OLC}	Output LOW Voltage		-1565		-1610	mV	or $V_{IL} (Max)$	
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL} (Min)$	
I_{IH}	Input HIGH Current		240		240	μA	$V_{IN} = V_{IH} (Max)$	
I_{EE}	Power Supply Current	-165	-75	-165	-80	mA	Inputs Open	

Note 8: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

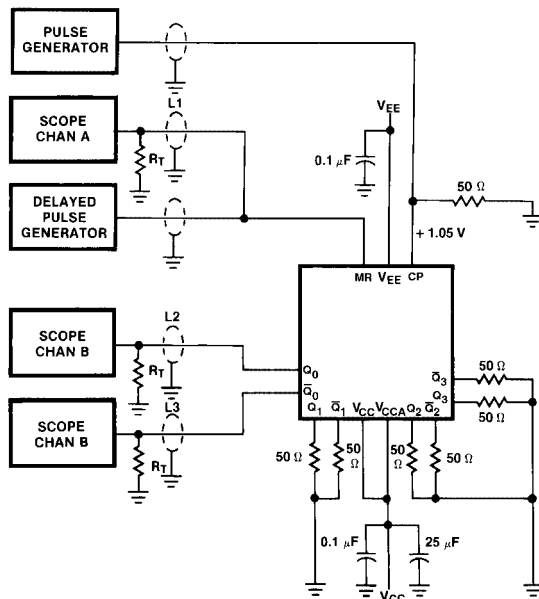
PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Shift Frequency	325		350		350		MHz	Figures 2, 3
t_{PLH}	Propagation Delay	1.00	1.80	1.00	1.80	1.00	1.80	ns	Figures 1, 3 (Note 9)
t_{PHL}	CP to Q_n , \overline{Q}_n								
t_{PLH}	Propagation Delay	2.00	3.30	2.10	3.30	2.10	3.50	ns	Figures 1, 7, 8 (Note 9)
t_{PHL}	CP to \overline{TC} (Shift)								
t_{PLH}	Propagation Delay	2.40	4.20	2.40	4.20	2.60	4.50	ns	Figures 1, 9 (Note 9)
t_{PHL}	CP to \overline{TC} (Count)								
t_{PLH}	Propagation Delay	1.40	2.30	1.40	2.30	1.50	2.40	ns	Figures 1, 4 (Note 9)
t_{PHL}	MR to Q_n , \overline{Q}_n								
t_{PLH}	Propagation Delay	2.80	4.90	2.90	5.00	3.10	5.30	ns	Figures 1, 12 (Note 9)
t_{PHL}	MR to \overline{TC} (Count)								
t_{PHL}	Propagation Delay	2.40	3.80	2.40	3.80	2.50	3.90	ns	Figures 1, 10, 11 (Note 9)
t_{PHL}	MR to \overline{TC} (Shift)								
t_{PLH}	Propagation Delay	1.70	2.90	1.80	2.90	1.90	3.10	ns	Figures 1, 5 (Note 9)
t_{PHL}	D_0/CET to \overline{TC}								
t_{PLH}	Propagation Delay	1.80	3.90	1.90	3.90	2.10	4.20	ns	Figures 1, 10, 11 (Note 9)
t_{PHL}	S_n to \overline{TC}								
t_{TLH}	Transition Time	0.20	1.90	0.35	1.10	0.35	1.10	ns	Figures 1, 3
t_{THL}	20% to 80%, 80% to 20%								
t_s	Setup Time							ns	Figure 6
	D_3	1.40		0.90		0.90			
	P_n	1.70		1.40		1.40			
	D_0/CET	1.80		1.20		1.20			
	\overline{CEP}	1.80		1.30		1.30			
	S_n	3.30		3.30		3.30			
	MR (Release Time)	2.60		2.50		2.50			
t_H	Hold Time							ns	Figure 6
	D_3	0.90		0.30		0.30			
	P_n	1.00		0.20		0.20			
	D_0/CET	0.70		0.20		0.20			
	\overline{CEP}	0.60		0.10		0.10			
	S_n	0.00		0.00		0.00			
$t_{PW(H)}$	Pulse Width HIGH CP, MR	2.20		2.00		2.00		ns	Figures 3, 4

Note 9: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Test Circuitry



Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1, L2 and L3 = equal length 50Ω impedance lines

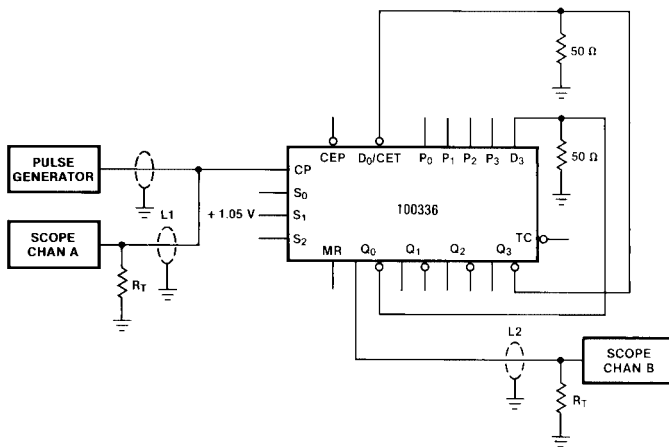
$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



Notes:

For shift right mode, +1.05V is applied at S_0 .

The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Switching Waveforms

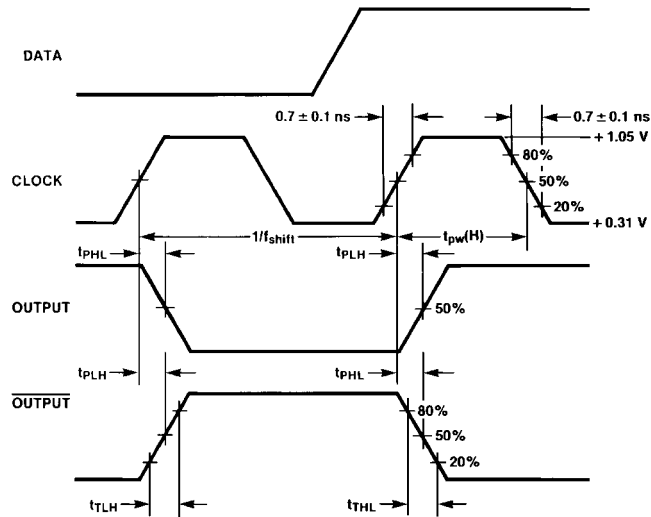


FIGURE 3. Propagation Delay (Clock) and Transition Times

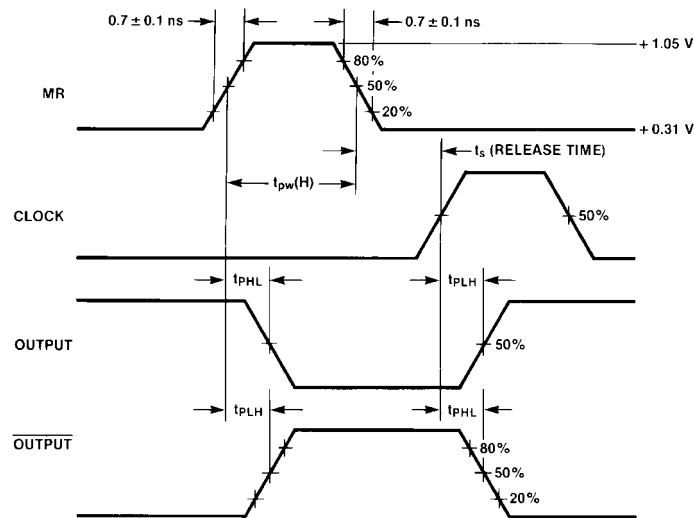


FIGURE 4. Propagation Delay (Reset)

Switching Waveforms (Continued)

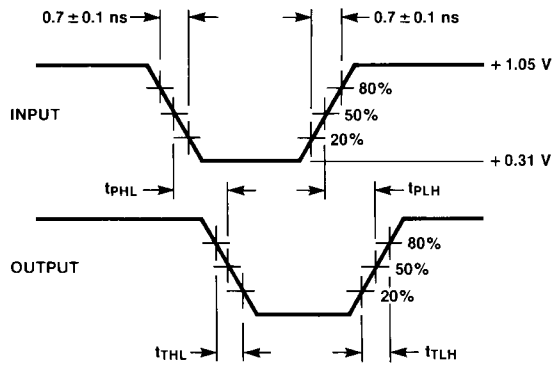
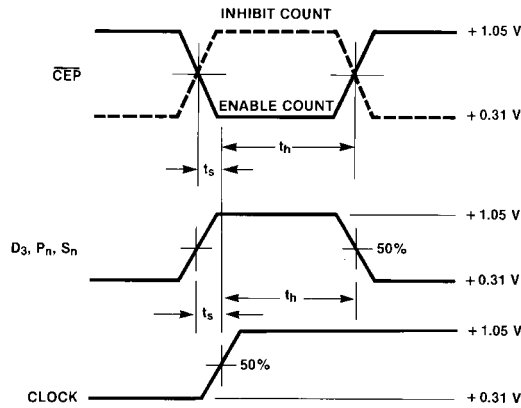


FIGURE 5. Propagation Delay (Serial Data, Selects)

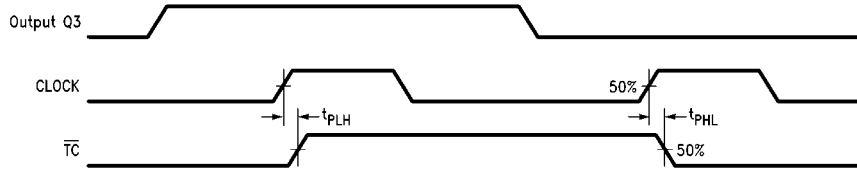


Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

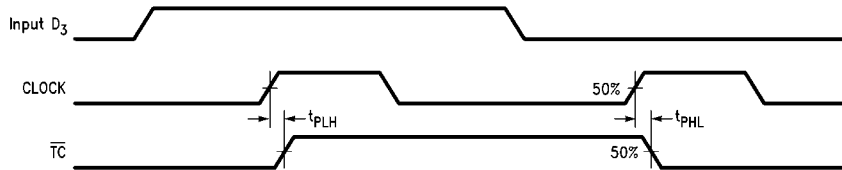
t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time



Note: Shift Right Mode; $S_0 = H, S_1 = H, S_2 = L$.

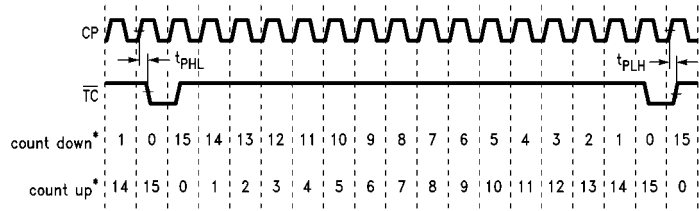
FIGURE 7. Propagation Delay, Clock to Terminal Count (Shift Right Mode)



Note: Shift Left Mode; $S_0 = L, S_1 = H, S_2 = L$.

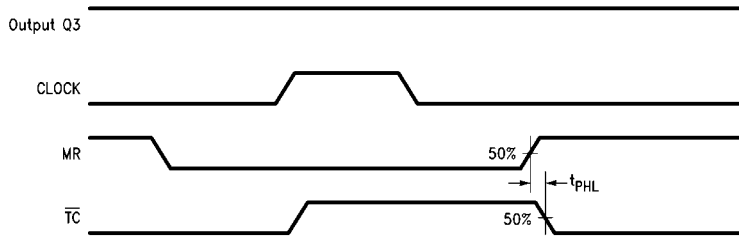
FIGURE 8. Propagation Delay, Clock to Terminal Count (Shift Left Mode)

Switching Waveforms (Continued)



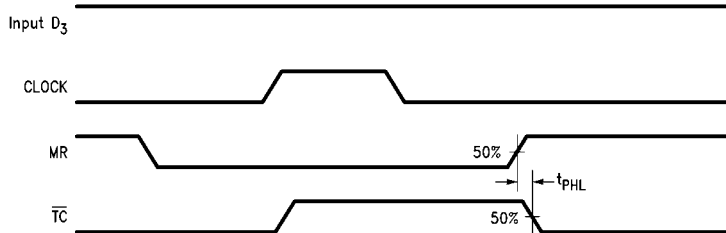
Note:
 *Decimal representation of binary outputs.
 Count Up: $S_0 = L, S_1 = H, S_2 = H$; Count Down: $S_0 = L, S_1 = L, S_2 = H$.
 Measurement taken at 50% point of waveform.

FIGURE 9. Propagation Delay, Clock to Terminal Count (Count Up and Count Down Modes)



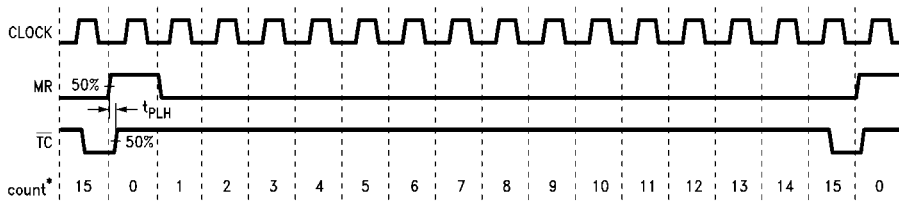
Note: Shift Right Mode; $S_0 = H, S_1 = H, S_2 = L$.

FIGURE 10. Propagation Delay, Master Reset to Terminal Count (Shift Right Mode)

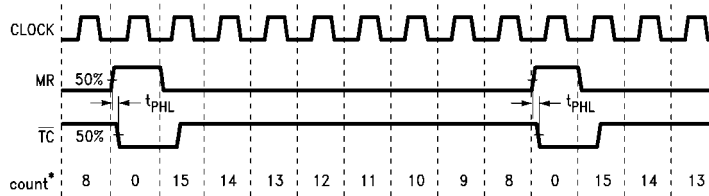


Note: Shift Left Mode; $S_0 = L, S_1 = H, S_2 = L$.

FIGURE 11. Propagation Delay, Master Reset to Terminal Count (Shift Left Mode)



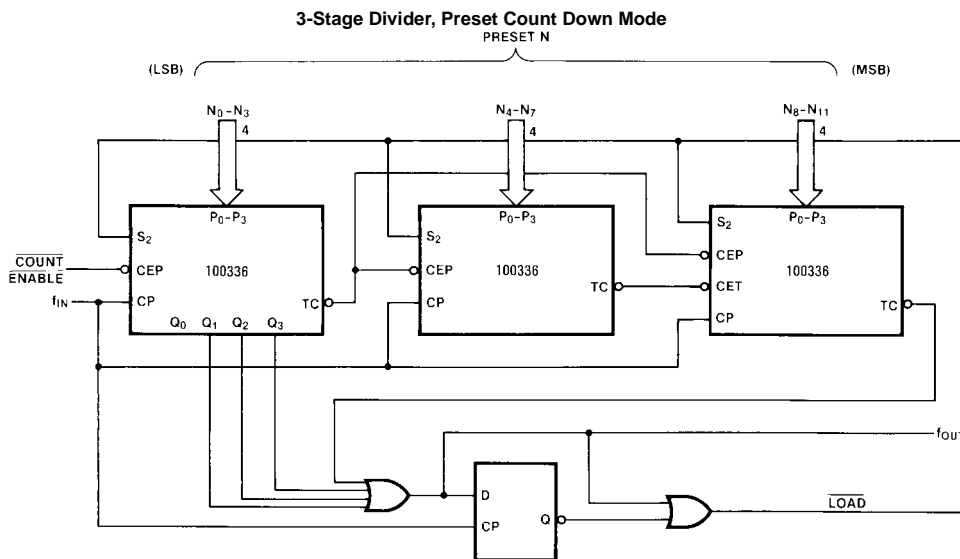
Note:
 *Decimal representation of binary outputs. Count Up Mode: $S_0 = L, S_1 = H, S_2 = H$.



Note:
 *Decimal representation of binary outputs. Count Down Mode: $S_0 = L, S_1 = L, S_2 = H$.

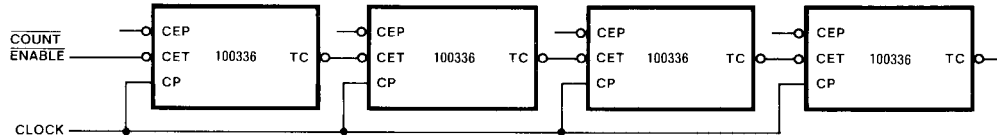
FIGURE 12. Propagation Delay, Master Reset to Terminal Count (Count Up and Count Down Modes)

Applications

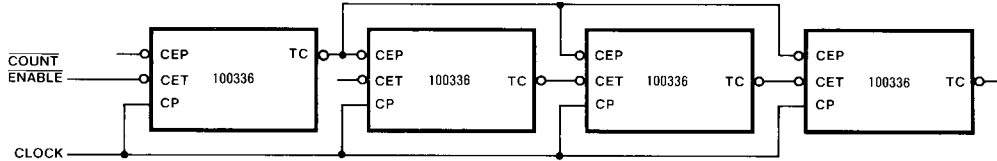


Note: If $S_0 = S_1 = S_2 = \text{LOW}$, then $T_C = \text{LOW}$

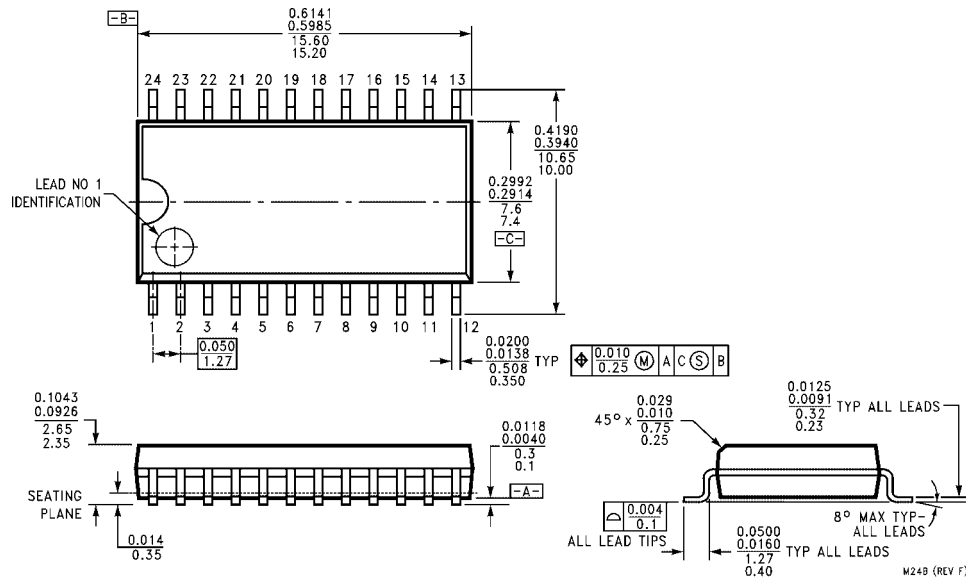
Slow Expansion Scheme



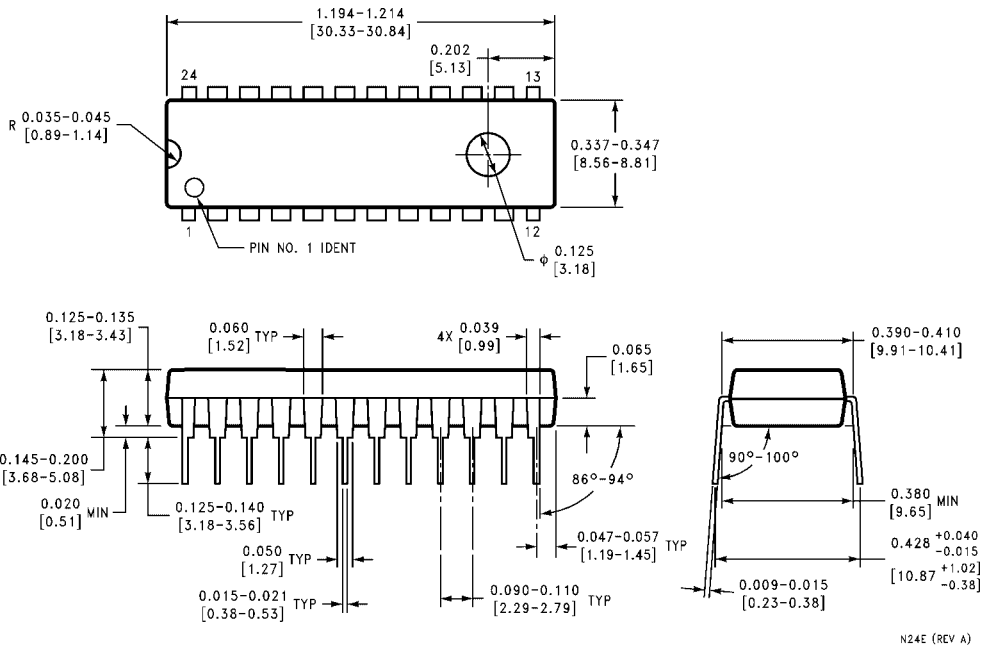
Fast Expansion Scheme



Physical Dimensions inches (millimeters) unless otherwise noted

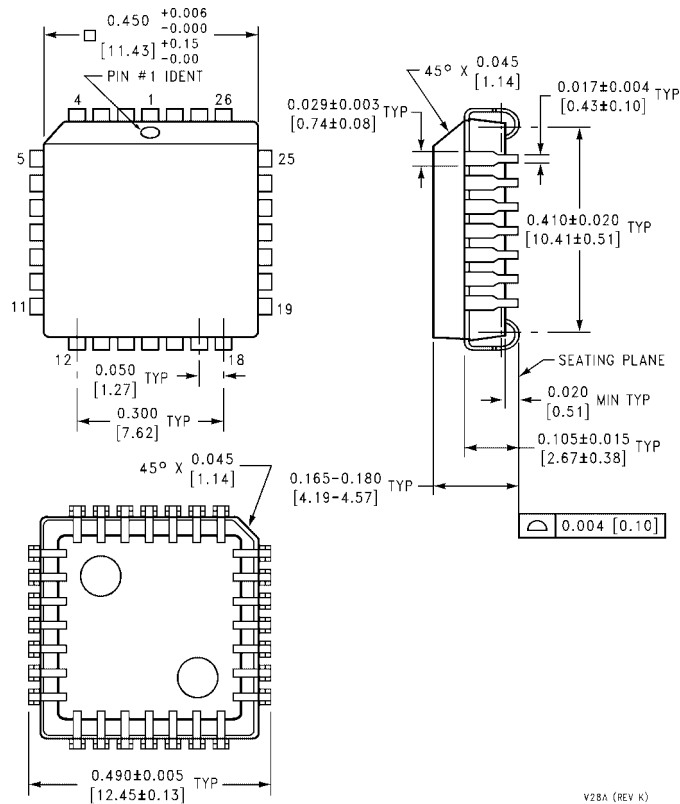


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[100336DC](#) [100336SCX](#) [100336QC](#) [100336QI](#) [100336SC](#) [100336PC](#) [100336QCX](#) [100336QIX](#)