Description

The ACPL-785J isolation amplifier is designed for current sensing in electronic motor drives. In a typical implementation, motor currents flow through an external resistor and the resulting analog voltage drop is sensed by the ACPL-785J. A larger analog output voltage is created on the other side of the ACPL-785J's optical isolation barrier. The output voltage is proportional to the motor current and can be connected directly to a single-supply A/D converter. A digital over-range output ($\overline{\text{FAULT}}$) and an analog rectified output (ABSVAL) are also provided. The wire OR-able over-range output ($\overline{\text{FAULT}}$) is useful for quick detection of short circuit conditions on any of the motor phases. The wire-OR-able rectified output (ABSVAL), simplifies measure-ment of motor load since it performs polyphase rectification. Since the common-mode voltage swings several hundred volts in tens of nanoseconds in modern electronic motor drives, the ACPL-785J was designed to ignore very high common-mode transient slew rates (10 kV/μs).

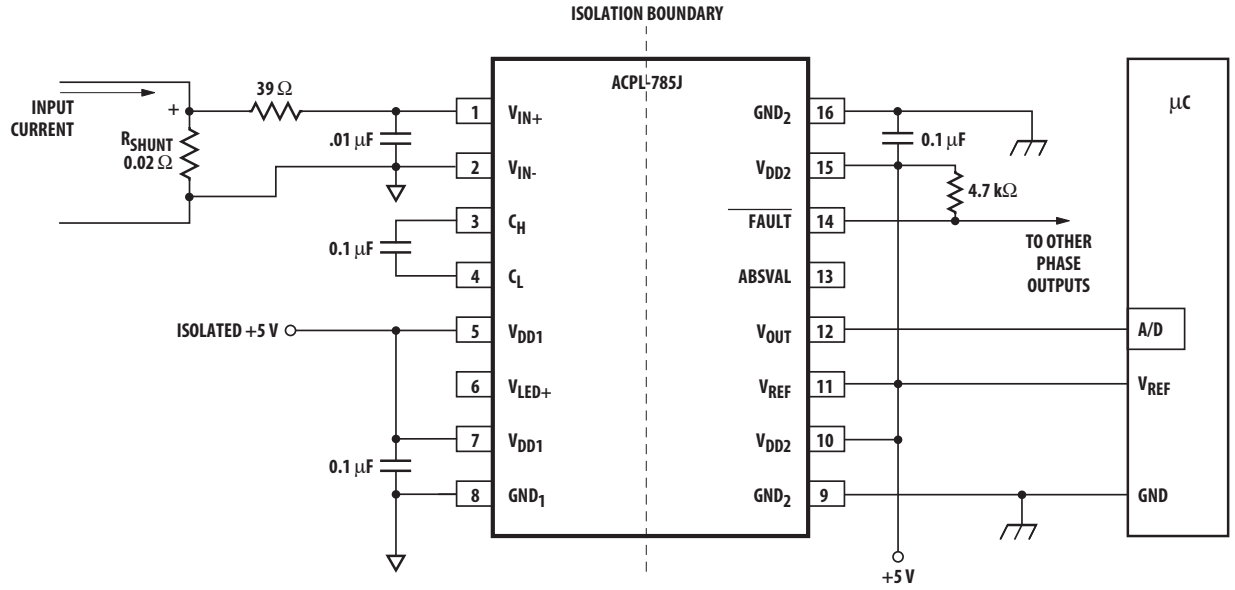


Figure 1. Current sensing circuit.

Pin Descriptions

Symbol	Description
V_{IN+}	Positive input voltage (±200 mV recommended).
V_{IN-}	Negative input voltage (normally connected to GND_1).
C_H / C_L	Internal Bias Node. Connections to or between C_H and C_L other than the required 0.1 μF capacitor shown, are not recommended.
V_{DD1}	Supply voltage input (4.5 V to 5.5 V).
V_{LED+}	LED anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
V_{DD1}	Supply voltage input (4.5 V to 5.5 V).
GND_1	Ground input.
GND_2	Ground input.
V_{DD2}	Supply voltage input (4.5 V to 5.5 V).

Symbol	Description
$\overline{\text{FAULT}}$	Short circuit fault output. $\overline{\text{FAULT}}$ changes from a high to low output voltage within 6 μs after V_{IN} exceeds the $\overline{\text{FAULT}}$ Detection Threshold. $\overline{\text{FAULT}}$ is an open drain output which allows outputs from all the ACPL-785Js in a circuit to be connected together ("wired-OR") forming a single fault signal for interfacing directly to the micro-controller.
ABSVAL	Absolute value of V_{OUT} output. ABSVAL is 0 V when V_{IN}=0 and increases toward V_{REF} as V_{IN} approaches +256 mV or -256 mV. ABSVAL is "wired-OR" able and is used for detecting overloads.
V_{OUT}	Voltage output. Swings from 0 to V_{REF}. The nominal gain is V_{REF}/504 mV.
V_{REF}	Reference voltage input (4.0 V to V_{DD2}). This voltage establishes the full scale output ranges and gains of V_{OUT} and ABSVAL.
V_{DD2}	Supply voltage input (4.5 V to 5.5 V).
GND_2	Ground input.

Ordering Information

ACPL-785J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-785J	-000E	SO-16	X			45 per tube
	-060E		X		X	45 per tube
	-500E		X	X		850 per reel
	-560E		X	X	X	850 per reel

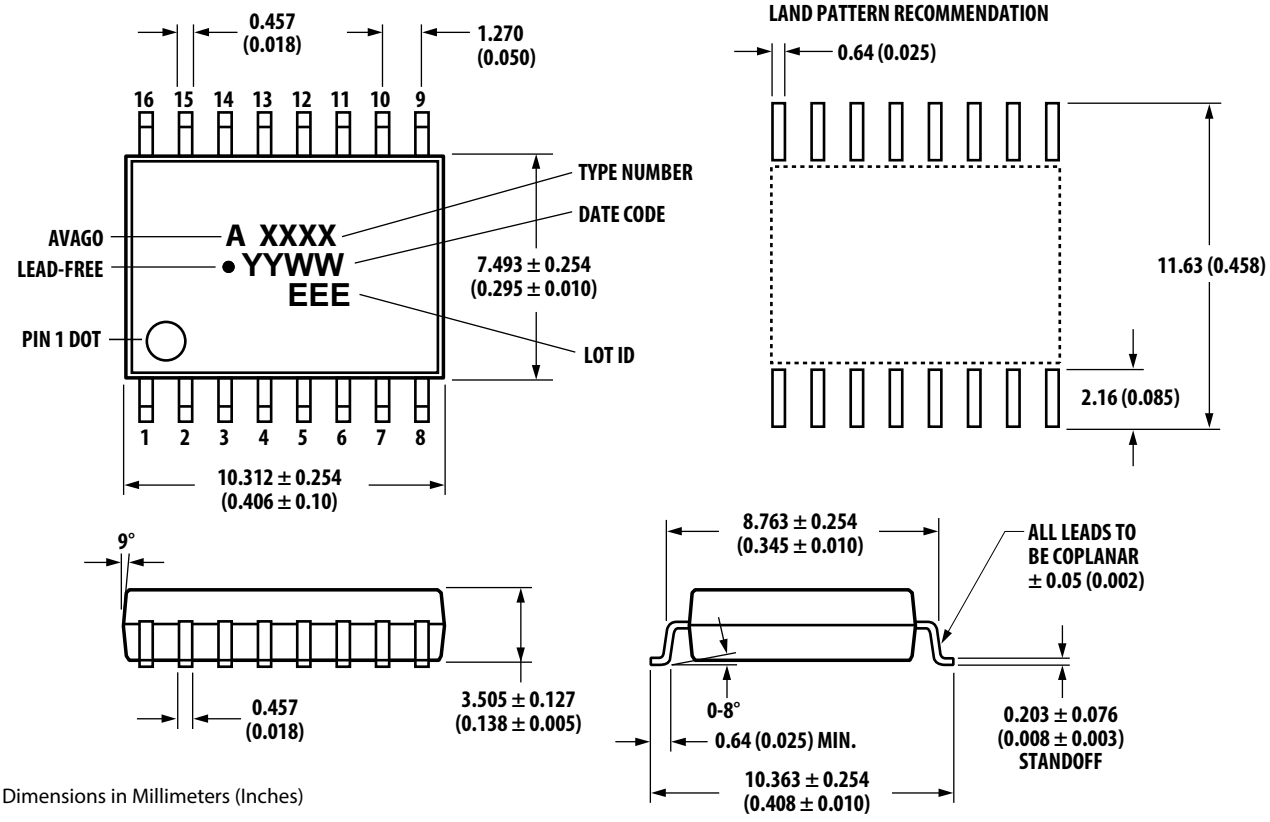
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example:

ACPL-785J-560E to order product of 16-Lead Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.

Package Outline Drawings

16-Lead Surface Mount



Dimensions in Millimeters (Inches)

Floating lead protrusion is 0.25 mm (10 mils) Max.

Note: Initial and continued variation in color of the white mold compound is normal and does not affect performance or reliability of the device

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-785J has been approved by the following organizations:

IEC/EN/DIN EN 60747-5-5	Approval under: DIN EN 60747-5-5 (VDE 0884-5):2011-11 EN 60747-5-5:2011
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V_{rms}		I-IV	
for rated mains voltage ≤ 600 V_{rms}		I-IV	
for rated mains voltage ≤ 1000 V_{rms}		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
Input to Output Test Voltage, Method b** V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2652	V_{PEAK}
Input to Output Test Voltage, Method a** V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	2262	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values — maximum values allowed in the event of a failure, also see Figure 2.			
Case Temperature	T_S	175	°C
Input Power	$P_{S1, INPUT}$	400	mW
Output Power	$P_{S1, OUTPUT}$	600	mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits within the application. Surface Mount Classification is class A in accordance with CECC00802.

** Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Avago Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

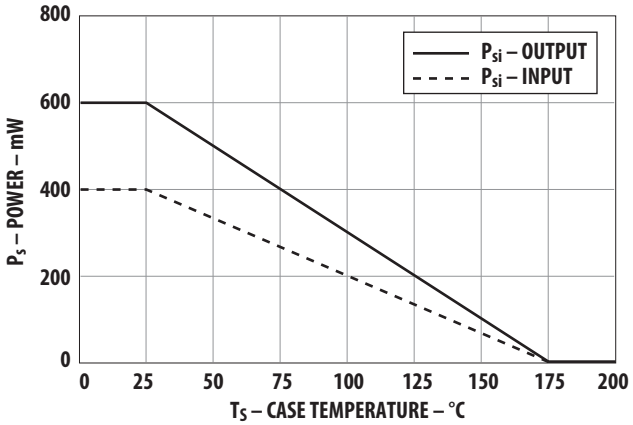


Figure 2. Dependence of safety-limiting values on temperature.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			Vrms	RH < 50%, t = 1 min., T_A = 25°C		1,2,3
Resistance (Input-Output)	R_{I-O}		$>10^9$		Ω	V_{I-O} = 500 V_{DC}		3
Capacitance (Input-Output)	C_{I-O}		1.3		pF	f = 1 MHz		3
Input IC Junction-to-Case Thermal Resistance	θjci		120		°C/W	T_A = 85°C		
Output IC Junction-to-Case Thermal Resistance	θjco		100		°C/W	T_A = 85°C		

Insulation and Safety Related Specifications

Parameter	Symbol	Min.	Max.	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1 Comparative Tracking Index)
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	4
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} + 0.5	V	
2 Second Transient Input Voltage	V_{IN+}, V_{IN-}	-6.0	V_{DD1} + 0.5	V	
Output Voltage	V_{OUT}	-0.5	V_{DD2} + 0.5	V	
Absolute Value Output Voltage	ABSVAL	-0.5	V_{DD2} + 0.5	V	
Reference Input Voltage	V_{REF}	0	V_{DD2} + 0.5 V	V	5
Reference Input Current	I_{REF}		20	mA	
Output Current	I_{VOUT}		20	mA	
Absolute Value Current	I_{ABSVAL}		20	mA	
$\overline{FAULT}$ Output Current	$I_{\overline{FAULT}}$		20	mA	
Input IC Power Dissipation	P_I		200	mW	
Output IC Power Dissipation	P_O		200	mW	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Ambient Operating Temperature	T_A	-40	85	°C	
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage (accurate and linear)	V_{IN+}, V_{IN-}	-200	200	mV	
Input Voltage (functional)	V_{IN+}, V_{IN-}	-2	2	V	
Reference Input Voltage	V_{REF}	4.0	V_{DD2}	V	
$\overline{FAULT}$ Output Current	$I_{\overline{FAULT}}$		4	mA	

DC Electrical Specifications

Unless otherwise noted, all typicals and figures are at the nominal operating conditions of V_{IN+} = 0, V_{IN-} = 0 V, V_{REF} = 4.0 V, V_{DD1} = V_{DD2} = 5 V and T_A = 25 °C; all Minimum/Maximum specifications are within the Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-3	0	3	mV	V_{IN+} = 0 V, T_A = –40 °C to +85 °C	3, 4, 5	6
Magnitude of Input Offset Change vs. Temperature	$\lvert\Delta V_{OS}/\Delta T_A\rvert$		1	10	µV/°C	V_{IN+} = 0 V, T_A = –40 °C to +85 °C		7
V_{OUT} Gain	G	V_{REF}/504 mV - 5%	V_{REF}/504 mV	V_{REF}/504 mV + 5%	V/V	$\lvert V_{IN+}\rvert$ < 200 mV, T_A = 25°C	6,7, 8,9	
Magnitude of V_{OUT} Gain Change vs. Temperature	$\lvert\Delta G/\Delta T_A\rvert$		50	300	ppm/°C	$\lvert V_{IN+}\rvert$ < 200 mV, T_A = –40 °C to +85 °C	6,7, 8,9	8
V_{OUT} 200 mV Nonlinearity	NL_{200}		0.06	0.4	%	$\lvert V_{IN+}\rvert$ < 200 mV, T_A = –40 °C to +85 °C	6,7, 8,9	
Maximum Input Voltage Before V_{OUT} Clipping	$\lvert V_{IN+}\rvert_{MAX}$		256		mV			
$\overline{\text{FAULT}}$ Detection Threshold	$\lvert V_{THF}\rvert$	230	256	280	mV		10	9
$\overline{\text{FAULT}}$ Low Output Voltage	V_{OLF}		350	800	mV	I_{OL} = 4 mA		
$\overline{\text{FAULT}}$ High Output Current	I_{OHF}		0.2	15	µA	$V_{\overline{\text{FAULT}}}$ = V_{DD2}		
ABSVAL Output Error	e_{ABS}		0.6	2	% of full scale output		11	10
Input Supply Current	I_{DD1}		10.7	20	mA			
Output Supply Current	I_{DD2}		10.4	20	mA			
Reference Voltage Input Current	I_{VREF}		0.26	1	mA			
Input Current	I_{IN+}		-350		nA	V_{IN+} = 0 V		
Input Resistance	R_{IN}		800		kΩ	V_{IN+} = 0 V		
V_{OUT} Output Resistance	R_{OUT}		0.2		Ω			
ABSVAL Output Resistance	R_{ABS}		0.3		Ω			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		85		dB			11

AC Electrical Specifications

Unless otherwise noted, all typicals and figures are at the nominal operating conditions of V_{IN+} = 0, V_{IN-} = 0 V, V_{REF} = 4.0 V, V_{DD1} = V_{DD2} = 5 V and T_A = 25°C; all Minimum/Maximum specifications are within the Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
V_{OUT} Bandwidth (-3dB)	BW	20	30		kHz	V_{IN+} = 200 mV_{pk-pk} sine wave.	12, 20	
V_{OUT} Noise	N_{OUT}		2.2	4	mVrms	V_{IN+} = 0 V	20	12
V_{IN} to V_{OUT} Signal Delay (50 - 50%)	t_{DSIG}		9	20	µs	V_{IN+} = 50 mV to 200 mV step.	14, 20	13
V_{OUT} Rise/Fall Time (10–90)	t_{RFSIG}		10	25	µs	V_{IN+} = 50 mV to 200 mV step.	14, 20	
ABSVAL Signal Delay	t_{DABS}		9	20	µs	V_{IN+} = 50 mV to 200 mV step.	14, 20	
ABSVAL Rise/Fall Time (10–90%)	t_{RFABS}		10	25	µs	V_{IN+} = 50 mV to 200 mV step.	14, 20	
$\overline{FAULT}$ Detection Delay	t_{FHL}		3	6	µs	V_{IN+} = 0 mV to ±500 mV step.	15, 20	14
$\overline{FAULT}$ Release Delay	t_{FLH}	10	20		µs	V_{IN+} = ±500 mV to 0 mV step.	16, 20	15
Transient Fault Rejection	t_{REJECT}	1	2		µs	V_{IN+} = 0 mV to ±500 mV pulse.	17, 20	16
Common Mode Transient Immunity	CMTI	10	25		kV/µs	For V_{OUT}, $\overline{FAULT}$, and ABSVAL outputs.		17
Common-Mode Rejection Ratio at 60 Hz	CMRR		>140		dB			18

Notes:

1. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table, if applicable.
2. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 insulation characteristics table.
3. Device considered a two terminal device: pins 1-8 shorted together and pins 9-16 shorted together.
4. V_{DD1} must be applied to both pins 5 and 7. V_{DD2} must be applied to both pins 10 and 15.
5. If V_{REF} exceeds V_{DD2} (due to power-up sequence, for example), the current into pin 11 (I_{REF}) should be limited to 20 mA or less.
6. Input Offset voltage is defined as the DC Input voltage required to obtain an output voltage (at pin 12) of $V_{REF}/2$.
7. This is the Absolute Value of Input Offset Change vs. Temperature.
8. This is the Absolute Value of V_{OUT} Gain Change vs. Temperature.
9. $|V_{IN+}|$ must exceed this amount in order for the $\overline{FAULT}$ output to be activated.
10. ABSVAL is derived from V_{OUT} (which has the gain and offset tolerances stated earlier). ABSVAL is 0 V when V_{IN} = 0 V and increases toward V_{REF} as V_{IN} approaches +256 mV or -256 mV. ε_{ABS} is the difference between the actual ABSVAL output and what ABSVAL should be, given the value of V_{OUT}. ε_{ABS} is expressed in terms of percent of full scale and is defined as:

$$\frac{|ABSVAL - 2 \times |V_{OUT} - V_{REF}/2||}{V_{REF}} \times 100.$$

11. $CMRR_{IN}$ is defined as the ratio of the gain for differential inputs applied between pins 1 and 2 to the gain for common mode inputs applied to both pins 1 and 2 with respect to pin 8.
12. The signal-to-noise ratio of the ACPL-785J can be improved with the addition of an external low pass filter to the output. See Frequently Asked Question #4.2 in the Applications Information Section at the end of this data sheet.
13. As measured from 50% of V_{IN} to 50% of V_{OUT}.
14. This is the amount of time from when the $\overline{FAULT}$ Detection Threshold (230 mV ≤ V_{THF} ≤ 280 mV) is exceeded to when the $\overline{FAULT}$ output goes low.
15. This is the amount of time for the $\overline{FAULT}$ Output to return to a high state once the $\overline{FAULT}$ Detection Threshold (230 mV ≤ V_{THF} ≤ 280 mV) is no longer exceeded.
16. Input pulses shorter than the fault rejection pulse width (t_{REJECT}), will not activate the $\overline{FAULT}$ (pin 14) output. See Frequently Asked Question #2.3 in the Applications Information Section at the end of this data sheet for additional detail on how to avoid false tripping of the $\overline{FAULT}$ output due to cable capacitance charging transients.
17. CMTI is also known as Common Mode Rejection or Isolation Mode Rejection. It is tested by applying an exponentially rising falling voltage step on pin 8 (GND1) with respect to pin 9 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until V_{OUT} (pin 12) exhibits more than 100 mV deviation from the average output voltage for more than 1μs. The ACPL-785J will continue to function if more than 10 kV/μs common mode slopes are applied, as long as the break-down voltage limitations are observed. [The ACPL-785J still functions with common mode slopes above 10 kV/μs, but output noise may increase to as much as 600 mV peak to peak.]
18. CMRR is defined as the ratio of differential signal gain (signal applied differentially between pins 1 and 2) to the common mode gain (input pins tied to pin 8 and the signal applied between the input and the output of the isolation amplifier) at 60 Hz, expressed in dB.

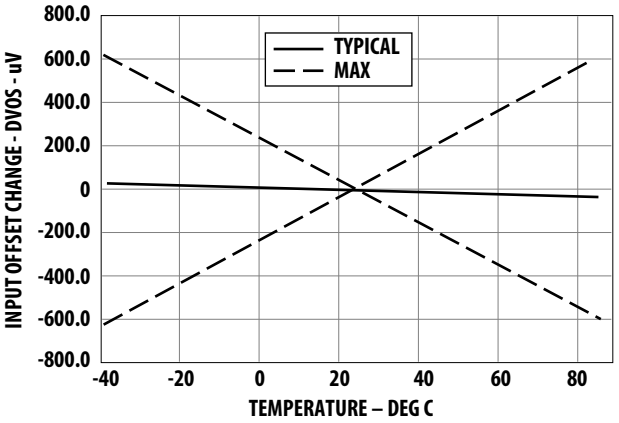


Figure 3. Input offset voltage change vs. temperature.

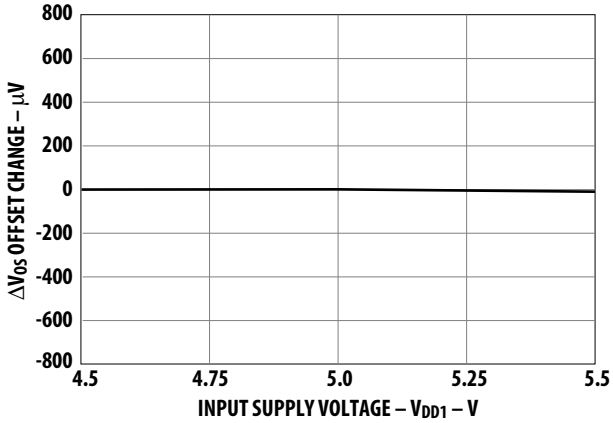


Figure 4. Input offset voltage change vs. V_{DD1}.

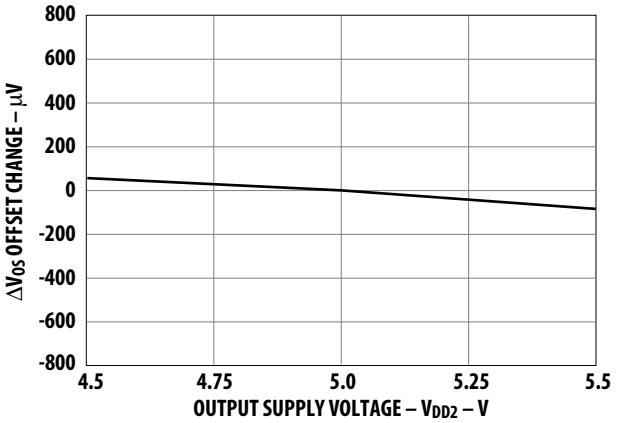


Figure 5. Input offset voltage change vs. V_{DD2}.

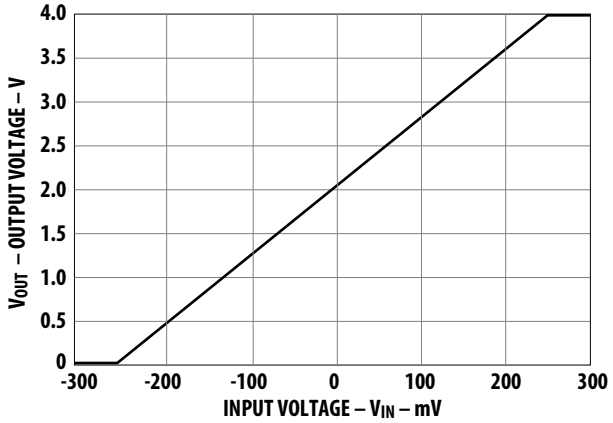


Figure 6. V_{OUT} vs. V_{IN}.

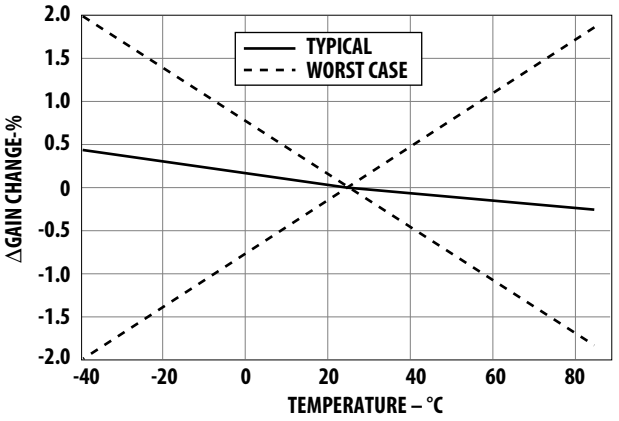


Figure 7. Gain change vs. temperature.

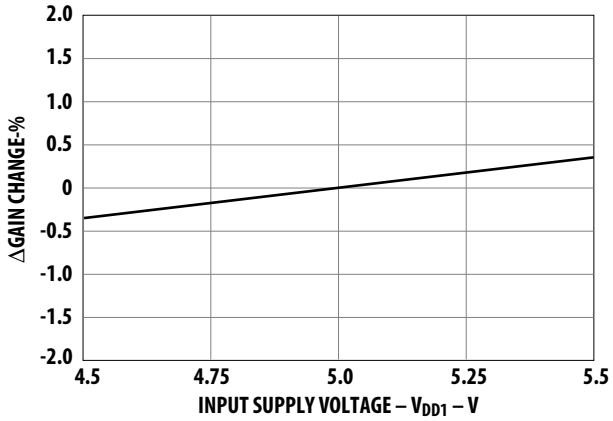


Figure 8. Gain change vs. V_{DD1}.

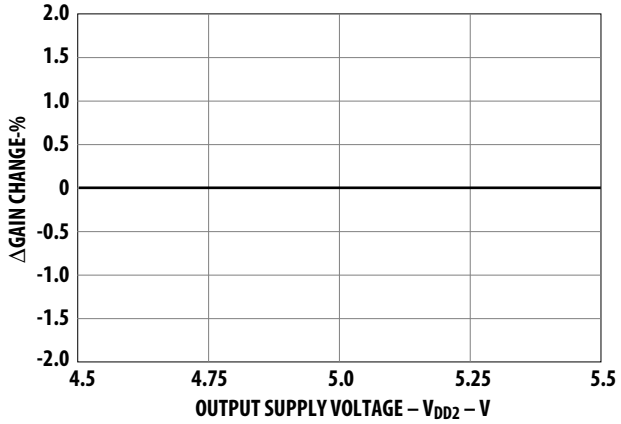


Figure 9. Gain change vs. V_{DD2}.

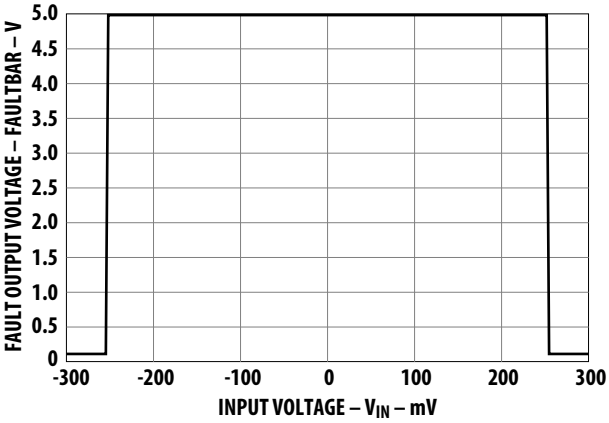


Figure 10. $\overline{\text{FAULT}}$ output voltage vs. V_{IN}.

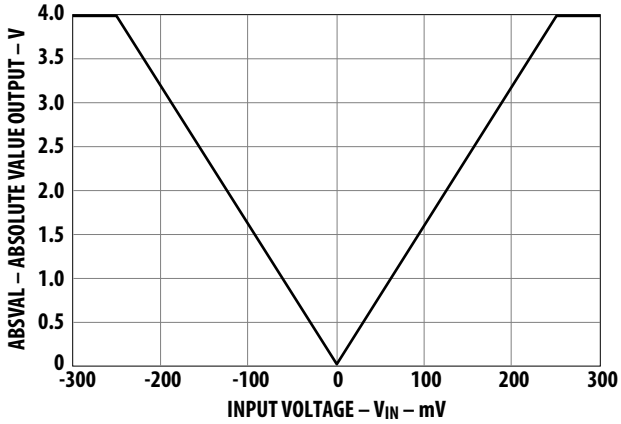


Figure 11. ABSVAL output voltage vs. V_{IN}.

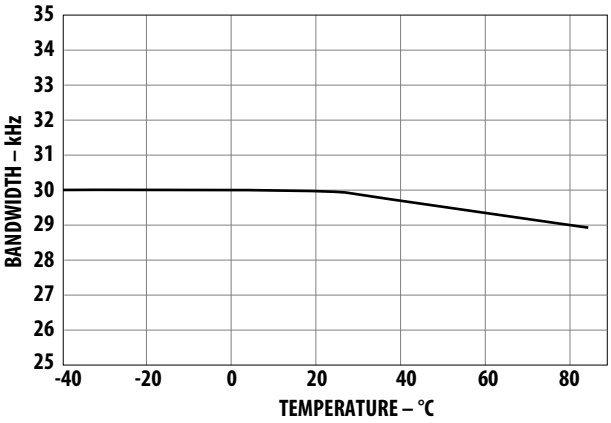


Figure 12. Bandwidth vs. temperature.

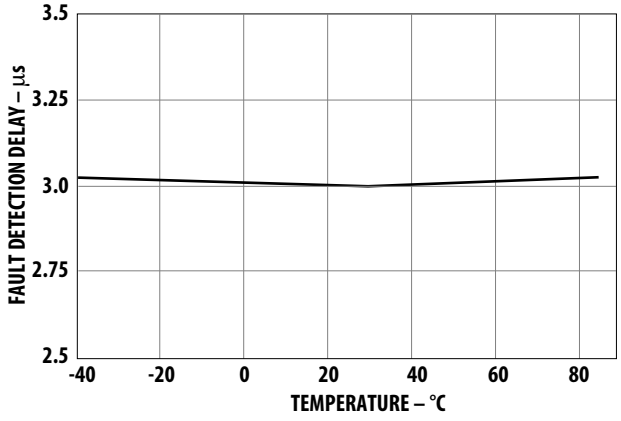


Figure 13. $\overline{\text{FAULT}}$ detection delay vs. temperature.

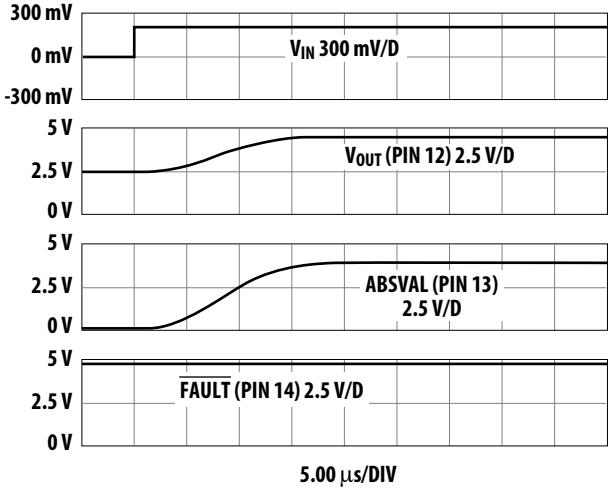


Figure 14. Step response, 0 to 200 mV input, at V_{REF} = 5 V.

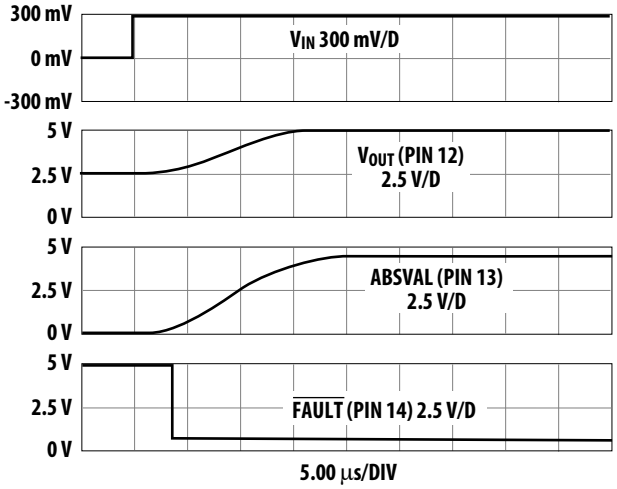


Figure 15. $\overline{\text{FAULT}}$ detection, 0 to 300 mV input, at V_{REF} = 5 V.

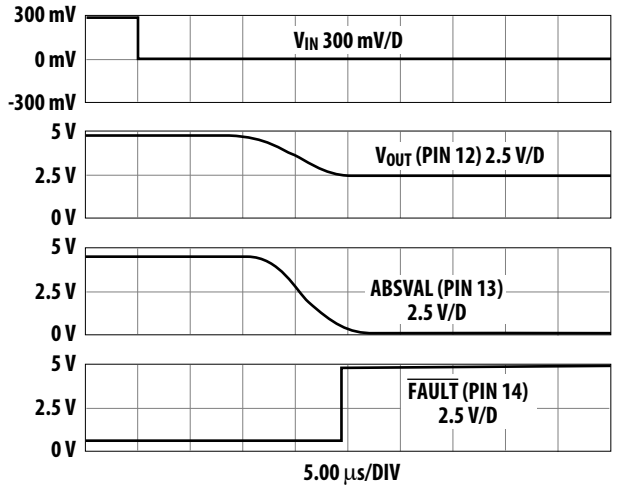


Figure 16. $\overline{\text{FAULT}}$ release, 300 to 0 mV input, at V_{REF} = 5 V.

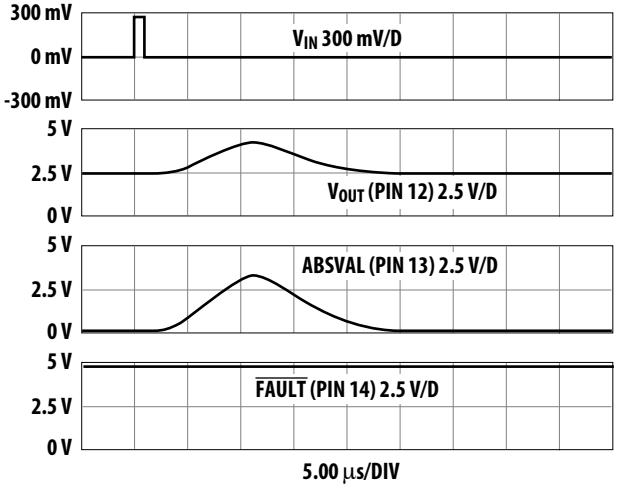


Figure 17. $\overline{\text{FAULT}}$ rejecting a 1 µs, 0 to 2 V to 0 input. Rejection is independent of amplitude.

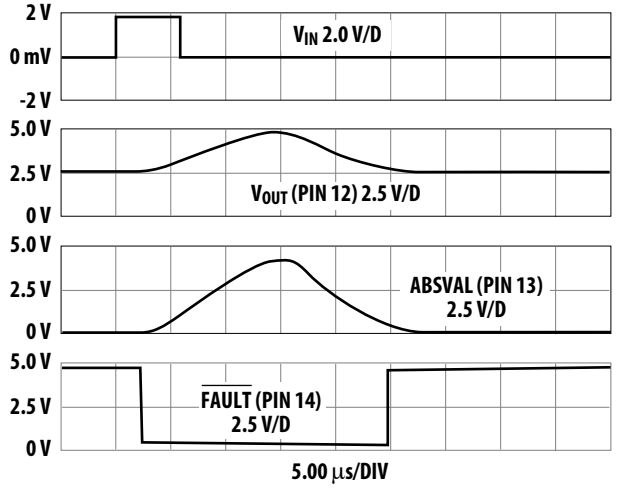


Figure 18. Detection of 6 µs fault 0 to 2 V to 0 input, at V_{REF} = 5 V.

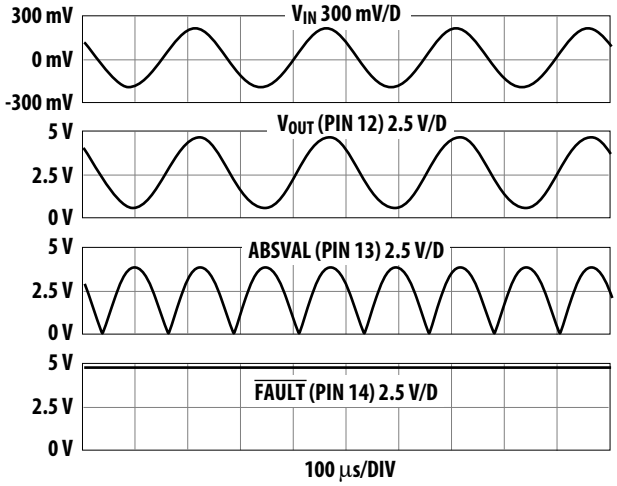


Figure 19. Sine response 400 mV pk to pk 4 kHz input, at V_{REF} = 5 V.

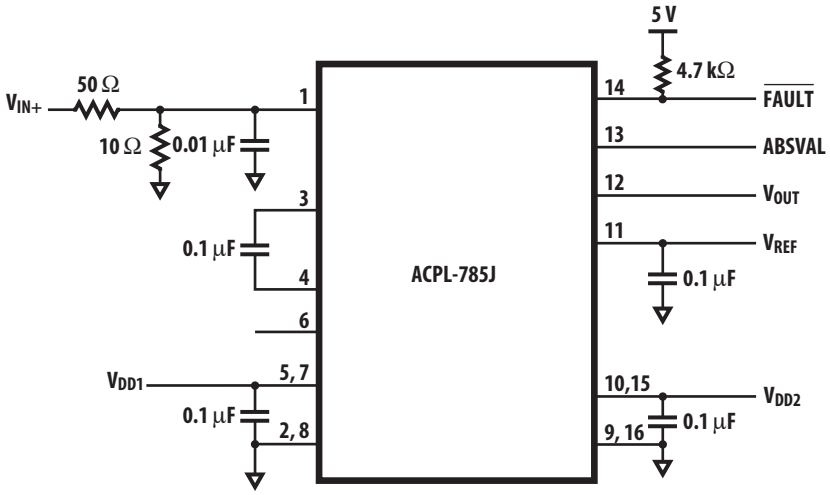


Figure 20. AC test circuit.

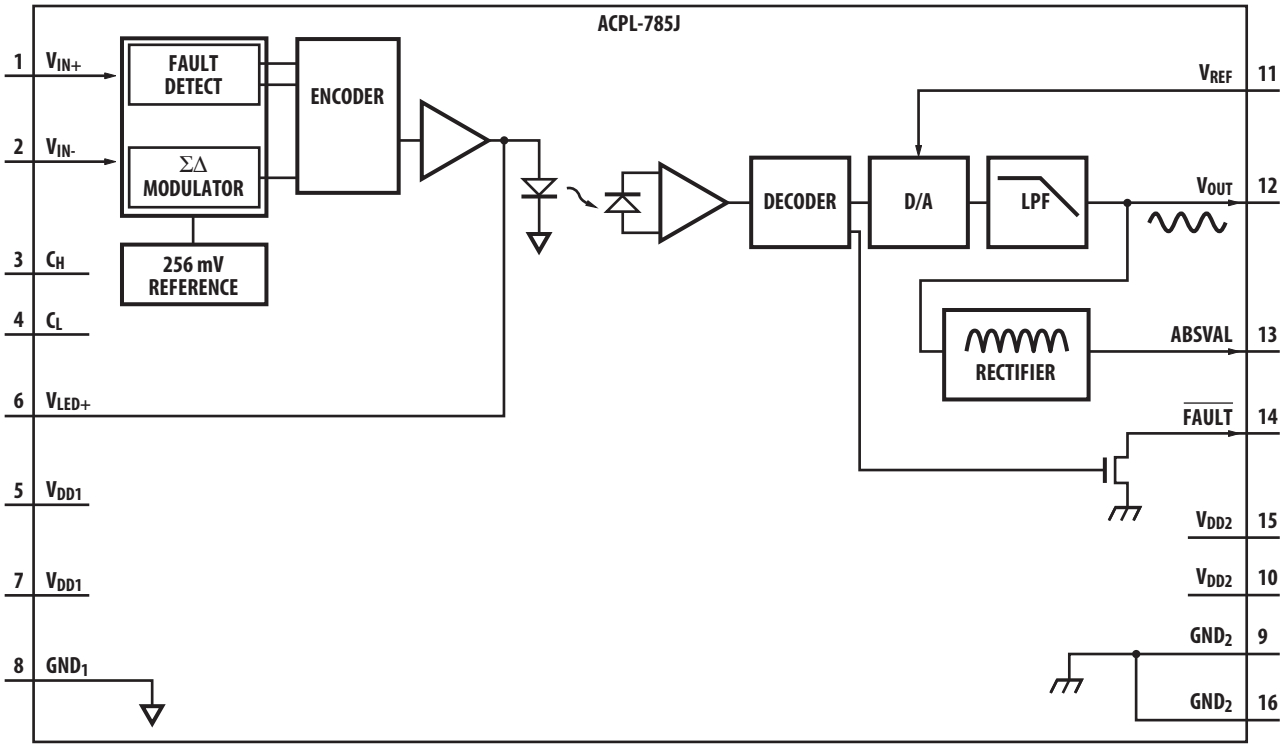


Figure 21. Internal block diagram.

Applications Information

Production Description

Figure 21 shows the internal block diagram of the ACPL-785J. The analog input (V_{IN}) is converted to a digital signal using a sigma-delta (Σ–Δ) analog to digital (A/D) converter. This A/D samples the input 6 million times per second and generates a high speed 1-bit output representing the input very accurately. This 1 bit data stream is transmitted via a light emitting diode (LED) over the optical barrier after encoding. The detector converts the optical signal back to a bit stream. This bit stream is decoded and drives a 1 bit digital to analog (D/A) converter. Finally a low pass filter and output buffer drive the output signal (V_{OUT}) which linearly represents the analog input. The output signal full-scale range is determined by the external reference voltage (V_{REF}). By sharing this reference voltage (which can be the supply voltage), the full-scale range of the ACPL-785J can precisely match the full-scale range of an external A/D converter.

In addition, the ACPL-785J compares the analog input (V_{IN}) to both the negative and positive full-scale values. If the input exceeds the full-scale range, the short-circuit fault output ($\overline{FAULT}$) is activated quickly. This feature operates independently of the Σ–Δ A/D converter in order to provide the high-speed response (typically 3 µs) needed to protect power transistors. The $\overline{FAULT}$ output is wire OR-able so that a short circuit on any one motor phase can be detected using only one signal.

One other output is provided — the rectified output (ABSVAL). This output is also wire OR-able. The motor phase having the highest instantaneous rectified output pulls the common output high. When three sinusoidal motor phases are combined, the rectified output (ABSVAL) is essentially a DC signal representing the rms motor current. This single DC signal and a threshold comparator can indicate motor overload conditions before damage to the motor or drive occur. Figure 22 shows the ABSVAL output when 3 ACPL-785Js are used to monitor a sinusoidal 60 Hz current. Figures 23 and 24 show the ABSVAL output when only 2 or 1 of the 3 phases are monitored, respectively.

The ACPL-785J's other main function is to provide galvanic isolation between the analog input and the analog output. An internal voltage reference determines the full-scale analog input range of the modulator (approximately ±256 mV); an input range of ±200 mV is recommended to achieve optimal performance.

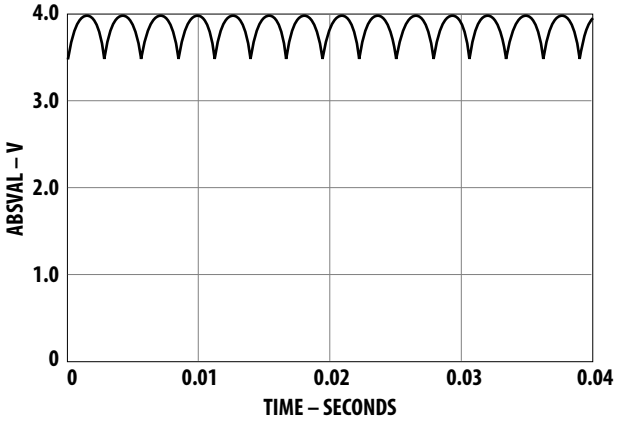


Figure 22. ABSVAL with 3 phases, wired-ORed together.

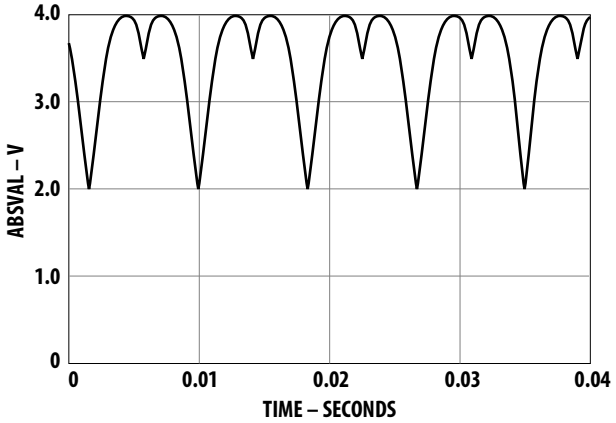


Figure 23. ABSVAL with 2 phases, wired-ORed together.

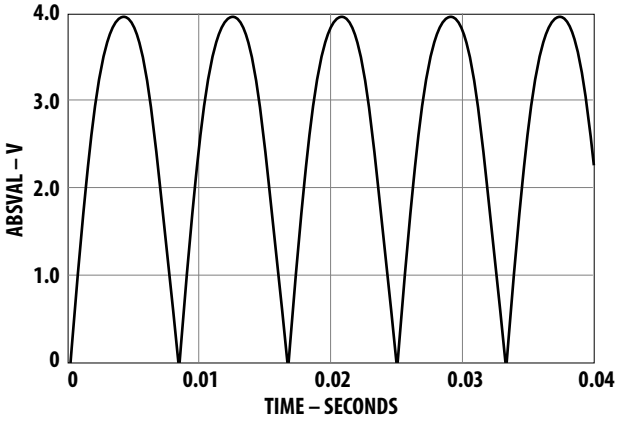


Figure 24. ABSVAL with 1 phase.

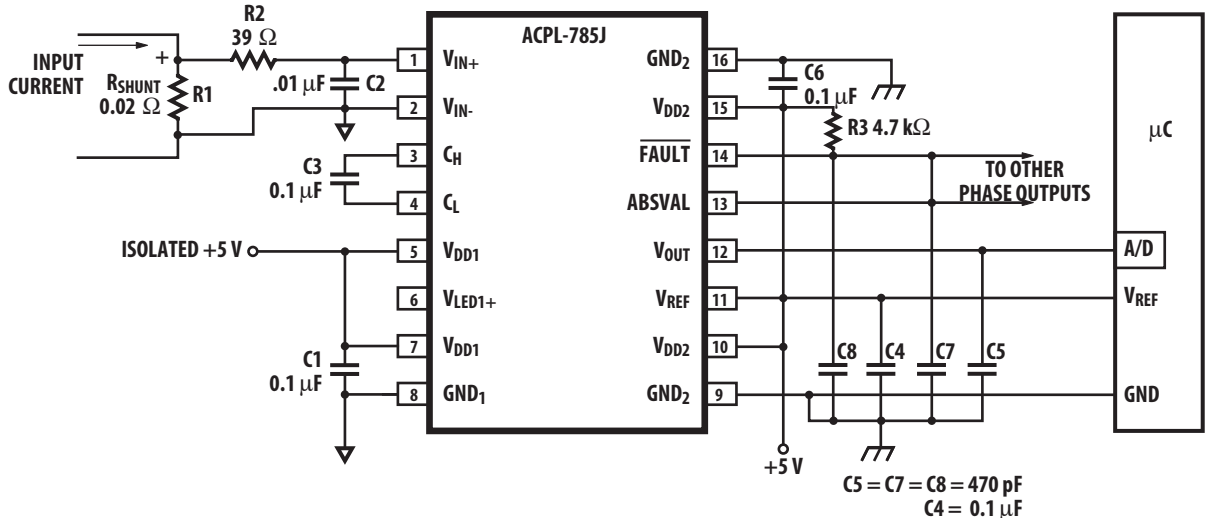


Figure 25. Recommended applications circuit.

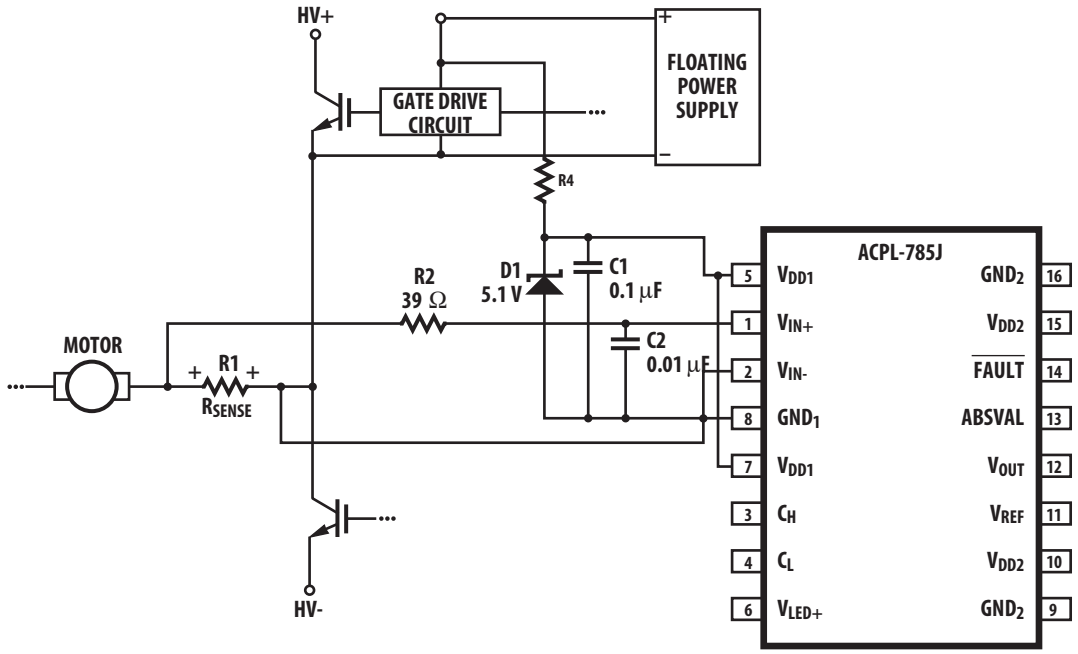


Figure 26. Recommended supply and sense resistor connections.

Analog Interfacing

Power Supplies and Bypassing

The recommended supply connections are shown in Figure 26. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple zener diode (D1); the value of resistor R4 should be chosen to supply sufficient current from the existing floating supply. The voltage from the current sensing resistor (Rsense) is applied to the input of the ACPL-785J through an RC anti-aliasing filter (R2 and C2). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the ACPL-785J is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

An inexpensive 78L05 three-terminal regulator can also be used to reduce the floating supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

As shown in Figure 25, 0.1 µF bypass capacitors (C1, C3, C4, and C6) should be located as close as possible to the pins of the ACPL-785J. The bypass capacitors are required because of the high-speed digital nature of the signals inside the ACPL-785J. A 0.01 µF bypass capacitor (C2) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. The input filter also performs an important reliability function — it reduces transient spikes from ESD events flowing through the current sensing resistor.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the ACPL-785J, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMTI performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the ACPL-785J.

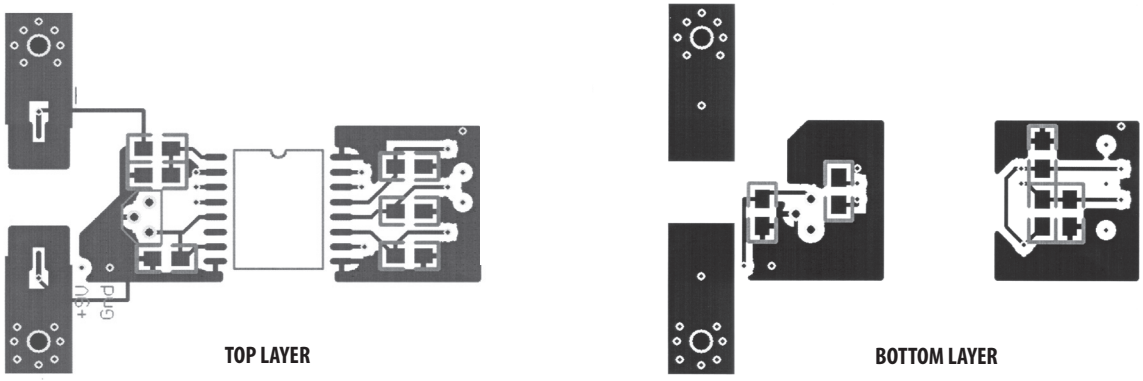


Figure 27. Example printed circuit board layout.

Current Sensing Resistors

The current sensing resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistance decreases power dissipation, while larger sense resistance can improve circuit accuracy by utilizing the full input range of the ACPL-785J.

The first step in selecting a sense resistor is determining how much current the resistor will be sensing. The graph in Figure 28 shows the rms current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the sense resistor is determined by the current being measured and the maximum recommended input voltage of the isolation amplifier. The maximum sense resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the sense resistor should see during normal operation. For example, if a motor will have a maximum rms current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10 x 1.414 x 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of sense resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the sense resistor can also be easily calculated by multiplying the sense resistance times the square of the maximum rms current, which is about 1 W in the previous example.

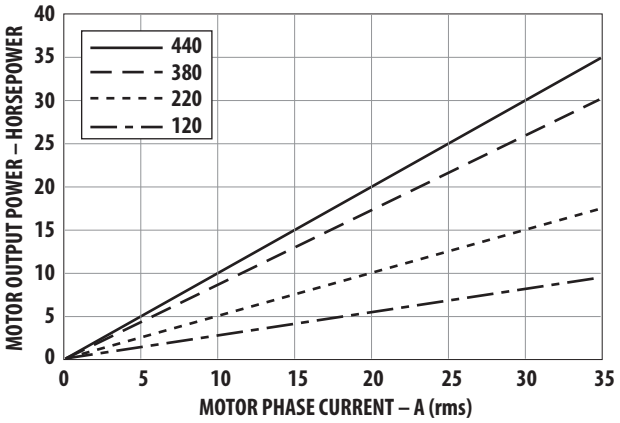


Figure 28. Motor output horsepower vs. motor phase current and supply voltage.

If the power dissipation in the sense resistor is too high, the resistance can be decreased below the maximum value to decrease power dissipation. The minimum value of the sense resistor is limited by precision and accuracy requirements of the design. As the resistance value is reduced, the output voltage across the resistor is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the sense resistor will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the sense resistor, the temperature coefficient (tempco) of the resistor can introduce nonlinearity due to the signal dependent temperature rise of the resistor. The effect increases as the resistor-to-ambient thermal resistance increases. This effect can be minimized by reducing the thermal resistance of the current sensing resistor or by using a resistor with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the current sensing resistor on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal current sensing resistor, as the value of resistance decreases, the resistance of the leads become a significant percentage of the total resistance. This has two primary effects on resistor accuracy. First, the effective resistance of the sense resistor can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the leads during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material, such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco overall.

Both of these effects are eliminated when a four-terminal current sensing resistor is used. A four-terminal resistor has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

When laying out a PC board for the current sensing resistors, a couple of points should be kept in mind. The Kelvin connections to the resistor should be brought together under the body of the resistor and then run very close to each other to the input of the ACPL-785J; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the sense resistor is not located on the same PC board as the ACPL-785J circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the sense resistor to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the sense resistor's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Sense Resistor Connections

The recommended method for connecting the ACPL-785J to the current sensing resistor is shown in Figure 26. V_{IN+} (pin 1 of the ACPL-785J) is connected to the positive terminal of the sense resistor, while V_{IN-} (pin 2) is shorted to GND_1 (pin 8), with the power-supply return path functioning as the sense line to the negative terminal of the current sense resistor. This allows a single pair of wires or PC board traces to connect the ACPL-785J circuit to the sense resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the resistor are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current sensing resistor.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND_1 of the ACPL-785J to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the ACPL-785J circuit and the gate drive circuit should be the positive power supply line. Please refer to Avago Technologies' Applications Note 1078 for additional information on using Isolation Amplifiers.

Frequently Asked Questions about the ACPL-785J

1. The Basics

1.1: Why should I use the ACPL-785J for sensing current when Hall-effect sensors are available which don't need an isolated supply voltage?	Historically, motor control current sense designs have required trade-offs between signal accuracy, response time, and the use of discrete components to detect short circuit and overload conditions. The ACPL-785J greatly simplifies current-sense designs by providing an output voltage which can connect directly to an A/D converter as well as integrated short circuit and overload detection (eliminating the need for external circuitry). Available in an auto-insertable, SO-16 package, the ACPL-785J is smaller than and has better linearity, offset vs. temperature and Common Mode Rejection (CMR) performance than most Hall-effect sensors.
1.2: What is the purpose of the V_{REF} input?	The V_{REF} input establishes the full scale output range. V_{REF} can be connected to the supply voltage (V_{DD2}) or a voltage between 4 V and V_{DD2}. The nominal gain of the ACPL-785J is the output full scale range divided by 504 mV.
1.3: What is the purpose of the rectified (ABSVAL) output on pin 13?	When 3 phases are wire-ORed together, the 3 phase AC currents are combined to form a DC voltage with very little ripple on it. This can be simply filtered and used to monitor the motor load. Moderate overload currents which don't trip the $\overline{\text{FAULT}}$ output can thus be detected easily.

2. Sense Resistor and Input Filter

2.1: Where do I get 10 mΩ resistors? I have never seen one that low.	Although less common than values above 10 Ω, there are quite a few manufacturers of resistors suitable for measuring currents up to 50 A when combined with the ACPL-785J. Example product information may be found at Vishay's web site (http://www.vishay.com) and Isotek's web site (http://www.isotekcorp.com).
2.2: Should I connect both inputs across the sense resistor instead of grounding V_{IN-} directly to pin 8?	This is not necessary, but it will work. If you do, be sure to use an RC filter on both pin 1 (V_{IN+}) and pin 2 (V_{IN-}) to limit the input voltage at both pads.
2.3: How can I avoid false tripping of the fault output due to cable capacitance charging transients?	In PWM motor drives there are brief spikes of current flowing in the wires leading to the motor each time a phase voltage is switched between states. The amplitude and duration of these current spikes is determined by the slew rate of the power transistors and the wiring impedances. To avoid false tripping of the $\overline{\text{FAULT}}$ output (pin 14) the ACPL-785J includes a blanking filter. This filter ignores over-range input conditions shorter than 1 μs. For very long motor wires, it may be necessary to increase the time constant of the input RC antialiasing filter to keep the peak value of the ACPL-785J inputs below ±230 mV. For example, a 39 Ω, 0.047 μF RC filter on pin 1 will ensure that 2 μs wide 500 mV pulses across the sense resistor do not trip the $\overline{\text{FAULT}}$ output.
2.4: Do I really need an RC filter on the input? What is it for? Are other values of R and C okay?	This filter prevents damage from input spikes which may go beyond the absolute maximum ratings of the ACPL-785J inputs during ESD and other transient events. The filter also prevents aliasing of high frequency (above 3 MHz) noise at the sampled input. Other RC values are certainly OK, but should be chosen to prevent the input voltage (pin 1) from exceeding ±5 V for any conceivable current waveform in the sense resistor. Remember to account for inductance of the sense resistor since it is possible to momentarily have tens of volts across even a 1 mΩ resistor if di/dt is quite large.
2.5: How do I ensure that the ACPL-785J is not destroyed as a result of short circuit conditions which cause voltage drops across the sense resistor that exceed the ratings of the ACPL-785J's inputs?	Select the sense resistor so that it will have less than 5 V drop when short circuits occur. The only other requirement is to shut down the drive before the sense resistor is damaged or its solder joints melt. This ensures that the input of the ACPL-785J cannot be damaged by sense resistors going open-circuit.

3. Isolation and Insulation

3.1: How many volts will the ACPL-785J withstand?	The momentary (1 minute) withstand voltage is 5000 V rms per UL1577 and CSA Component Acceptance Notice #5.
***3.2:* What happens if I don't use the 470 pF output capacitors Avago recommends?**	These capacitors are to reduce the narrow output spikes caused by high common mode slew rates. If your application does not have rapid common mode voltage changes, these capacitors are not needed.

4. Accuracy

4.1: What is the meaning of the offset errors and gain errors in terms of the output?	For zero input, the output should ideally be $^1/_2$ of V_{REF}. The nominal slope of the input/output relationship is V_{REF} divided by 0.504 V. Offset errors change only the DC input voltage needed to make the output equal to $^1/_2$ of V_{REF}. Gain errors change only the slope of the input/output relationship. For example, if V_{REF} is 4.0 V, the gain should be 7.937 V/V. For zero input, the output should be 2.000 V. Input offset voltage of ±3 mV means the output voltage will be 2.000 V ±0.003*7.937 or 2.000 ±23.8 mV when the input is zero. Gain tolerance of ±5% means that the slope will be 7.937 ±0.397. Over the full range of ±3 mV input offset error and ±5% gain error, the output voltage will be 2.000 ±25.0 mV when the input is zero.
4.2: Can the signal to noise ratio be improved?	Yes. Some noise energy exists beyond the 30 kHz bandwidth of the ACPL-785J. An external RC low pass filter can be used to improve the signal to noise ratio. For example, a 680 Ω, 4700 pF RC filter will cut the rms output noise roughly by a factor of 2. This filter reduces the -3dB signal bandwidth only by about 10%. In applications needing only a few kHz bandwidth even better noise performance can be obtained. The noise spectral density is roughly 400 nV/$\sqrt{\text{Hz}}$ below 15 kHz (input referred). As an example, a 2 kHz (680 Ω, 0.1 μF) RC low pass filter reduces output noise to a typical value of 0.08 mVrms.
4.3: I need 1% tolerance on gain. Does Avago sell a more precise version?	At present Avago does not have a standard product with tighter gain tolerance. A 100 Ω variable resistor divider can be used to adjust the input voltage at pin 1, if needed.
4.4: The output doesn't go all the way to V_{REF} when the input is above full scale. Why not?	Op-amps are used to drive V_{OUT} (pin 12) and ABSVAL (pin 13). These op-amps can swing nearly from rail to rail when there is no load current. The internal V_{DD2} is about 100 mV below the external V_{DD2}. In addition, the pullup and pulldown output transistors are not identical in capability. The net result is that the output can typically swing to within 20 mV of GND_2 and to within 150 mV of V_{DD2}. When V_{REF} is tied to V_{DD2}, the output cannot reach V_{REF} exactly. This limitation has no effect on gain — only on maximum output voltage. The output remains linear and accurate for all inputs between -200 mV and +200 mV. For the maximum possible swing range, separate V_{REF} and V_{DD2} voltages can be used. Since 5.0 V is normally recommended for V_{DD2}, use of 4.5 V or 4.096 V references for V_{REF} allow the outputs to swing all the way up to V_{REF} (and down to typically 20 mV).
4.5: Does the gain change if the internal LED light output degrades with time?	No. The LED is used only to transmit a digital pattern. Gain is determined by a bandgap voltage reference and the user-provided V_{REF}. Avago has accounted for LED degradation in the design of the product to ensure long life.
4.6: Why is gain defined as V_{REF}/504 mV, not V_{REF}/512 mV as expected, based on Figure 24?	Ideally gain would be V_{REF}/512 mV, however, due to internal settling characteristics, the average effective value of the internal 256 mV reference is 252 mV.

5. Power Supplies and Start-Up

5.1: What are the output voltages before the input side power supply is turned on?	V_{OUT} (pin 12) is close to zero volts, ABSVAL (pin 13) is close to V_{REF} and $\overline{FAULT}$ (pin 14) is in the high (inactive) state when power to the input side is off. In fact, a self test can be performed using this information. In a motor drive, it is possible to turn off all the power transistors and thus cause all the sense resistor voltages to be zero. In this case, finding V_{OUT} less than $^1/_4$ of V_{REF}, ABSVAL more than $^3/_4$ of V_{REF} and $\overline{FAULT}$ in the high state indicates that power to the input side is not on.
5.2: How long does the ACPL-785J take to begin working properly after power-up?	About 50 µs after a V_{DD2} power-up and 100 µs after a V_{DD1} power-up.

6. Miscellaneous

6.1: How does the ACPL-785J measure negative signals with only a +5 V supply?	The inputs have a series resistor for protection against large negative inputs. Normal signals are no more than 200 mV in amplitude. Such signals do not forward bias any junctions sufficiently to interfere with accurate operation of the switched capacitor input circuit.
6.2: What load capacitance can the ACPL-785J drive?	Typically, noticeable ringing and overshoot begins for C_{LOAD} above 0.02 µF. Avago recommends keeping the load capacitance under 5000 pF (at pin 12). ABSVAL (pin 13) typically exhibits no instability at any load capacitance, but speed of response gradually slows above 470 pF load.
6.3: Can I use the ACPL-785J with a bipolar input A/D converter?	Yes, with a compromise on offset accuracy. One way to do this is by connecting +2.5 V to pins 10, 11, and 15 and connecting -2.5 V to pins 9 and 16 with 0.1 µF bypass capacitors from +2.5 V to -2.5 V and from -2.5 V to ground. Note that $\overline{FAULT}$ cannot swing above 2.5 V in this case, so a level shifter may be needed. Alternately, a single 5 V supply could be power the ACPL-785J which could drive an op amp configured to subtract $^1/_2$ of V_{REF} from V_{OUT}.

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