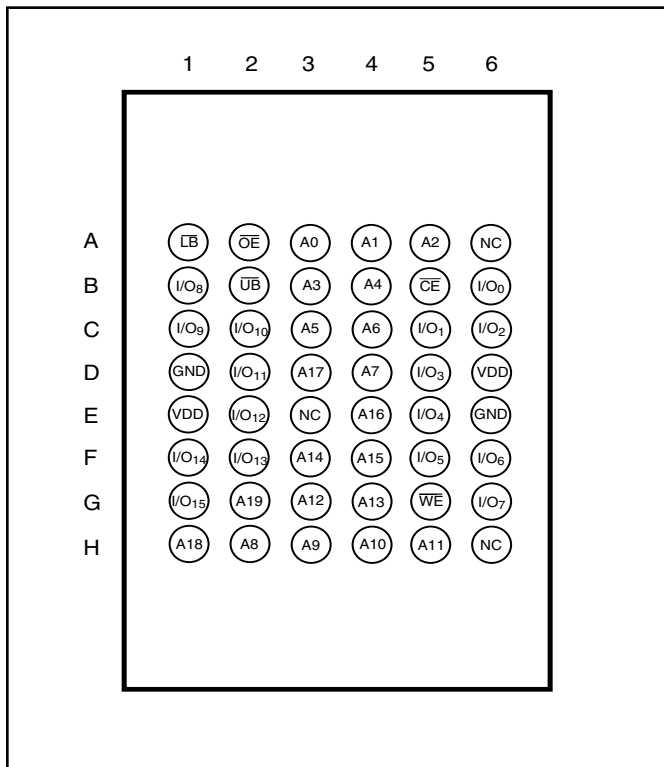


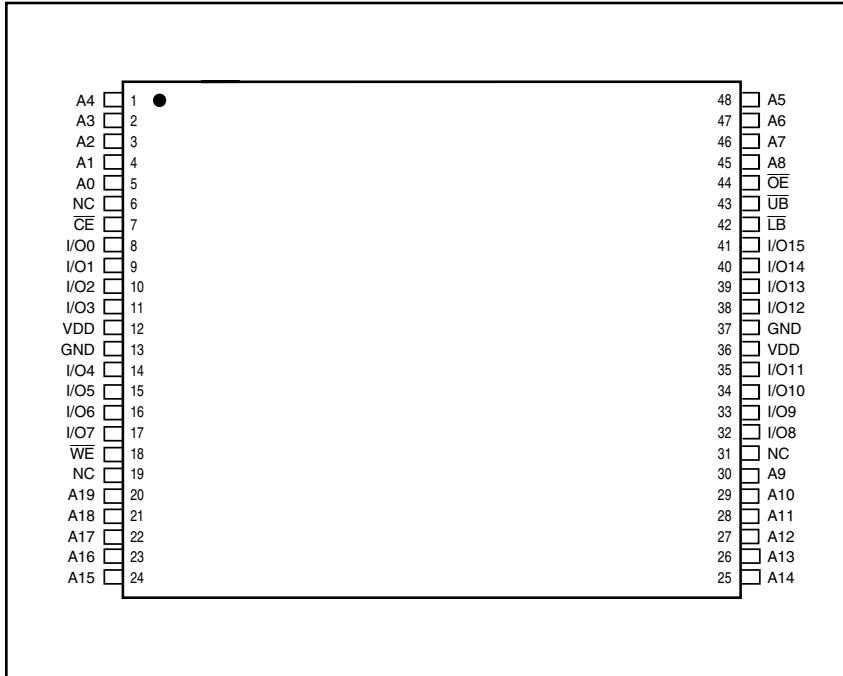
48-pin mini BGA (9mmx11mm)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A19 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| V _{DD} | Power |
| GND | Ground |

48-pin TSOP-I (12mm x 20mm)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A19 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

TRUTH TABLE

| Mode | | | | | | I/O PIN | | V _{DD} Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------------------------------------|
| | \overline{WE} | \overline{CE} | \overline{OE} | \overline{LB} | \overline{UB} | I/O0-I/O7 | I/O8-I/O15 | |
| Not Selected | X | H | X | X | X | High-Z | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | I _{CC} |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | D _{OUT} | High-Z | I _{CC} |
| | H | L | L | H | L | High-Z | D _{OUT} | |
| | H | L | L | L | L | D _{OUT} | D _{OUT} | |
| Write | L | L | X | L | H | D _{IN} | High-Z | I _{CC} |
| | L | L | X | H | L | High-Z | D _{IN} | |
| | L | L | X | L | L | D _{IN} | D _{IN} | |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | V _{DD} Relates to GND | -0.3 to 4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

OPERATING RANGE (V_{DD}) (IS61WV102416ALL)

| Range | Ambient Temperature | V _{DD} (20 ns) |
|------------|---------------------|-------------------------|
| Commercial | 0°C to +70°C | 1.65V-2.2V |
| Industrial | -40°C to +85°C | 1.65V-2.2V |
| Automotive | -40°C to +125°C | 1.65V-2.2V |

OPERATING RANGE (V_{DD}) (IS61WV102416BLL)⁽¹⁾

| Range | Ambient Temperature | V _{DD} (8 ns) | V _{DD} (10 ns) |
|------------|---------------------|------------------------|-------------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 2.4V-3.6V |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 2.4V-3.6V |

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV102416BLL)

| Range | Ambient Temperature | V _{DD} (10 ns) |
|------------|---------------------|-------------------------|
| Automotive | -40°C to +125°C | 2.4V-3.6V |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 3.3V \pm 5\%$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------|----------------------------------|---------------------------------------------------|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{DD} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$ | 2.4 | — | V |
| V_{OL} | Output LOW Voltage | $V_{DD} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$ | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | -1 | 1 | μA |

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 2.4V-3.6V$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------|----------------------------------|---------------------------------------------------|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$ | 1.8 | — | V |
| V_{OL} | Output LOW Voltage | $V_{DD} = \text{Min.}, I_{OL} = 1.0 \text{ mA}$ | — | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.0 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | -1 | 1 | μA |

Note:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 1.65V-2.2V$

| Symbol | Parameter | Test Conditions | V_{DD} | Min. | Max. | Unit |
|----------------|---------------------|---------------------------------------------------|-----------|------|----------------|---------------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$ | 1.65-2.2V | 1.4 | — | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 0.1 \text{ mA}$ | 1.65-2.2V | — | 0.2 | V |
| V_{IH} | Input HIGH Voltage | | 1.65-2.2V | 1.4 | $V_{DD} + 0.2$ | V |
| $V_{IL}^{(1)}$ | Input LOW Voltage | | 1.65-2.2V | -0.2 | 0.4 | V |
| I_{LI} | Input Leakage | $GND \leq V_{IN} \leq V_{DD}$ | | -1 | 1 | μA |
| I_{LO} | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled | | -1 | 1 | μA |

Notes:

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$ (pulse width -2.0ns). Not 100% tested.
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$ (pulse width -2.0ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

| Parameter | Unit (2.4V-3.6V) | Unit (3.3V ± 5%) | Unit (1.65V-2.2V) |
|-----------------------------------------------------------|-----------------------|-----------------------|-----------------------|
| Input Pulse Level | 0.4V to $V_{DD}-0.3V$ | 0.4V to $V_{DD}-0.3V$ | 0.4V to $V_{DD}-0.2V$ |
| Input Rise and Fall Times | 1.5ns | 1.5ns | 1.5ns |
| Input and Output Timing and Reference Level (V_{Ref}) | $V_{DD}/2$ | $V_{DD}/2 + 0.05$ | $V_{DD}/2$ |
| Output Load | See Figures 1 and 2 | See Figures 1 and 2 | See Figures 1 and 2 |

AC TEST LOADS

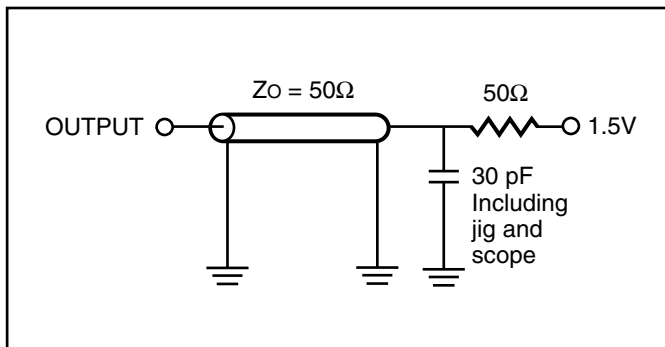


Figure 1.

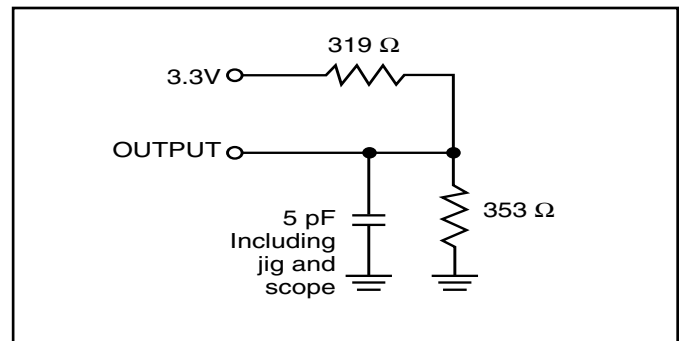


Figure 2.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 | | -10 | | -20 | | Unit |
|------------------|--------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} V _{IN} = 0.4V or V _{DD} - 0.3V | Com. | — | 110 | — | 90 | — | 50 | mA |
| | | | Ind. | — | 115 | — | 95 | — | 60 | |
| | | | Auto. | — | — | — | 140 | — | 100 | |
| | | | typ. ⁽²⁾ | | | 60 | | | | |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = 0 V _{IN} = 0.4V or V _{DD} - 0.3V | Com. | — | 85 | — | 85 | — | 45 | mA |
| | | | Ind. | — | 90 | — | 90 | — | 55 | |
| | | | Auto. | — | — | — | 110 | — | 90 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0 | Com. | — | 30 | — | 30 | — | 30 | mA |
| | | | Ind. | — | 35 | — | 35 | — | 35 | |
| | | | Auto. | — | — | — | 70 | — | 70 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 20 | — | 20 | — | 20 | mA |
| | | | Ind. | — | 25 | — | 25 | — | 25 | |
| | | | Auto. | — | — | — | 60 | — | 60 | |
| | | | typ. ⁽²⁾ | | | 4 | | | | |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|----------------------------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | ns |
| t _{OHA} | Output Hold Time | 2.5 | — | 2.5 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 8 | — | 10 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 5.5 | — | 6.5 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | — | 3 | — | 4 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | 0 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 3 | 0 | 4 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 3 | — | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 5.5 | — | 6.5 | ns |
| t _{HZB⁽²⁾} | \overline{LB} , \overline{UB} to High-Z Output | 0 | 3 | 0 | 3 | ns |
| t _{LZB⁽²⁾} | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | 0 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 8 | — | 10 | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

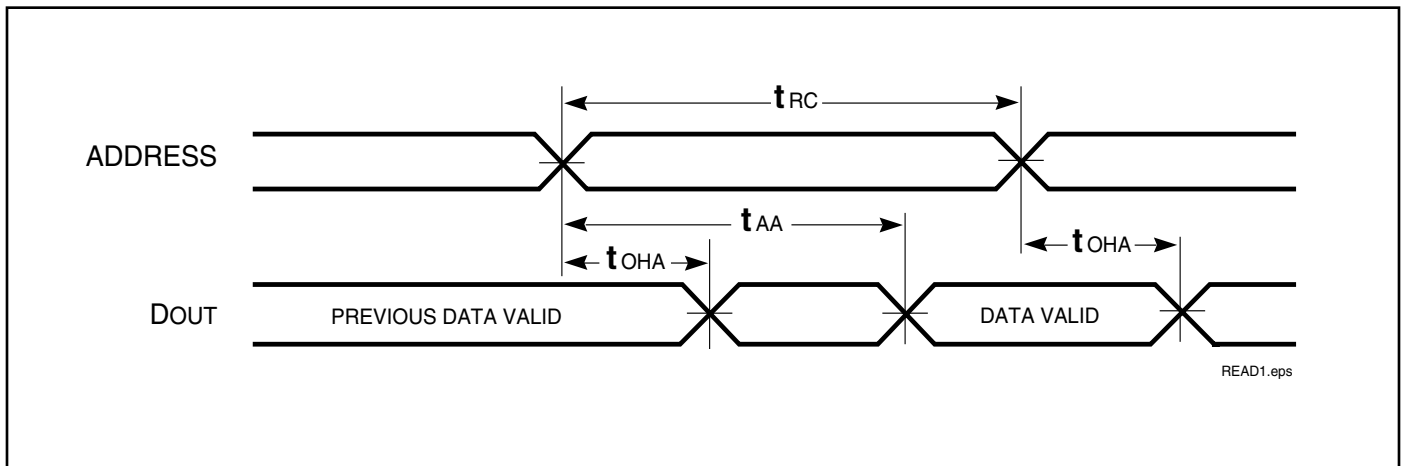
| Symbol | Parameter | -20 ns | | Unit |
|---------------------------------|----------------------------------------------------|--------|------|------|
| | | Min. | Max. | |
| t _{RC} | Read Cycle Time | 20 | — | ns |
| t _{AA} | Address Access Time | — | 20 | ns |
| t _{OHA} | Output Hold Time | 2.5 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 20 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 8 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | 0 | 8 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 8 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 8 | ns |
| t _{HZB} | \overline{LB} , \overline{UB} to High-Z Output | 0 | 8 | ns |
| t _{LZB} | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | ns |

Notes:

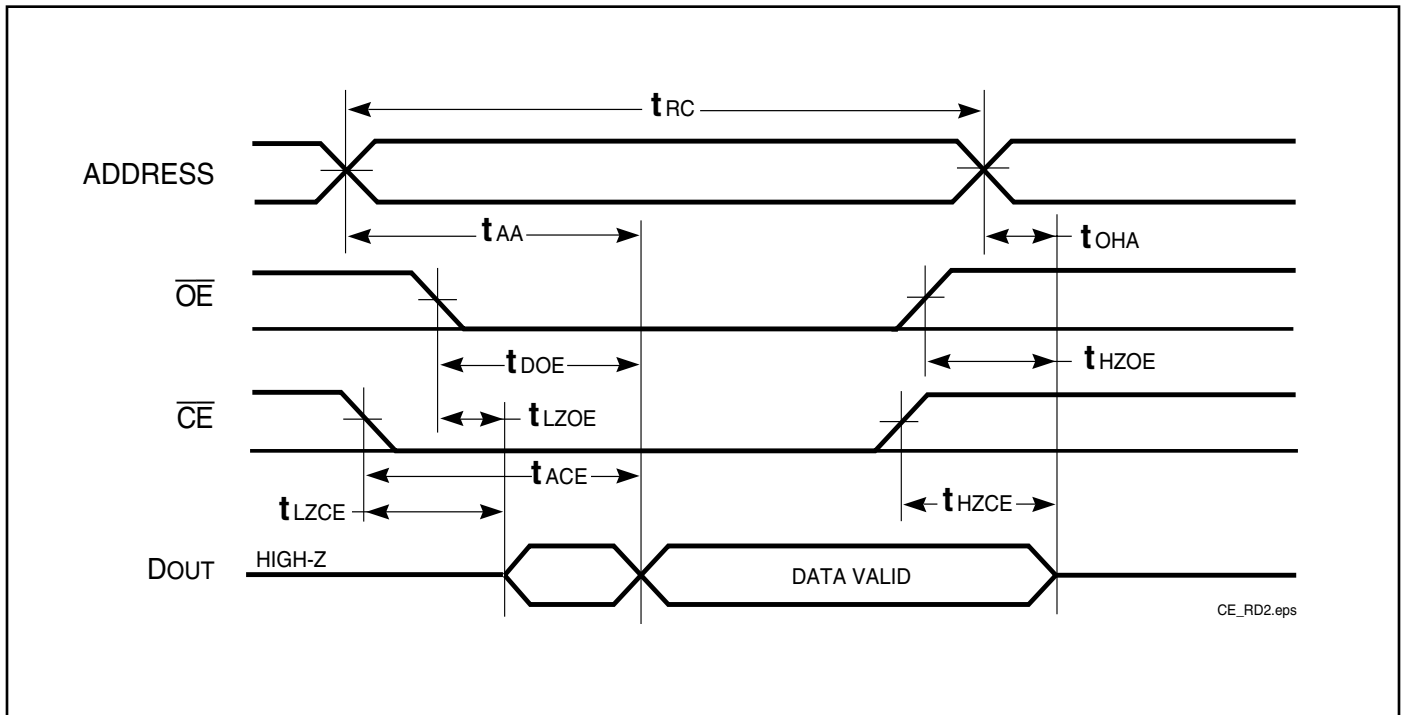
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) (\overline{CE} and \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|--------------------------------------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 6.5 | — | 8 | — | ns |
| t _{AW} | Address Setup Time to Write End | 6.5 | — | 8 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{PWB} | \overline{LB} , \overline{UB} Valid to End of Write | 6.5 | — | 8 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width | 6.5 | — | 8 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width ($\overline{OE} = \text{LOW}$) | 8.0 | — | 10 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 3.5 | — | 5 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 2 | — | 2 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and UB or LB, and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

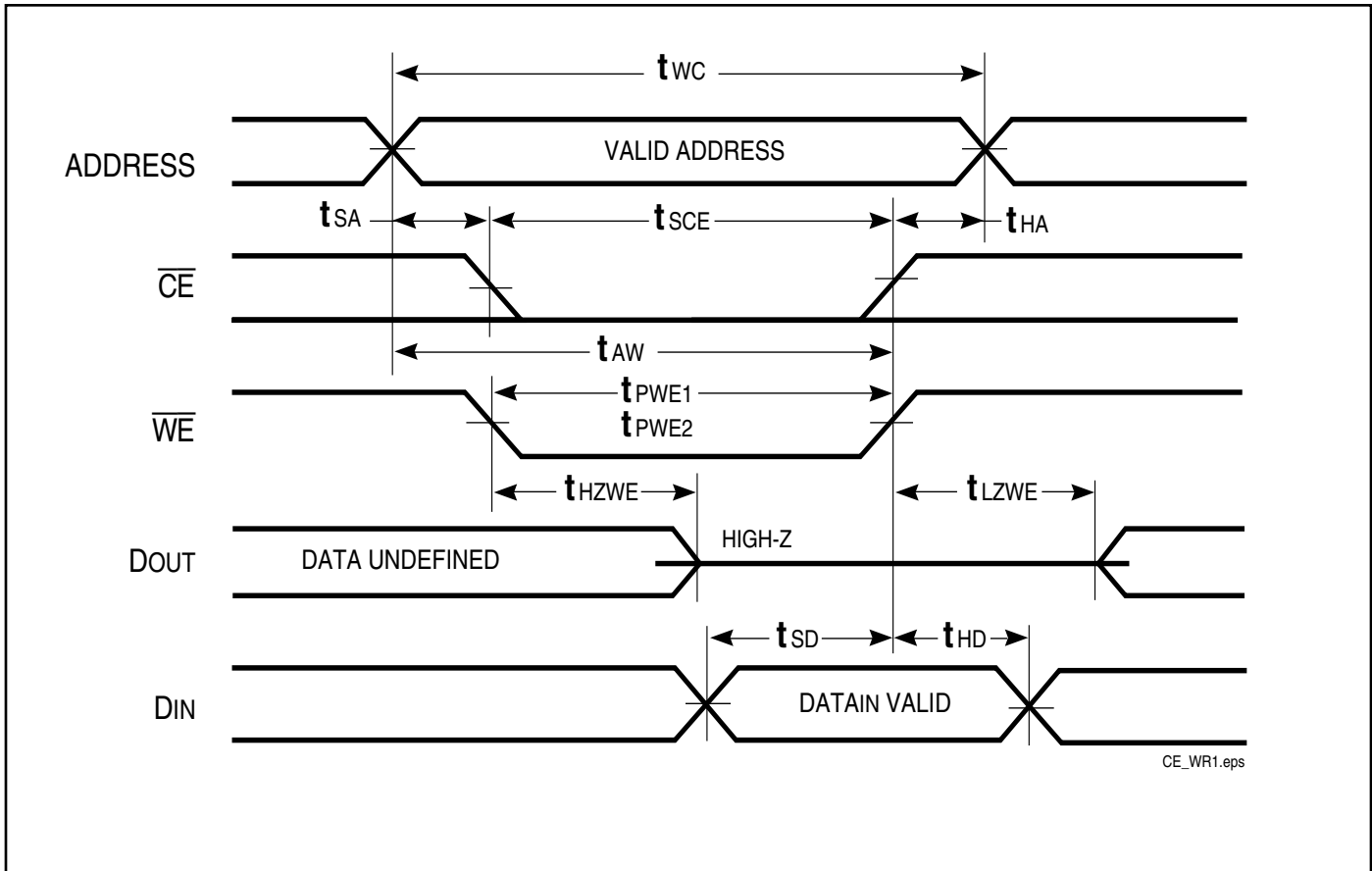
| Symbol | Parameter | -20 ns | | Unit |
|---------------------------------|---------------------------------------------------------|--------|------|------|
| | | Min. | Max. | |
| t _{WC} | Write Cycle Time | 20 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 12 | — | ns |
| t _{AW} | Address Setup Time to Write End | 12 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | ns |
| t _{PWB} | \overline{LB} , \overline{UB} Valid to End of Write | 12 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 12 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 17 | — | ns |
| t _{SD} | Data Setup to Write End | 9 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | ns |
| t _{HZWE⁽³⁾} | \overline{WE} LOW to High-Z Output | — | 9 | ns |
| t _{LZWE⁽³⁾} | \overline{WE} HIGH to Low-Z Output | 3 | — | ns |

Notes:

1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

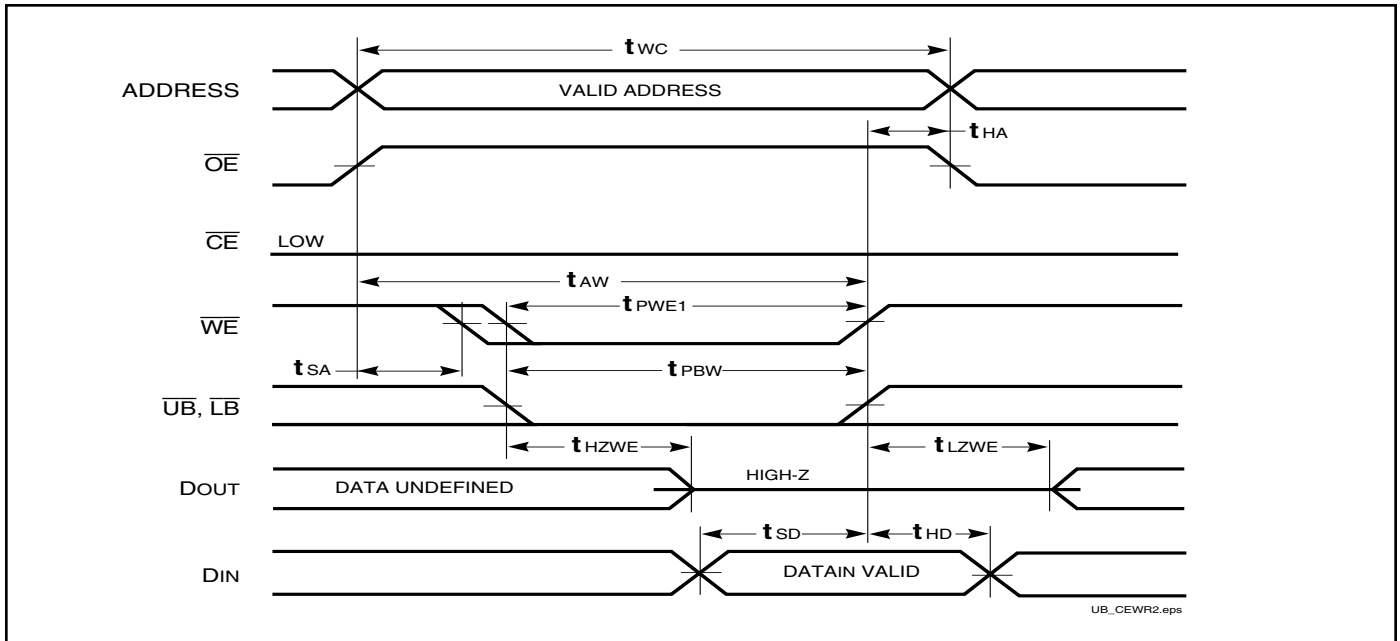
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)

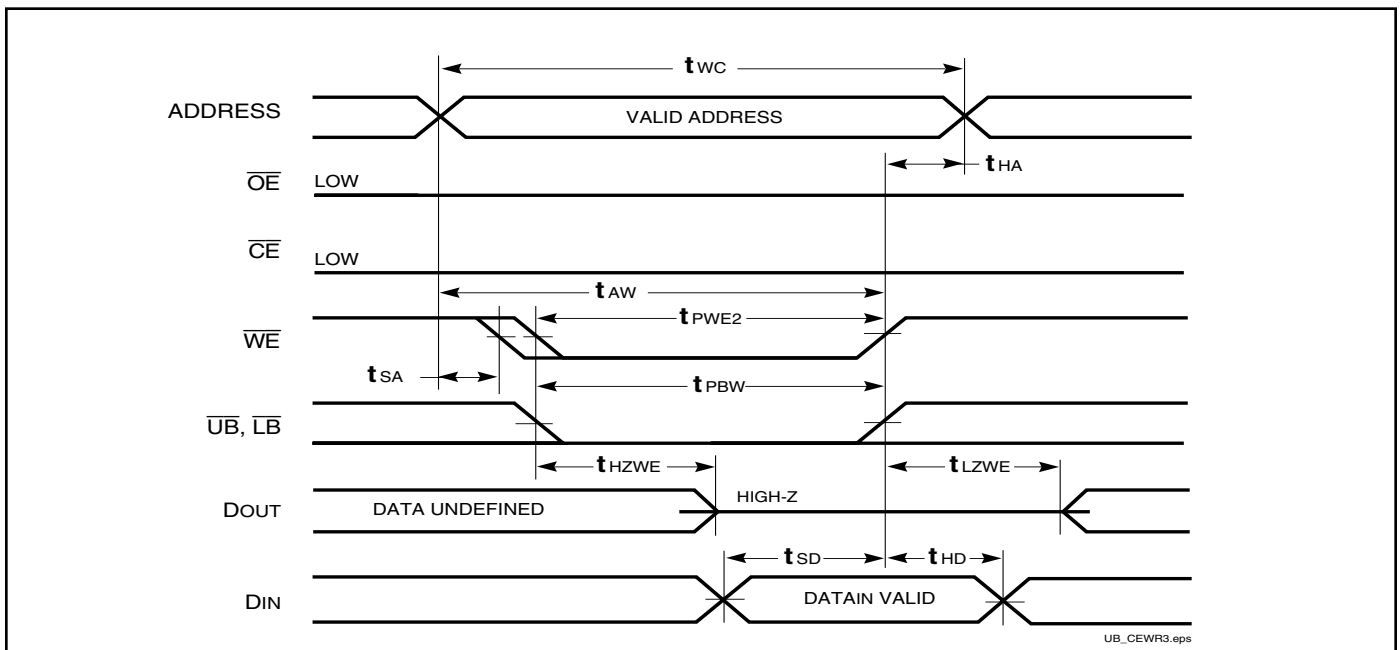


AC WAVEFORMS

WRITE CYCLE NO. 2 (\overline{WE} Controlled. \overline{OE} is HIGH During Write Cycle) ^(1,2)

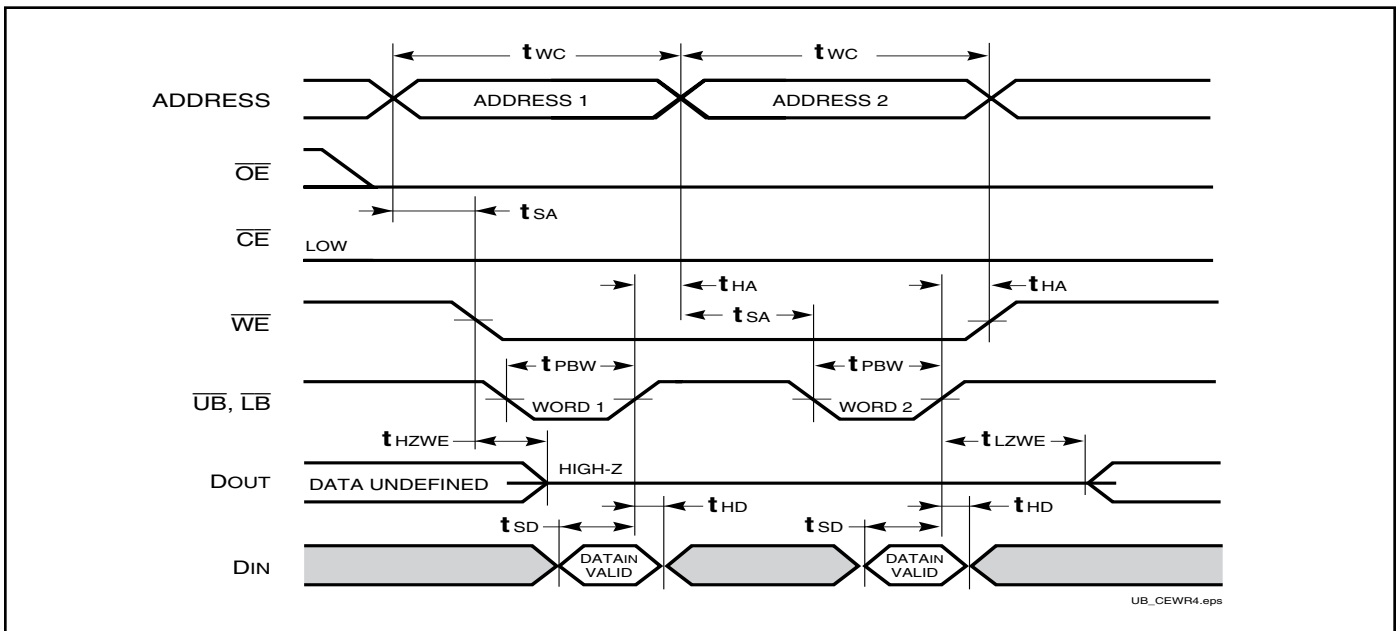


WRITE CYCLE NO. 3 (\overline{WE} Controlled. \overline{OE} is LOW During Write Cycle) ⁽¹⁾



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write) ^(1,3)



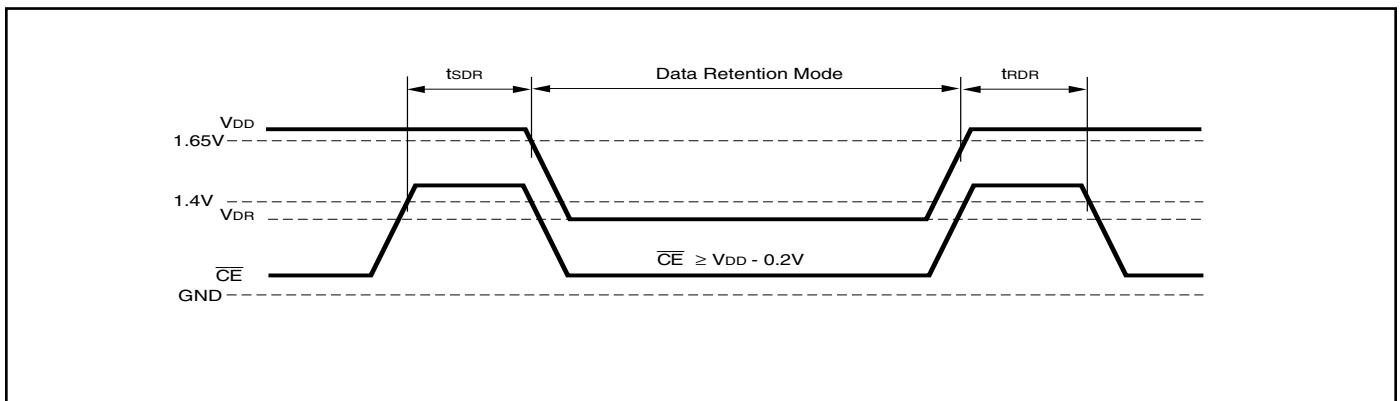
Notes:

1. The internal Write time is defined by the overlap of $\overline{\text{CE}} = \text{LOW}$, $\overline{\text{UB}}$ and/or $\overline{\text{LB}} = \text{LOW}$, and $\overline{\text{WE}} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{\text{OE}}$ HIGH for a minimum of 4 ns before $\overline{\text{WE}} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. $\overline{\text{WE}}$ may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|-----------|-----------------------------|---------------------------------------------------|---------------|----------|------|
| V_{DR} | V_{DD} for Data Retention | See Data Retention Waveform | 1.2 | 3.6 | V |
| I_{DR} | Data Retention Current | $V_{DD} = 1.2V, \overline{CE} \geq V_{DD} - 0.2V$ | Ind. Auto. | 20 50 | mA |
| t_{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | — | ns |
| t_{RDR} | Recovery Time | See Data Retention Waveform | t_{RC} | — | ns |

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|----------------------|-----------------------|-------------------------------------|
| 10 (8 ¹) | IS61WV102416BLL-10MI | 48 mini BGA (9mm x 11mm) |
| | IS61WV102416BLL-10MLI | 48 mini BGA (9mm x 11mm), Lead-free |
| | IS61WV102416BLL-10TLI | TSOP (Type I), Lead-free |

Note:

1. Speed = 8ns for $V_{DD} = 3.3V \pm 5\%$. Speed = 10ns for $V_{DD} = 2.4V - 3.6V$

Industrial Range: -40°C to +85°C

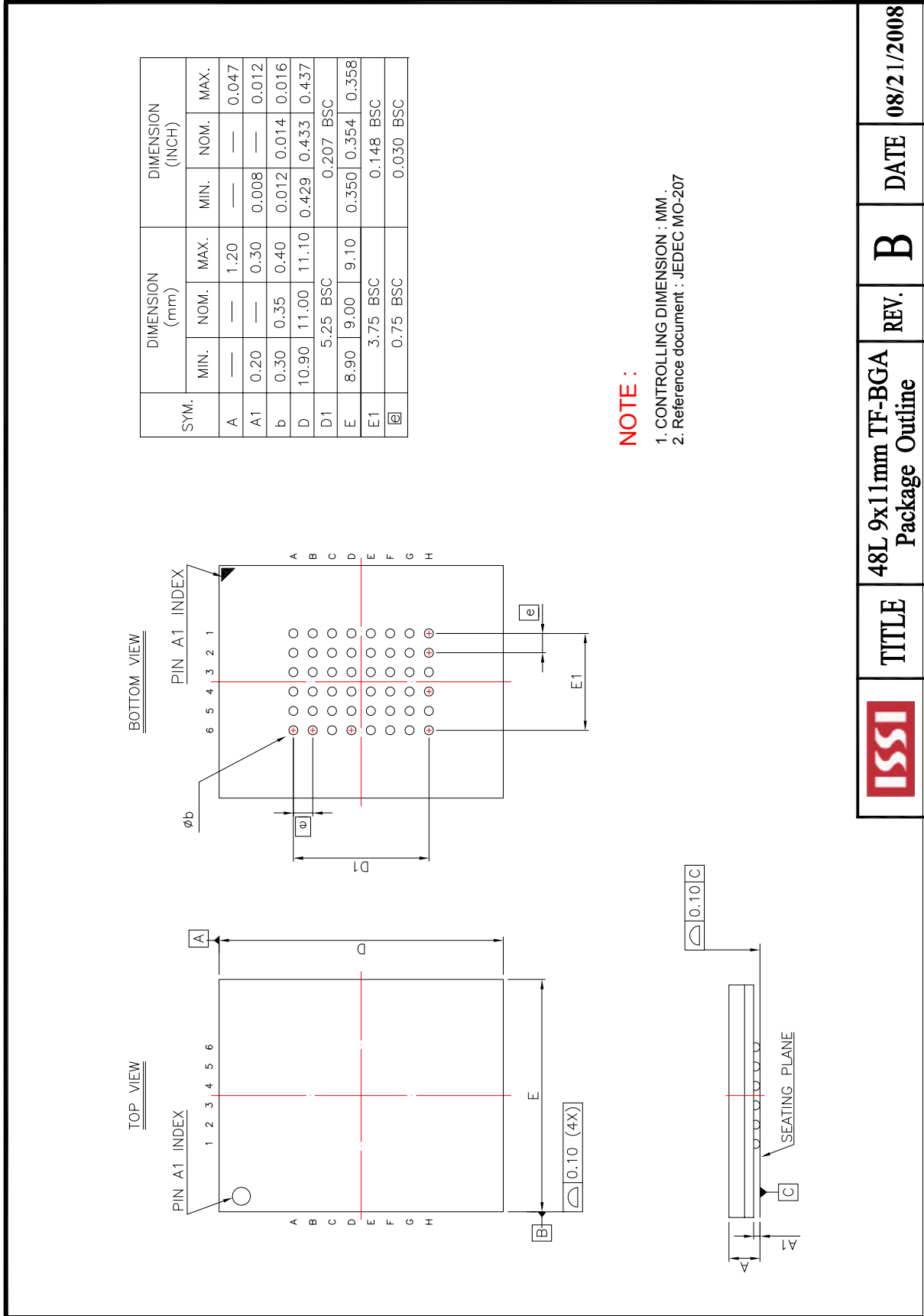
Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|------------|-----------------------|--------------------------|
| 20 | IS61WV102416ALL-20MI | 48 mini BGA (9mm x 11mm) |
| | IS61WV102416ALL-20TLI | TSOP (Type I), Lead-free |

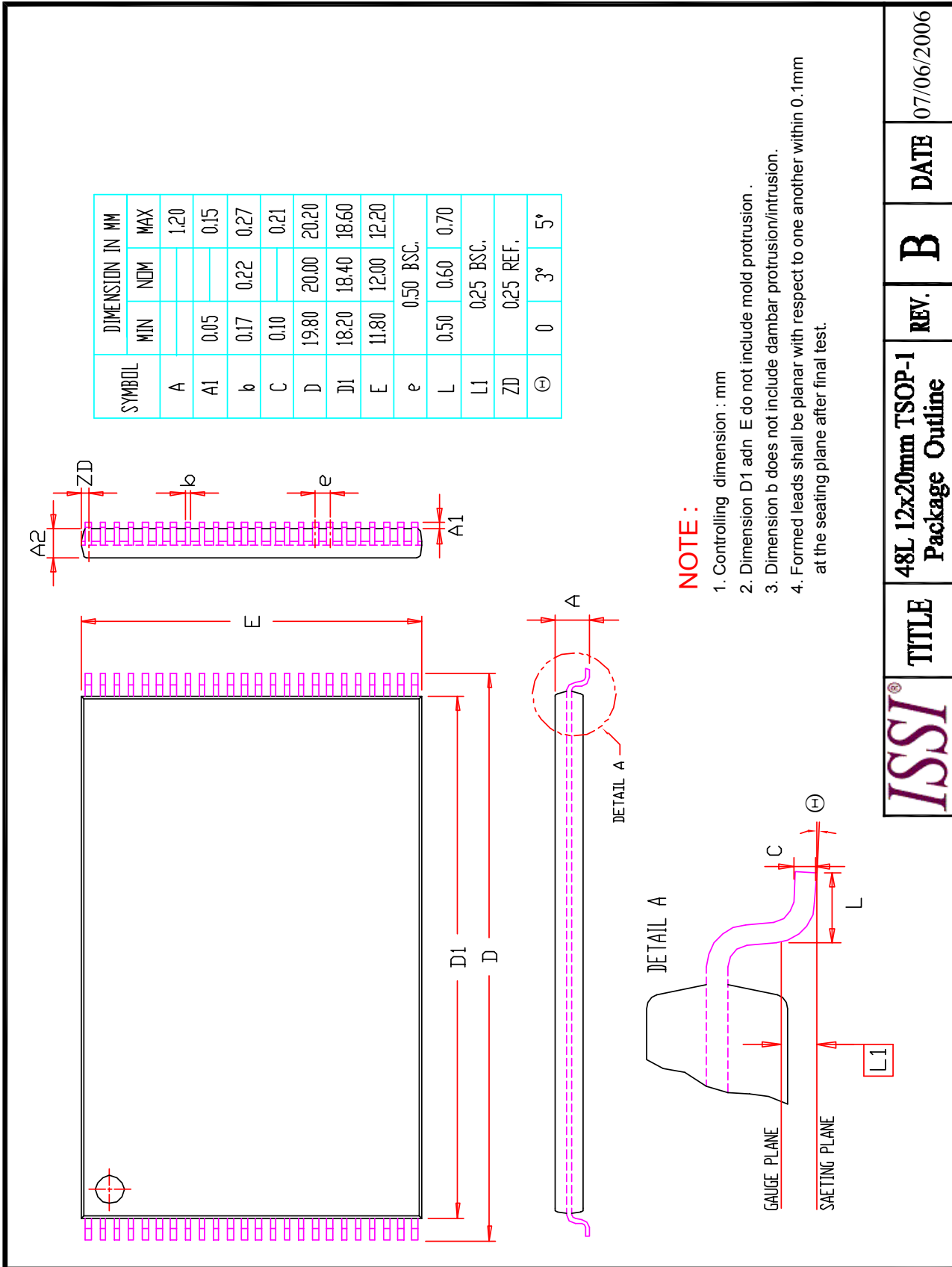
Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|------------|-------------------------|--------------------------------------------|
| 10 | IS64WV102416BLL-10MA3 | 48 mini BGA (9mm x 11mm) |
| | IS64WV102416BLL-10MLA3 | 48 mini BGA (9mm x 11mm), Lead-free |
| | IS64WV102416BLL-10CTLA3 | TSOP (Type I), Copper Leadframe, Lead-free |



| | | | | | | |
|--|--------------|--------------------------------------|-------------|----------|-------------|------------|
| | TITLE | 48L 9x11mm TF-BGA Package Outline | REV. | B | DATE | 08/21/2008 |
|--|--------------|--------------------------------------|-------------|----------|-------------|------------|



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| ISSI | TITLE | REV. | DATE |
| | 48L 12x20mm TSOP-1 Package Outline | B | 07/06/2006 |

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