5th-Order, Lowpass, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

V_DD to GND ....-0.3V to +6V
IN, OUT, COM, OS, CLK, $\overline{\text{SHDN}}$ ....-0.3V to (V_DD + 0.3V)
OUT Short-Circuit Duration..1sec
Continuous Power Dissipation (T_A = +70°C)
    8-Pin DIP (derate 9.09mW/°C above +70°C)...............727mW
    8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW

Operating Temperature Ranges
    MAX74 _ _C_A ....0°C to +70°C
    MAX74 _ _E_A ....-40°C to +85°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX7409/MAX7410

(V_DD = +5V, filter output measured at OUT, 10kΩ ∥ 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{\text{SHDN}}$ = V_DD, f_CLK = 100kHz, T_A = T_MIN to T_MAX, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C	(Note 1)			0.001 to 15		kHz
Clock-to-Corner Ratio	f_{CLK} / f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_DD - 0.25	V
Output Offset Voltage	V_{OFFSET}	$V_{IN} = V_{COM} = V_{DD} / 2$			±4	±25	mV
DC Insertion Gain with Output Offset Removed		$V_{COM} = V_{DD} / 2$ (Note 2)		-0.2	0	0.2	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 4Vp-p, measurement bandwidth = 22kHz	MAX7409		-85		dB
			MAX7410		-78		
Offset Voltage Gain	A_{OS}	OS to OUT			1		V/V
COM Voltage Range	V_{COM}	Input, COM externally driven		2.0	2.5	3.0	V
		Output, COM unconnected		2.3	2.5	2.7	
Input Voltage Range at OS	V_{OS}	Input, OS externally driven			V_{COM} ±0.1		V
Input Resistance at COM	R_{COM}			110	180		kΩ
Clock Feedthrough					5		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Output Load Drive	C_L			50	500		pF
Input Leakage Current at COM		$\overline{\text{SHDN}}$ = GND, V_{COM} = 0 to V_DD			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to V_DD			±0.1	±10	µA
CLOCK							
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 3)		21	30	38	kHz
Clock Output Current (Internal Oscillator Mode)	I_{CLK}	V_{CLK} = 0 or 5V			±13.5	±20	µA
Clock Input High	V_{IH}			4.5			V
Clock Input Low	V_{IL}					0.5	V

MAXIM

ELECTRICAL CHARACTERISTICS—MAX7409/MAX7410

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Operating mode, no load		1.2	1.5	mA
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	IN = COM (Note 4)		70		dB
SHUTDOWN						
$\overline{SHDN}$ Input High	V_{SDH}		4.5			V
$\overline{SHDN}$ Input Low	V_{SDL}				0.5	V
$\overline{SHDN}$ Input Leakage Current		V $\overline{SHDN}$ = 0 to V_{DD}		±0.2	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7413/MAX7414

(V_{DD} = +3V, filter output measured at OUT pin, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C	(Note 1)			0.001 to 15		kHz
Clock-to-Corner Ratio	f_{CLK} / f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	V_{IN} = V_{COM} = V_{DD} / 2			±4	±25	mV
DC Insertion Gain with Output Offset Removed		V_{COM} = V_{DD} / 2 (Note 2)		-0.2	0	+0.2	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 2.5Vp-p, measurement bandwidth = 22kHz	MAX7413		-83		dB
			MAX7414		-81		
Offset Voltage Gain	A_{OS}	OS to OUT			1		V/V
COM Voltage Range	V_{COM}	Input, COM externally driven		1.4	1.5	1.6	V
		Output, COM unconnected		1.4	1.5	1.6	V
Input Voltage Range at OS	V_{OS}	Input, OS externally driven			V_{COM} ±0.1		V
Input Resistance at COM	R_{COM}			110	180		kΩ
Clock Feedthrough					3		mVp-p
Resistance Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Output Load Drive	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to V_{DD}			±0.1	±10	µA

5th-Order, Lowpass,
Switched-Capacitor Filters

ELECTRICAL CHARACTERISTICS—MAX7413/MAX7414 (continued)

(V$_{DD}$ = +3V, filter output measured at OUT pin, 10kΩ ‖ 50pF load to GND at OUT, OS = COM, 0.1µF capacitor from COM to GND, $\overline{SHDN}$ = V$_{DD}$, f$_{CLK}$ = 100kHz, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK						
Internal Oscillator Frequency	f$_{OSC}$	C$_{OSC}$ = 1000pF (Note 3)	21	30	38	kHz
Clock Output Current (Internal Oscillator Mode)	I$_{CLK}$	V$_{CLK}$ = 0 or 3V		±13.5	±20	µA
Clock Input High	V$_{IH}$		2.5			V
Clock Input Low	V$_{IL}$				0.5	V
POWER REQUIREMENTS						
Supply Voltage	V$_{DD}$		2.7		3.6	V
Supply Current	I$_{DD}$	Operating mode, no load		1.2	1.5	mA
Shutdown Current	I$_{\overline{SHDN}}$	$\overline{SHDN}$ = GND		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	IN = COM (Note 4)		70		dB
SHUTDOWN						
$\overline{SHDN}$ Input High	V$_{SDH}$		2.5			V
$\overline{SHDN}$ Input Low	V$_{SDL}$				0.5	V
$\overline{SHDN}$ Input Leakage Current		V$_{\overline{SHDN}}$ = 0 to V$_{DD}$		0.2	±10	µA

FILTER CHARACTERISTICS

(V$_{DD}$ = +5V for MAX7409/MAX7410, V$_{DD}$ = +3V for MAX7413/MAX7414, filter output measured at OUT, 10kΩ ‖ 50pF load to GND at OUT, $\overline{SHDN}$ = V$_{DD}$, f$_{CLK}$ = 100kHz, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BESSEL FILTERS—MAX7409/MAX7413					
Insertion Gain Relative to DC Gain	f$_{IN}$ = 0.5f$_C$	-1	-0.74		dB
	f$_{IN}$ = f$_C$	-3.6	-3.0	-2.4	
	f$_{IN}$ = 4f$_C$		-41.0	-35	
	f$_{IN}$ = 7f$_C$		-64.3	-58	
BUTTERWORTH FILTERS—MAX7410/MAX7414					
Insertion Gain Relative to DC Gain	f$_{IN}$ = 0.5f$_C$	-0.3	0		dB
	f$_{IN}$ = f$_C$	-3.6	-3.0	-2.4	
	f$_{IN}$ = 3f$_C$		-47.5	-43	
	f$_{IN}$ = 5f$_C$		-70	-65	

Note 1: The maximum f$_C$ is defined as the clock frequency f$_{CLK}$ = 100 x f$_C$ at which the peak S / (THD+N) drops to 68dB with a sinusoidal input at 0.2f$_C$.

Note 2: DC insertion gain is defined as ΔV$_{OUT}$ / ΔV$_{IN}$.

Note 3: f$_{OSC}$ (kHz) ≅ 30 x 10^3 / C$_{OSC}$ (pF).

Note 4: PSRR is the change in output voltage from a V$_{DD}$ of 4.5V and a V$_{DD}$ of 5.5V.

MAXIM

5th-Order, Lowpass, Switched-Capacitor Filters

Typical Operating Characteristics

(V_{DD} = +5V for MAX7409/MAX7410, V_{DD} = +3V for MAX7413/MAX7414, f_{CLK} = 100kHz, $\overline{SHDN}$ = V_{DD}, COM = OS = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)
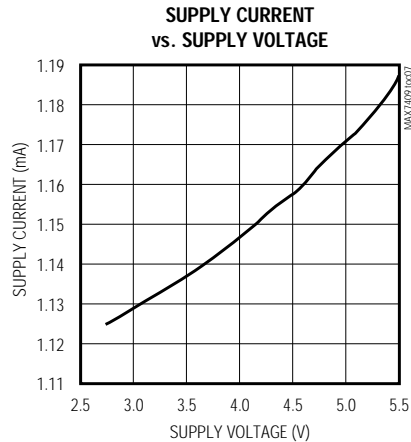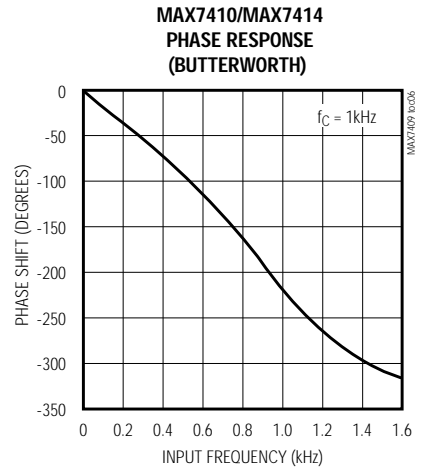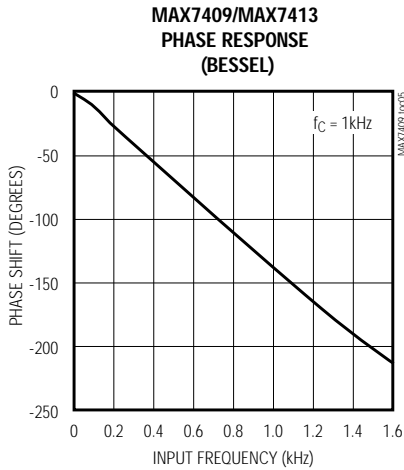
MAX7409/MAX7413 FREQUENCY RESPONSE (BESSEL)

MAX7410/MAX7414 FREQUENCY RESPONSE (BUTTERWORTH)

MAX7409/MAX7413 PASSBAND FREQUENCY RESPONSE (BESSEL)

MAX7410/MAX7414 PASSBAND FREQUENCY RESPONSE (BUTTERWORTH)

MAX7409/MAX7413 PHASE RESPONSE (BESSEL)

MAX7410/MAX7414 PHASE RESPONSE (BUTTERWORTH)
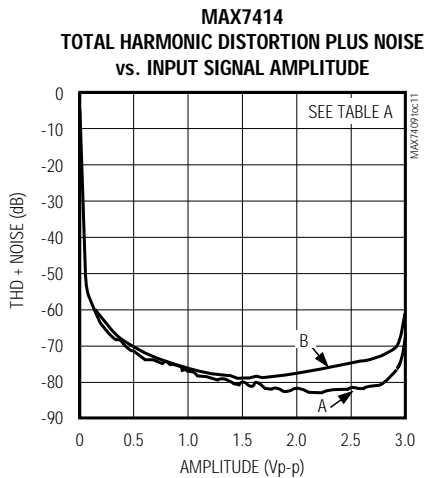

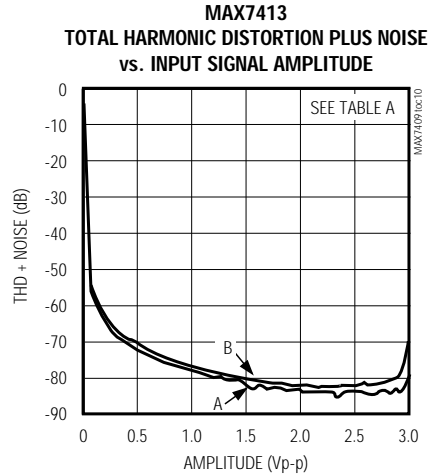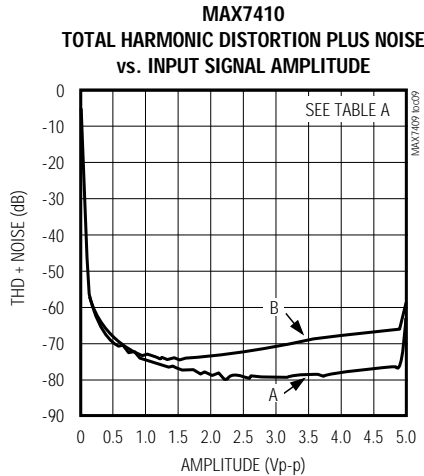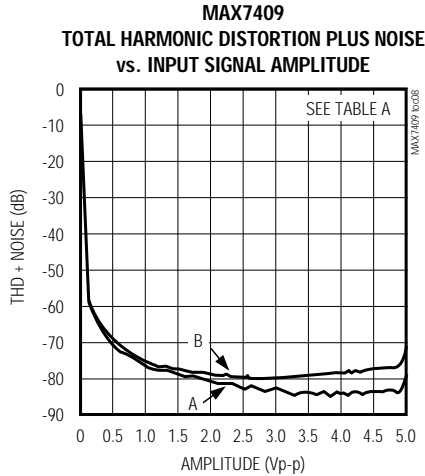**SUPPLY CURRENT vs. SUPPLY VOLTAGE**
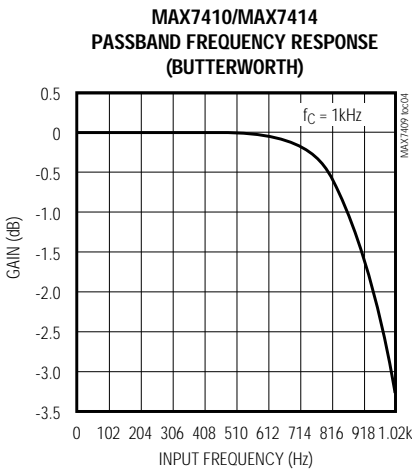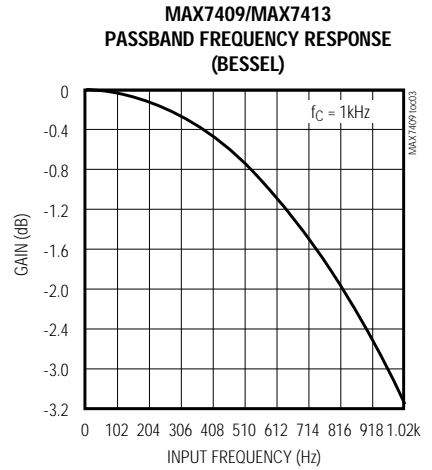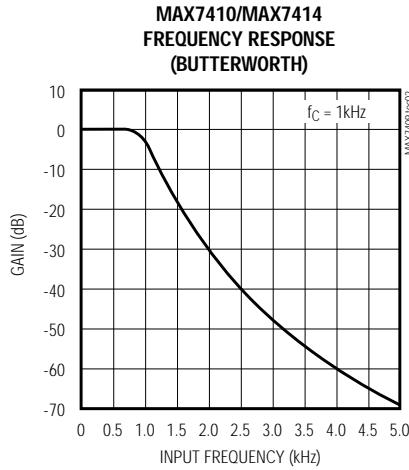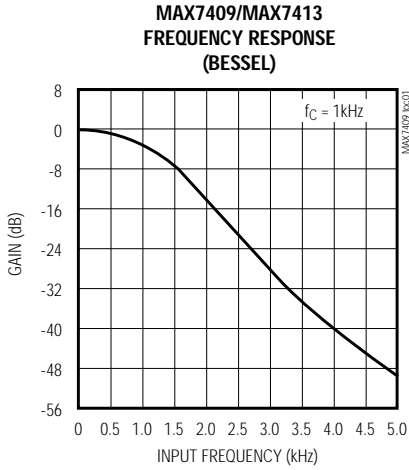
Table A. THD+N vs. Input Signal Amplitude Plot Characteristics

LABEL	f_{IN} (Hz)	f_C (kHz)	f_{CLK} (kHz)	MEASUREMENT BANDWIDTH (kHz)
A	200	1	100	22
B	1k	5	500	80

5th-Order, Lowpass, Switched-Capacitor Filters

_____Typical Operating Characteristics (continued)

(V_DD = +5V for MAX7409/MAX7410, V_DD = +3V for MAX7413/MAX7414, f_CLK = 100kHz, SHDN = V_DD, COM = OS = V_DD / 2, T_A = +25°C, unless otherwise noted.)

MAX7409
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. INPUT SIGNAL AMPLITUDE

MAX7410
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. INPUT SIGNAL AMPLITUDE

MAX7413
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. INPUT SIGNAL AMPLITUDE

MAX7414
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. INPUT SIGNAL AMPLITUDE

SUPPLY CURRENT vs. TEMPERATURE

INTERNAL OSCILLATOR PERIOD
vs. SMALL CAPACITANCE

INTERNAL OSCILLATOR PERIOD
vs. LARGE CAPACITANCE

INTERNAL OSCILLATOR FREQUENCY
vs. SUPPLY VOLTAGE

INTERNAL OSCILLATOR FREQUENCY
vs. TEMPERATURE

MAXIM

_____Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7409/MAX7410, V_{DD} = +3V for MAX7413/MAX7414, f_{CLK} = 100kHz, $\overline{SHDN}$ = V_{DD}, COM = OS = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)
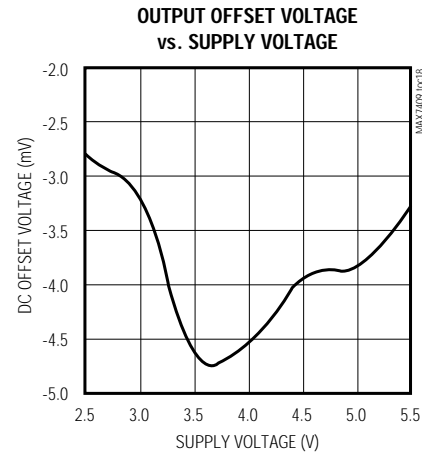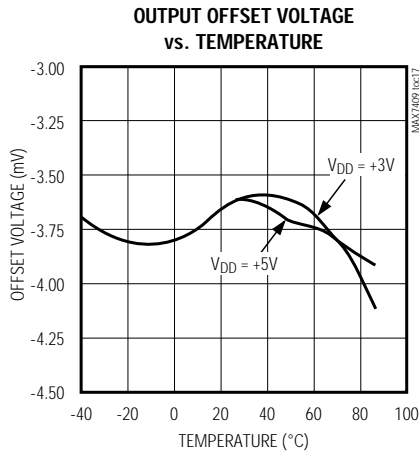
OUTPUT OFFSET VOLTAGE
vs. TEMPERATURE

OUTPUT OFFSET VOLTAGE
vs. SUPPLY VOLTAGE
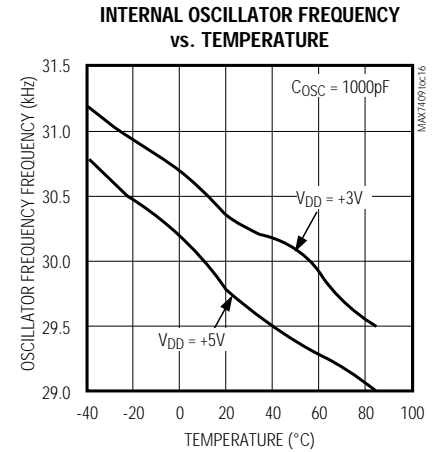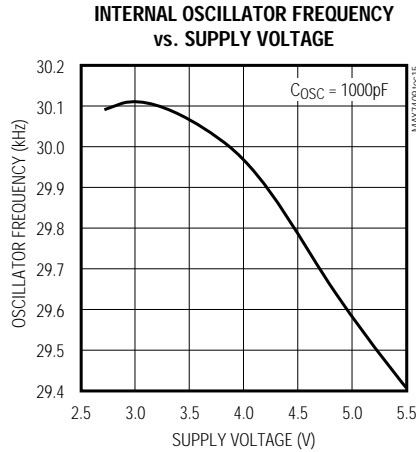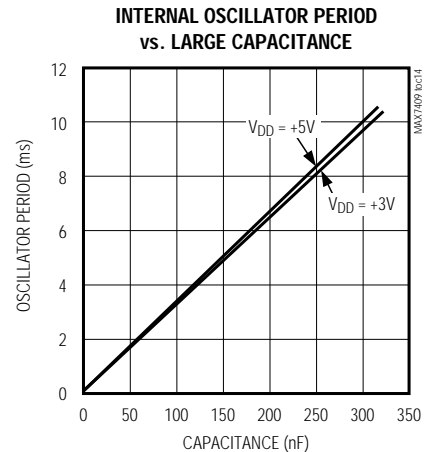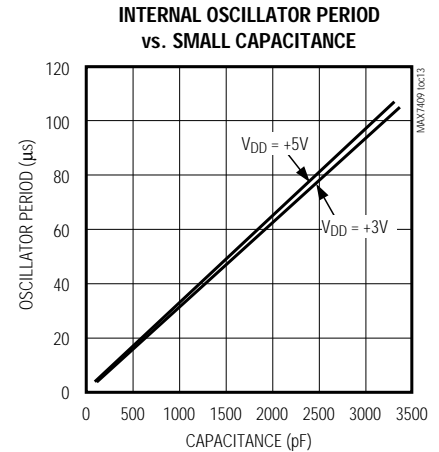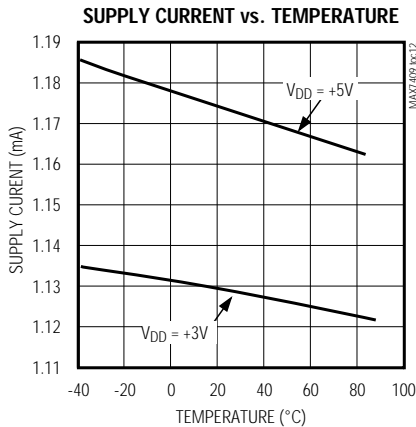
_____Pin Description

PIN	NAME	FUNCTION
1	COM	Common Input Pin. Biased internally at midsupply. Bypass COM externally to GND with a 0.1μF capacitor. To override internal biasing, drive COM with an external supply.
2	IN	Filter Input
3	GND	Ground
4	V_{DD}	Positive Supply Input: +5V for MAX7409/MAX7410, +3V for MAX7413/MAX7414.
5	OUT	Filter Output
6	OS	Offset Adjust Input. To adjust output offset, connect OS to an external supply through a resistive voltage-divider (Figure 3). Connect OS to COM if no offset adjustment is needed. Refer to the *Offset and Common-Mode Input Adjustment* section.
7	$\overline{SHDN}$	Shutdown Input. Drive low to enable shutdown mode; drive high or connect to V_{DD} for normal operation.
8	CLK	Clock Input. Connect an external capacitor (C_{OSC}) from CLK to ground: f_{OSC} (kHz) = 30 x 10^3 / C_{OSC} (pF). To override the internal oscillator, connect CLK to an external clock: f_C = f_{CLK} /100.

_____Detailed Description

The MAX7409/MAX7413 Bessel filters provide low over-shoot and fast settling responses, and the MAX7410/MAX7414 Butterworth filters provide a maximally flat passband response. All parts operate with a 100:1 clock-to-corner frequency ratio and a 15kHz maximum corner frequency.

Bessel Characteristics

Lowpass Bessel filters such as the MAX7409/MAX7413 delay all frequency components equally, preserving the shape of step inputs (subject to the attenuation of the higher frequencies). Bessel filters settle quickly—an important characteristic in applications that use a multiplexer (mux) to select an input signal for an analog-to-digital converter (ADC). An anti-aliasing filter placed between the mux and the ADC must settle quickly after a new channel is selected.

Butterworth Characteristics

Lowpass Butterworth filters such as the MAX7410/MAX7414 provide a maximally flat passband response, making them ideal for instrumentation applications that require minimum deviation from the DC gain throughout the passband.
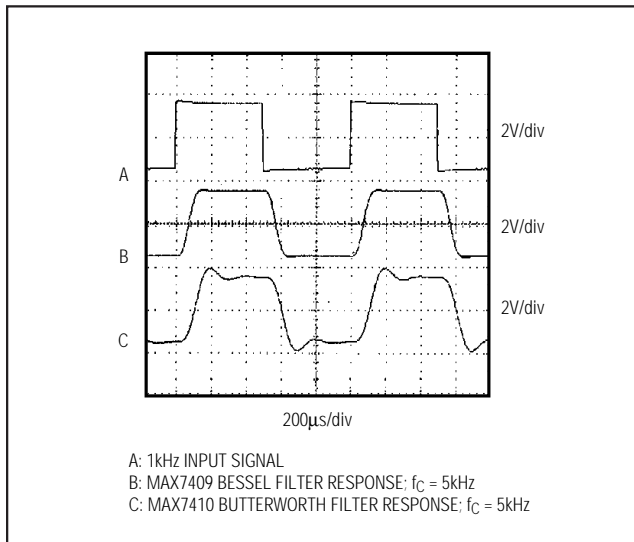
MAX7409/MAX7410/MAX7413/MAX7414

Figure 1. Bessel vs. Butterworth Filter Response

The difference between Bessel and Butterworth filters can be observed when a 1kHz square wave is applied to the filter input (Figure 1, trace A). With the filter cutoff frequencies set at 5kHz, trace B shows the Bessel filter response and trace C shows the Butterworth filter response.

Background Information
Most switched-capacitor filters (SCFs) are designed with biquadratic sections. Each section implements two filtering poles, and the sections are cascaded to produce higher-order filters. The advantage to this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high. An alternative approach is to emulate a passive network using switched-capacitor integrators with summing and scaling. Figure 2 shows a basic 5th-order ladder filter structure.

A switched-capacitor filter such as the MAX7409/MAX7410/MAX7413/MAX7414 emulates a passive ladder filter. The filter's component sensitivity is low when compared to a cascaded biquad design, because each component affects the entire filter shape, not just one pole-zero pair. In other words, a mismatched component in a biquad design will have a concentrated error on its respective poles, while the same mismatch in a ladder filter design results in an error distributed over all poles.
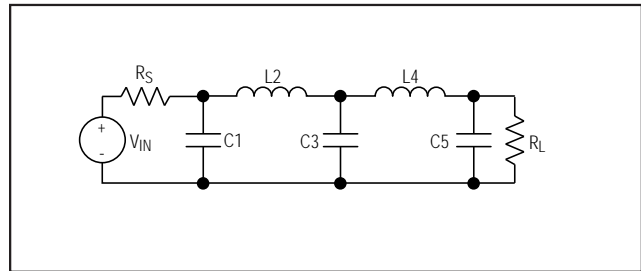

Figure 2. 5th-Order Ladder Filter Network

Clock Signal
External Clock
The MAX7409/MAX7410/MAX7413/MAX7414 family of SCFs is designed for use with external clocks that have a 50% ±10% duty cycle. When using an external clock with these devices, drive CLK with a CMOS gate powered from 0 to V_{DD}. Varying the rate of the external clock adjusts the corner frequency of the filter as follows:

$$f_C = f_{CLK} / 100$$

Internal Clock
When using the internal oscillator, connect a capacitor (C_{OSC}) between CLK and ground. The value of the capacitor determines the oscillator frequency as follows:

$$f_{OSC} (kHz) = 30 \times 10^3 / C_{OSC} (pF)$$

Minimize the stray capacitance at CLK so that it does not affect the internal oscillator frequency. Vary the rate of the internal oscillator to adjust the filter's corner frequency by a 100:1 clock-to-corner frequency ratio. For example, an internal oscillator frequency of 100kHz produces a nominal corner frequency of 1kHz.

Input Impedance vs. Clock Frequencies
The MAX7409/MAX7410/MAX7413/MAX7414's input impedance is effectively that of a switched-capacitor resistor (see the following equation), and is inversely proportional to frequency. The input impedance values determined below represent the average input impedance, since the input current is not continuous. As a rule, use a driver with an output impedance less than 10% of the filter's input impedance. Estimate the input impedance of the filter using the following formula:

$$Z_{IN} = 1 / (f_{CLK} \times 2.1pF)$$

For example, an f_{CLK} of 100kHz results in an input impedance of 4.8MΩ.

MAXIM

Low-Power Shutdown Mode

These devices feature a shutdown mode that is activated by driving $\overline{SHDN}$ low. In shutdown mode, the filter's supply current reduces to 0.2μA and its output becomes high impedance. For normal operation, drive $\overline{SHDN}$ high or connect it to V_{DD}.

_____Applications Information

Offset and Common-Mode Input Adjustment

The COM pin sets the common-mode input voltage and is biased at mid-supply with an internal resistor-divider. If the application does not require offset adjustment, connect OS to COM. For applications requiring offset adjustment, apply an external bias voltage through a resistor-divider network to OS such as shown in Figure 3. For applications that require DC level shifting, adjust OS with respect to COM. (Note: OS should not be left unconnected.) The output voltage is represented by this equation:

$$V_{OUT} = (V_{IN} - V_{COM}) + V_{OS}$$

with $V_{COM} = V_{DD} / 2$ (typical), and where $(V_{IN} - V_{COM})$ is lowpass filtered by the SCF, and OS is added at the output stage. See the _Electrical Characteristics_ for the voltage range of COM and OS. Changing the voltage on COM or OS significantly from midsupply reduces the filter's dynamic range.

Power Supplies

The MAX7409/MAX7410 operate from a single +5V supply and the MAX7413/MAX7414 operate from a single +3V supply. Bypass V_{DD} to GND with a 0.1μF capacitor. If dual supplies are required (±2.5V for MAX7409/MAX7410, ±1.5V for MAX7413/MAX7414), connect COM to system ground and connect GND to the negative supply. Figure 4 shows an example of dual-supply operation. Single- and dual-supply performance are equivalent. For either single- or dual-supply operation, drive CLK and $\overline{SHDN}$ from GND (V- in dual-supply operation) to V_{DD}. For ±5V dual-supply applications, use the MAX291–MAX297.

Input Signal Amplitude Range

The optimal input signal range is determined by observing the voltage level at which the Total Harmonic Distortion + Noise is minimized for a given corner frequency. The _Typical Operating Characteristics_ show graphs of the devices' Total Harmonic Distortion plus Noise Response as the input signal's peak-to-peak amplitude is varied.
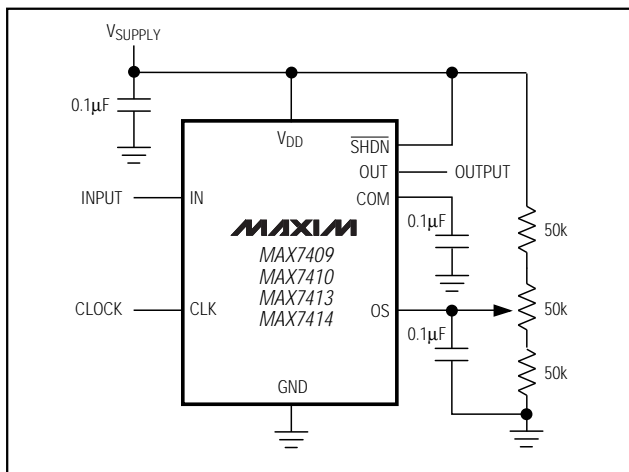

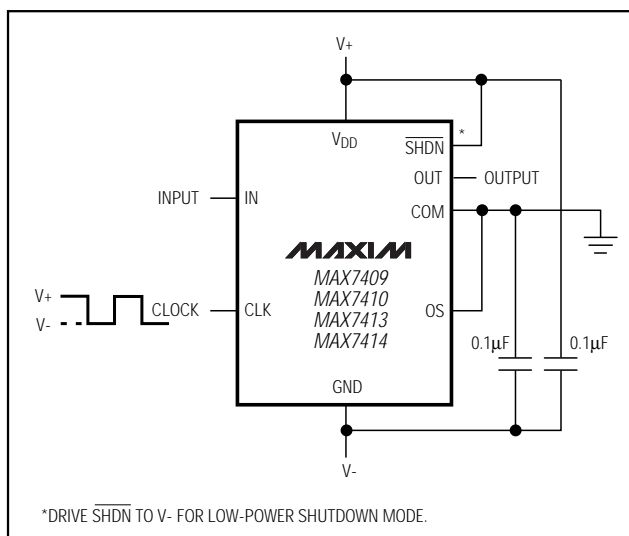Figure 3. Offset Adjustment Circuit

*DRIVE $\overline{SHDN}$ TO V- FOR LOW-POWER SHUTDOWN MODE.

Figure 4. Dual-Supply Operation

Anti-Aliasing and DAC Postfiltering

When using these devices for anti-aliasing or DAC postfiltering, synchronize the DAC (or ADC) and the filter clocks. If the clocks are not synchronized, beat frequencies will alias into the desired passband.

Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 1 lists typical harmonic-distortion values for the MAX7410/MAX7414 with a 10kΩ load at T_A = +25°C. Table 2 lists typical harmonic-distortion values for the MAX7409/MAX7413 with a 10kΩ load at T_A = +25°C.

5th-Order, Lowpass, Switched-Capacitor Filters

Table 1. MAX7410/MAX7414 Typical Harmonic Distortion

FILTER	f$_{CLK}$ (kHz)	f$_{IN}$ (Hz)	V$_{IN}$ (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
				2nd	3rd	4th	5th
MAX7410	500	1k	4	-85	-67	-86.7	-82
	100	200		-84	-78	-88.7	-88.5
MAX7414	500	1k	2	-85.3	-74	-87.1	-87.6
	100	200		-86.1	-85.5	-85.8	-86.4

Table 2. MAX7409/MAX7413 Typical Harmonic Distortion

FILTER	f$_{CLK}$ (kHz)	f$_{IN}$ (Hz)	V$_{IN}$ (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
				2nd	3rd	4th	5th
MAX7409	500	1k	4	-82.5	-79	-88.8	-91.1
	100	200		-83.5	-85.4	-88.4	-88.8
MAX7413	500	1k	2	-86	-81	-87.3	-87.9
	100	200		-86.4	-86.9	-87.9	-88.3

__Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX7413CUA	0°C to +70°C	8 µMAX
MAX7413CPA	0°C to +70°C	8 Plastic DIP
MAX7413EUA	-40°C to +85°C	8 µMAX
MAX7413EPA	-40°C to +85°C	8 Plastic DIP
MAX7414CUA	0°C to +70°C	8 µMAX
MAX7414CPA	0°C to +70°C	8 Plastic DIP
MAX7414EUA	-40°C to +85°C	8 µMAX
MAX7414EPA	-40°C to +85°C	8 Plastic DIP

_____Chip Information

TRANSISTOR COUNT: 1457

MAXIM

Package Information
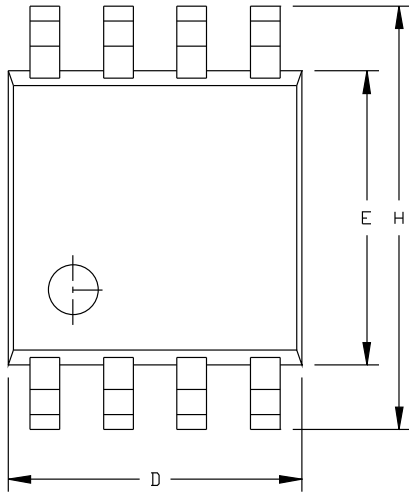
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
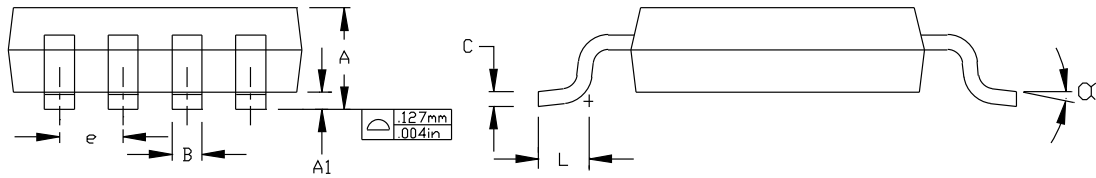
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION

TITLE:
8LD uMAX PACKAGE OUTLINE DWG.

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	D	1/1

8LUMAXD.EPS

MAX7409/MAX7410/MAX7413/MAX7414

MAXIM _____ 11

MAX7409/MAX7410/MAX7413/MAX7414

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM
120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300"
TITLE

1/1

21-0043 A
DOCUMENT CONTROL NUMBER REV

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Maxim Integrated](#):

MAX7409CPA+ MAX7409CUA+ MAX7409CUA+T MAX7409EPA+ MAX7409EUA+T MAX7410CPA+
MAX7410CUA+ MAX7410CUA+T MAX7410EPA+ MAX7410EUA+T MAX7413CPA+ MAX7413CUA+
MAX7413CUA+T MAX7413EPA+ MAX7413EUA+T MAX7414CPA+ MAX7414CUA+ MAX7414CUA+T
MAX7414EPA+ MAX7414EUA+T MAX7410EUA+ MAX7413EUA+ MAX7414EUA+ MAX7409EUA+