

uPSD32xx

Table 1. Device Summary

Part Number	Max Clock (MHz)	1st Flash (bytes)	2nd Flash (bytes)	SRAM (bytes)	GPIO	USB	8032 Bus	V _{CC} (V)	Pkg.	Temp.
uPSD3212C-40T6	40	64K	16K	2K	37	No	No	4.5-5.5	TQFP52	-40°C to 85°C
uPSD3212CV-24T6	24	64K	16K	2K	37	No	No	3.0-3.6	TQFP52	-40°C to 85°C
uPSD3212C-40U6	40	64K	16K	2K	46	No	Yes	4.5-5.5	TQFP80	-40°C to 85°C
uPSD3212CV-24U6	24	64K	16K	2K	46	No	Yes	3.0-3.6	TQFP80	-40°C to 85°C
uPSD3233B-40T6	40	128K	32K	8K	37	No	No	4.5-5.5	TQFP52	-40°C to 85°C
uPSD3233BV-24T6	24	128K	32K	8K	37	No	No	3.0-3.6	TQFP52	-40°C to 85°C
uPSD3233B-40U6	40	128K	32K	8K	46	No	Yes	4.5-5.5	TQFP80	-40°C to 85°C
uPSD3233BV-24U6	24	128K	32K	8K	46	No	Yes	3.0-3.6	TQFP80	-40°C to 85°C
uPSD3234A-40T6	40	256K	32K	8K	37	Yes	No	4.5-5.5	TQFP52	-40°C to 85°C
uPSD3234A-40U6	40	256K	32K	8K	46	Yes	Yes	4.5-5.5	TQFP80	-40°C to 85°C
uPSD3234BV-24U6	24	256K	32K	8K	46	No	Yes	3.0-3.6	TQFP80	-40°C to 85°C
uPSD3253B-40T6	40	128K	32K	32K	37	No	No	4.5-5.5	TQFP52	-40°C to 85°C
uPSD3253BV-24T6	24	128K	32K	32K	37	No	No	3.0-3.6	TQFP52	-40°C to 85°C
uPSD3254BV-24U6	24	256K	32K	32K	46	No	Yes	3.0-3.6	TQFP80	-40°C to 85°C
uPSD3254A-40T6	40	256K	32K	32K	37	Yes	No	4.5-5.5	TQFP52	-40°C to 85°C
uPSD3254A-40U6	40	256K	32K	32K	46	Yes	Yes	4.5-5.5	TQFP80	-40°C to 85°C

SUMMARY DESCRIPTION

The uPSD32xx Series combines a fast 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix including USB, to form an ideal embedded controller. At its core is an industry-standard 8032 MCU operating up to 40MHz.

A JTAG serial interface is used for In-System Programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development.

The USB 1.1 low-speed interface has one Control endpoint and two Interrupt endpoints suitable for HID class drivers.

The 8032 core is coupled to Programmable System Device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64K bytes using on-chip programmable decode logic.

Dual Flash memory banks provide a robust solution for remote product updates in the field through In-Application Programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips.

General purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSD-soft Express, available from the web at www.st.com/psm, at no charge.

The uPSD32xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

Figure 2. Block Diagram

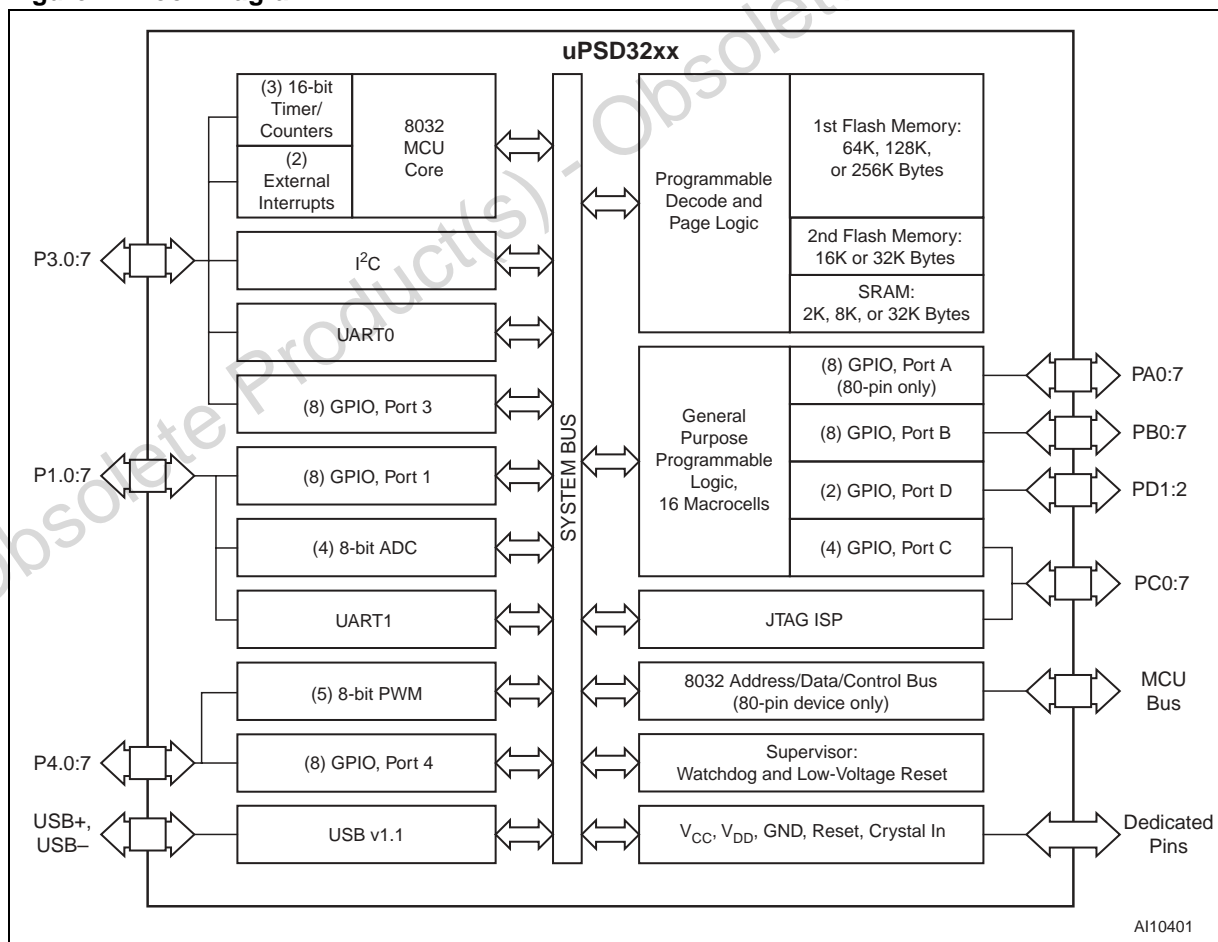
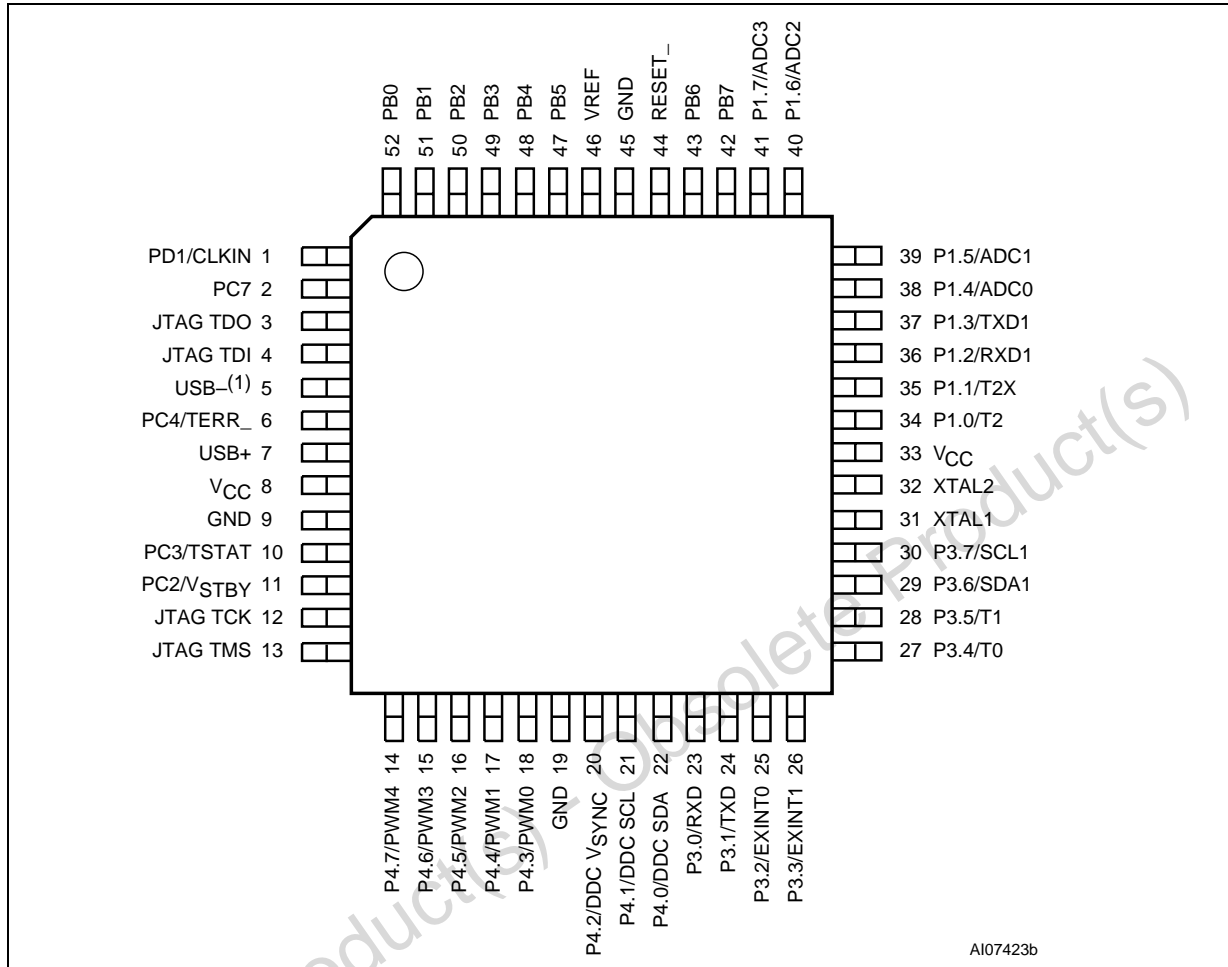
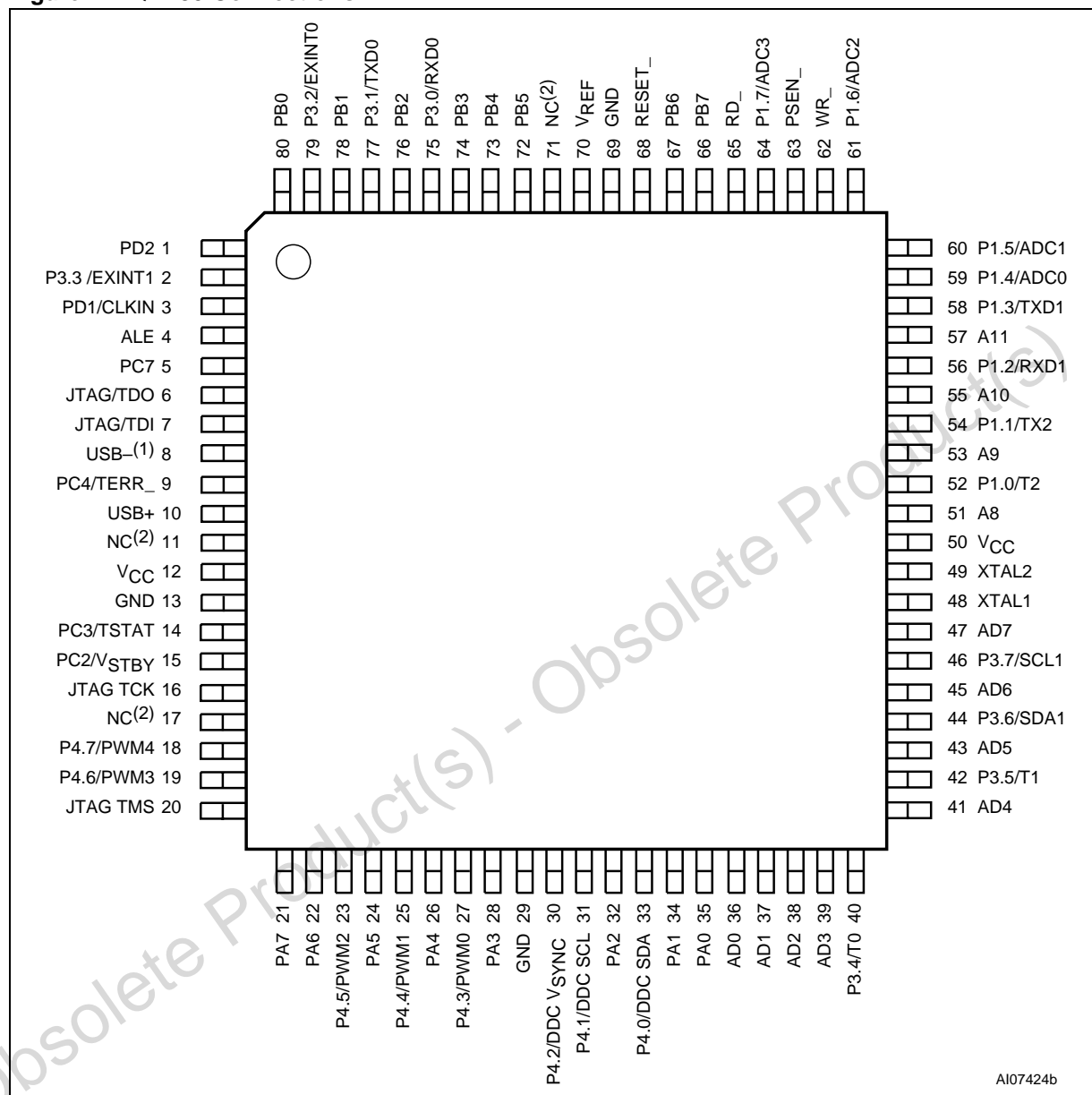


Figure 3. TQFP52 Connections



Note: 1. Pull-up resistor required on pin 5 (2kΩ for 3V devices, 7.5kΩ for 5V devices).

Figure 4. TQFP80 Connections



Note: 1. Pull-up resistor required on pin 8 (2kΩ for 3V devices, 7.5kΩ for 5V devices).
 2. NC = Not Connected.

Table 2. Major Parameters

Parameters/Conditions/ Comments	5V Test Conditions	5.0V Value	3.3V Test Conditions	3.3V Value	Unit
Operating Voltage	–	4.5 to 5.5	–	3.0 to 3.6	V
Operating Temperature	–	–40 to 85	–	–40 to 85	°C
MCU Frequency 12MHz (min) for USB; 8MHz (min) for I ² C	–	1 Min, 40 Max	–	1 Min, 24 Max	MHz
Active Current, Typical (25°C operation; 80% Flash and 15% SRAM accesses, 45 PLD product terms used; PLD Turbo mode Off)	24MHz MCU clock, 12MHz PLD input frequency, 4MHz ALE	72	12MHz MCU clock, 6MHz PLD input frequency, 2MHz ALE	21	mA
Idle Current, Typical (CPU halted but some peripherals active; 25°C operation; 45 PLD product terms used; PLD Turbo mode Off)	24MHz MCU clock, 12MHz PLD input frequency	25	12MHz MCU clock, 1MHz PLD input frequency	7	mA
Standby Current, Typical (Power-down Mode, requires reset to exit mode; without Low-Voltage Detect (LVD) Supervisor)	180µA with LVD	110	100µA with LVD	60	µA
SRAM Backup Current, Typical (If external battery is attached.)	–	0.5	–	0.5	µA
I/O Sink/Source Current Ports A, B, C, and D	V _{OL} = 0.25V (max); V _{OH} = 3.9V (min)	I _{OL} = 8 (max); I _{OH} = –2 (min)	V _{OL} = 0.15V (max); V _{OH} = 2.6V (min)	I _{OL} = 4 (max); I _{OH} = –1 (min)	mA
PLD Macrocells (For registered or combinatorial logic)	–	16	–	16	–
PLD Inputs (Inputs from pins, macrocell feedback, or MCU addresses)	–	69	–	69	–
PLD Outputs (Output to pins or internal feedback)	–	16	–	16	–
PLD Propagation Delay, Typical (PLD input to output, Turbo Mode)	–	15	–	22	ns

PART NUMBERING

Table 3. Ordering Information Scheme

Example:	uPSD	3	2	1	2	C	V	-	24	U	6	T
Device Type uPSD = Microcontroller PSD												
Family 3 = 8032 core												
PLD Size 2 = 16 Macrocells												
SRAM Size 1 = 2K bytes 3 = 8K bytes 5 = 32K bytes												
Main Flash Memory Size 2 = 64K bytes 3 = 128K bytes 4 = 256K bytes												
IP Mix A = USB, I ² C, PWM, DDC, ADC, (2) UARTs, Supervisor (Reset Out, Reset In, LVD, WD) B = I ² C, PWM, DDC, ADC, (2) UARTs, Supervisor (Reset Out, Reset In, LVD, WD) C = I ² C, PWM, ADC, (2) UARTs, Supervisor (Reset Out, Reset In, LVD, WD)												
Operating Voltage blank = V _{CC} = 4.5 to 5.5V V = V _{CC} = 3.0 to 3.6V												
Speed -24 = 24MHz -40 = 40MHz												
Package T = 52-pin TQFP U = 80-pin TQFP												
Temperature Range 6 = -40 to 85°C												
Shipping Option T = Tape and Reel Packing												

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

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