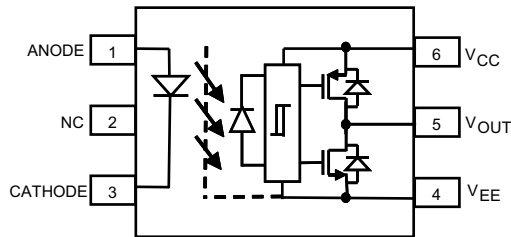


Functional Diagram



NOTE: A 1- μ F bypass capacitor must be connected between pins V_{CC} and V_{EE} .

Truth Table

LED	$V_{CC} - V_{EE}$ Positive Going (Turn-On)	V_{CC} to V_{EE} Negative Going (Turn-Off)	V_O
OFF	0V to 20V	0V to 20V	LOW
ON	0V to 8.1V	0V to 7.1V	LOW
ON	8.1V to 9.1V	7.1V to 8.1V	TRANSITION
ON	9.1V to 20V	8.1V to 20V	HIGH

Ordering Information

ACPL-P345 is UL Recognized with 3750V_{RMS} for 1 minute per UL1577. ACPL-W345 is UL Recognized with 5000 V_{RMS} for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-P345	-000E	Stretched SO-6	X			100 per tube
ACPL-W345	-500E		X	X		1000 per reel
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

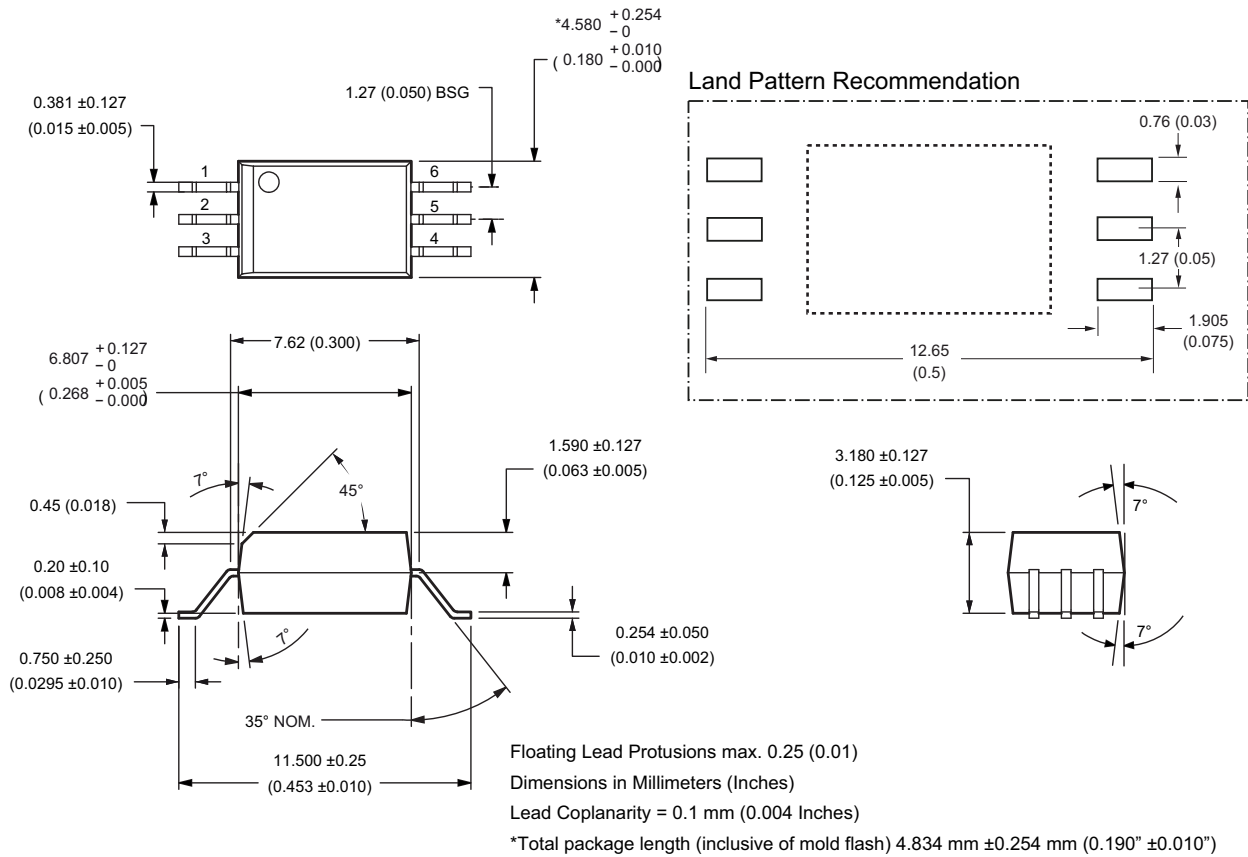
ACPL-P345-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACPL-W345-000E to order product of Stretched SO-6 Surface Mount package in Tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

ACPL-W345 Stretched SO-6 Package (8-mm Clearance)



Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-P345/W345 is approved by the following organizations.

UL	Recognized under UL 1577, component recognition program up to $V_{ISO} = 3750 V_{RMS}$ (ACPL-P345) and $V_{ISO} = 5000 V_{RMS}$ (ACPL-W345).
CSA	CSA Component Acceptance Notice #5, File CA 88324
IEC/EN/DIN EN 60747-5-5 (Option 060 Only)	Maximum Working Insulation Voltage $V_{IORM} = 891 V_{peak}$ (ACPL-P345) and $V_{IORM} = 1140 V_{peak}$ (ACPL-W345)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

Description	Symbol	ACPL-P345 Option 060	ACPL-W345 Option 060	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 450 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$ for rated mains voltage $\leq 1000 V_{RMS}$		I – IV I – IV I – III I – III	I – IV I – IV I – IV I – IV I – III	
Climatic Classification		40/105/21	40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{PEAK}
Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ second, Partial discharge < 5 pC	V_{PR}	1671	2137	V_{PEAK}
Input to Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10$ seconds, Partial discharge < 5 pC	V_{PR}	1426	1824	V_{PEAK}
Highest Allowable Overvoltage ^a (Transient Overvoltage $t_{ini} = 60$ seconds)	V_{IOTM}	6000	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S , $V_{IO} = 500$ V	R_S	$>10^9$	$>10^9$	Ω

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the *Broadcom Regulatory Guide to Isolation Circuits*, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Insulation and Safety-Related Specifications

Parameter	Symbol	ACPL-P345	ACPL-W345	Units	Conditions
Minimum External Air Gap (Clearance) ^a	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage) ^a	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance) ^a		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	V	DIN EN 60112 (2010-05)
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

a. All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J	—	125	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 μ s pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage	V_R	—	5	V	
“High” Peak Output Current	$I_{OH(PEAK)}$	—	1.0	A	b
“Low” Peak Output Current	$I_{OL(PEAK)}$	—	1.0	A	b
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	25	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
Output IC Power Dissipation	P_O	—	500	mW	c
Total Power Dissipation	P_T	—	550	mW	d

- Derate linearly above 85°C free-air temperature at a rate of 0.3 mA/°C.
- Maximum pulse width = 10 μ s. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.8A. See [Application Information](#) for additional details on limiting I_{OH} peak.
- Derate linearly above 85°C free-air temperature at a rate of 12.5 mW/°C.
- Derate linearly above 85°C free-air temperature at a rate of 13.75 mW/°C. The maximum LED junction temperature should not exceed 125°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_A	-40	+105	°C	
Output Supply Voltage	$(V_{CC} - V_{EE})$	10	20	V	
Input Current (ON)	$I_{F(ON)}$	7	11	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V	

Electrical Specifications (DC)

All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} - V_{EE} = 15\text{V}$, $V_{EE} = \text{Ground}$. All minimum and maximum specifications are at recommended operating conditions ($T_A = -40^\circ\text{C}$ to 105°C , $I_{F(ON)} = 7\text{ mA}$ to 11 mA , $V_{F(OFF)} = -3.6\text{V}$ to 0.8V , $V_{EE} = \text{Ground}$, $V_{CC} = 10\text{V}$ to 20V), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
High Level Peak Output Current	I_{OH}	-0.8	—	—	A	$V_{CC} - V_O = 10\text{V}$		a
Low Level Peak Output Current	I_{OL}	0.8	—	—	A	$V_O - V_{EE} = 10\text{V}$		a
High Level Output Voltage	V_{OH}	$V_{CC} - 0.3$	$V_{CC} - 0.2$	—	V	$I_O = -100\text{ mA}$, $I_F = 9\text{ mA}$	2, 4	b, c
High Level Output Voltage	V_{OH}	—	V_{CC}	—	V	$I_O = 0\text{ mA}$, $I_F = 9\text{ mA}$	1	
Low Level Output Voltage	V_{OL}	—	0.1	0.25	V	$I_O = 100\text{ mA}$	3	
High Level Supply Current	I_{CCH}	—	2.6	4.0	mA	$I_F = 9\text{ mA}$	10, 11	
Low Level Supply Current	I_{CCL}	—	2.6	4.0	mA	$V_F = 0\text{V}$		
Threshold Input Current Low to High	I_{FLH}	0.5	1.5	4.0	mA	$V_O > 5\text{ V}$	12, 13	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	$I_F = 9\text{ mA}$	13	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$	—	-1.7	—	mV/°C			
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	$I_R = 100\text{ }\mu\text{A}$		
Input Capacitance	C_{IN}	—	70	—	pF	$f = 1\text{ MHz}$, $V_F = 0\text{V}$		
UVLO Threshold	V_{UVLO+}	8.1	8.6	9.1	V	$V_O > 5\text{ V}$, $I_F = 9\text{ mA}$		
	V_{UVLO-}	7.1	7.6	8.1				
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0	—	V			

- Maximum pulse width = $10\text{ }\mu\text{s}$.
- In this test, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
- Maximum pulse width = 1 ms .

Switching Specifications (AC)

All typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} - V_{EE} = 10\text{V}$, $V_{EE} = \text{Ground}$. All minimum and maximum specifications are at recommended operating conditions ($T_A = -40^\circ\text{C}$ to 105°C , $I_{F(\text{ON})} = 7\text{ mA}$ to 11 mA , $V_{F(\text{OFF})} = -3.6\text{V}$ to 0.8V , $V_{EE} = \text{Ground}$), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	30	55	120	ns	$R_g = 10\Omega$, $C_g = 10\text{ nF}$, $f = 200\text{ kHz}$, Duty Cycle = 50%, $V_{CC} = 10\text{V}$	8, 9, 10, 11	
Propagation Delay Time to Low Output Level	t_{PHL}	30	55	120	ns			
Pulse Width Distortion	PWD	—	0	50	ns			a
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PHL} - t_{PLH}$)	-50	—	+50	ns			18, 19
Propagation Delay Skew	t_{PSK}	—	—	40	ns			c
Rise Time	t_R	—	8	30	ns	$C_g = 1\text{ nF}$, $f = 200\text{ kHz}$, Duty Cycle = 50%, $V_{CC} = 10\text{V}$	12, 14	
Fall Time	t_F	—	8	30	ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	100	—	—	kV/ μs	$T_A = 25^\circ\text{C}$, $I_F = 9\text{ mA}$, $V_{CC} = 20\text{V}$, $V_{CM} = 1500\text{V}$ with split resistors	15	d, e
Output Low Level Common Mode Transient Immunity	$ CM_L $	100	—	—	kV/ μs	$T_A = 25^\circ\text{C}$, $V_F = 0\text{V}$, $V_{CC} = 20\text{V}$, $V_{CM} = 1500\text{V}$ with split resistors		f

- The difference between t_{PHL} and t_{PLH} between any two ACPL-P345 parts under the same test condition.
- Propagation Delay Difference (PDD) is the difference between t_{PHL} and t_{PLH} between any two units under the same test condition.
- t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
- Pin 2 needs to be connected to LED common. Split resistor network in the ratio 1.5:1 with 232Ω at the anode and 154Ω at the cathode.
- Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in the high state (that is, $V_O > 10.0\text{V}$).
- Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM} , to assure that the output will remain in a low state (meaning $V_O < 1.0\text{V}$).

Package Characteristics

All typical values are at $T_A = 25^\circ\text{C}$. All minimum/maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage ^a	V_{ISO}	ACPL-P345	3750	—	—	V_{RMS}	RH < 50%, t = 1 min., $T_A = 25^\circ\text{C}$		b, c
		ACPL-W345	5000	—	—	V_{RMS}	RH < 50%, t = 1 min., $T_A = 25^\circ\text{C}$		c, d
Input-Output Resistance	R_{I-O}		—	$>50^{12}$	—	Ω	$V_{I-O} = 500 V_{DC}$		c
Input-Output Capacitance	C_{I-O}		—	0.6	—	pF	f = 1 MHz		
LED-to-Ambient Thermal Resistance	R_{11}		—	135	—	$^\circ\text{C/W}$			e
LED-to-Detector Thermal Resistance	R_{12}		—	27	—				
Detector-to-LED Thermal Resistance	R_{21}		—	39	—				
Detector-to-Ambient Thermal Resistance	R_{22}		—	47	—				

- The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.
- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500V_{RMS}$ for 1 second (leakage detection current limit, $I_{I-O} \leq 5 \mu\text{A}$).
- Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 6000V_{RMS}$ for 1 second (leakage detection current limit $I_{I-O} \leq 5 \mu\text{A}$).
- The device was mounted on a high conductivity test board as per JEDEC 51-7.

Typical Performance Plots

Figure 1: High Output Rail Voltage vs. Temperature

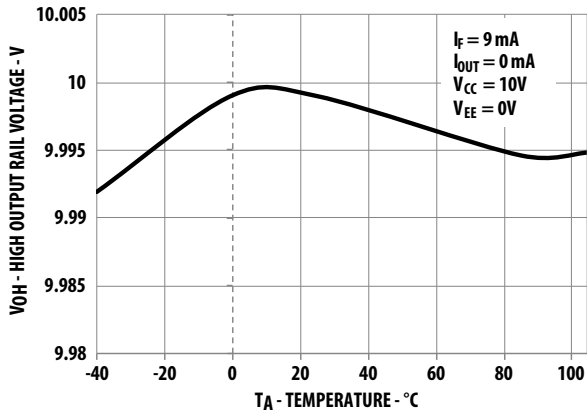


Figure 2: V_{OH} vs. Temperature

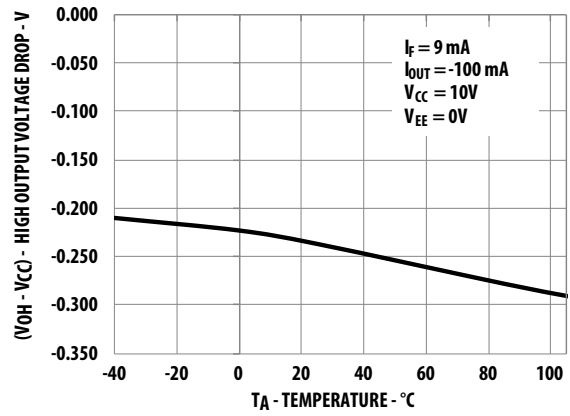


Figure 3: V_{OL} vs. Temperature

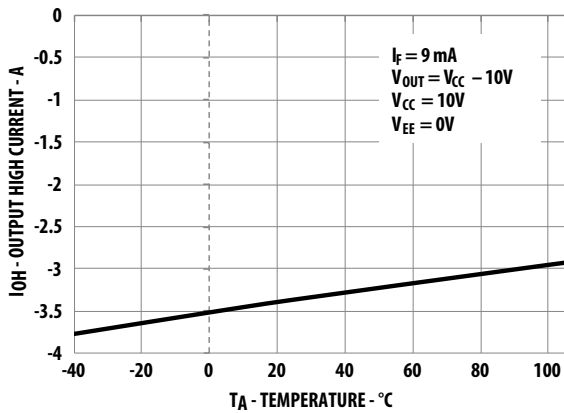


Figure 4: I_{CC} vs. Temperature

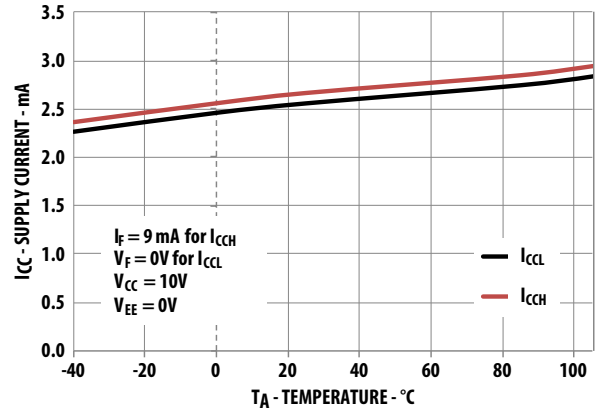


Figure 5: I_{CC} vs. V_{CC}

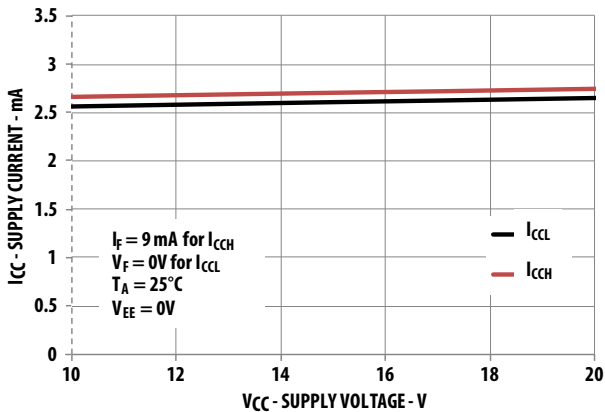


Figure 6: I_{FLH} Hysteresis

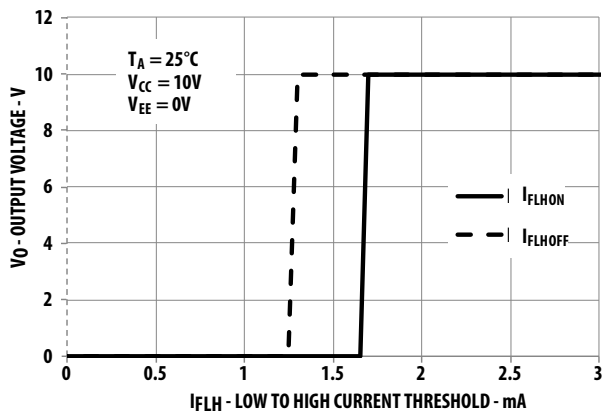


Figure 7: I_{FLH} vs. Temperature

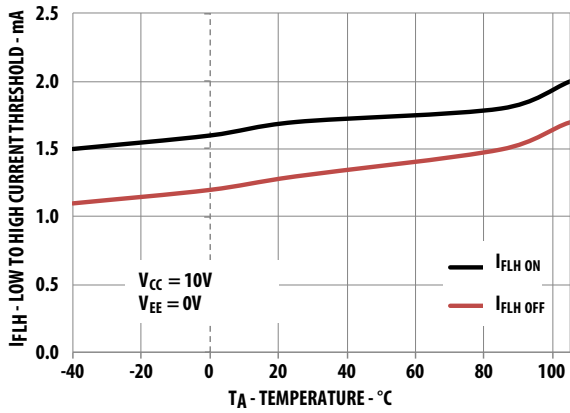


Figure 8: Propagation Delay vs. I_F

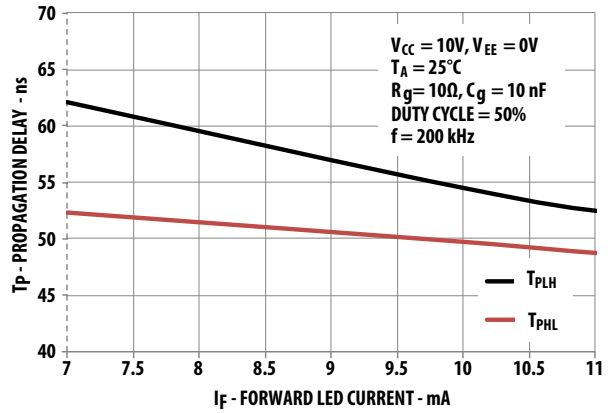


Figure 9: Propagation Delay vs. Temperature

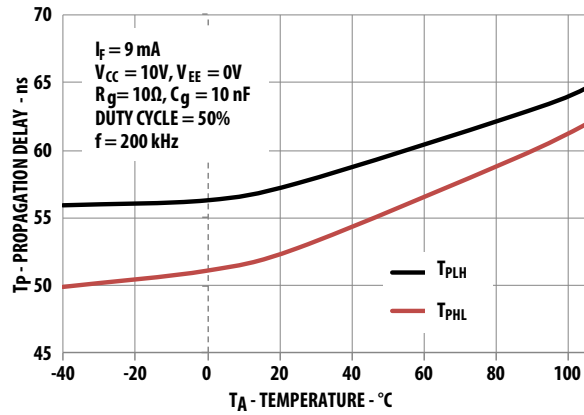


Figure 10: Propagation Delay vs. R_g

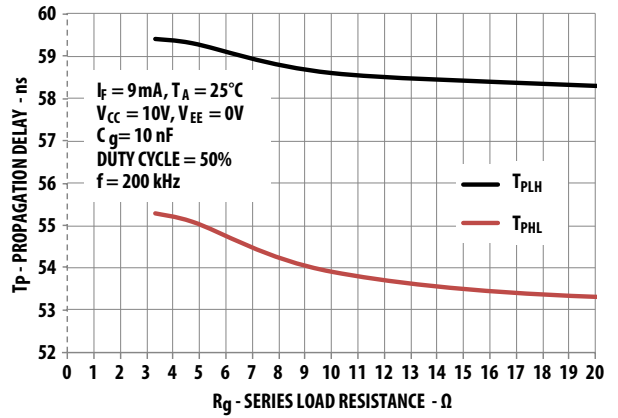


Figure 11: Propagation Delay vs. C_g

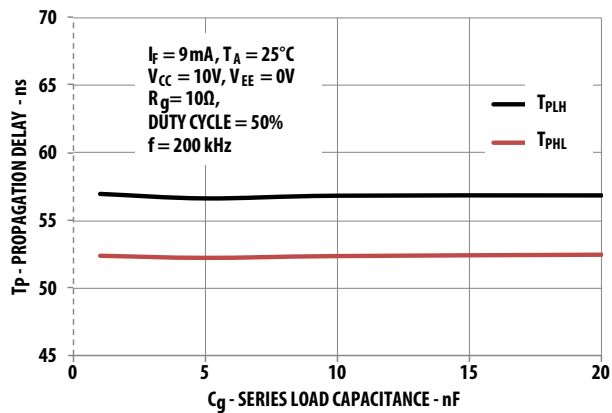


Figure 12: Rise and Fall Time vs. C_g

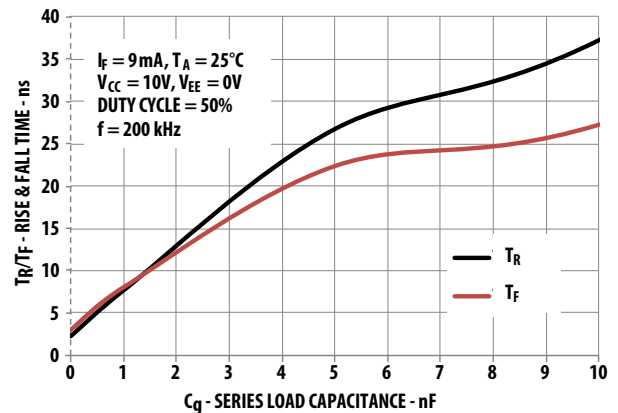


Figure 13: Input Current vs. Forward Voltage

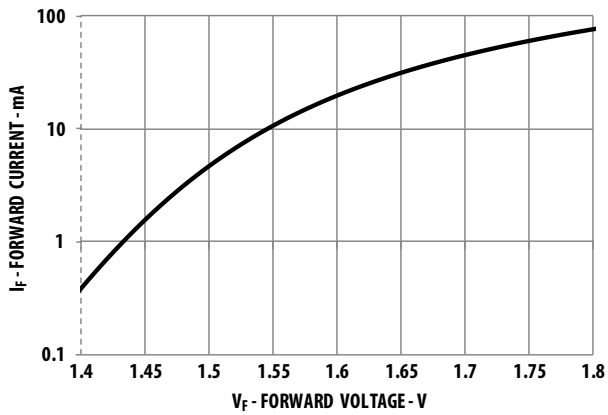


Figure 14: t_r and t_f Test Circuit and Waveforms

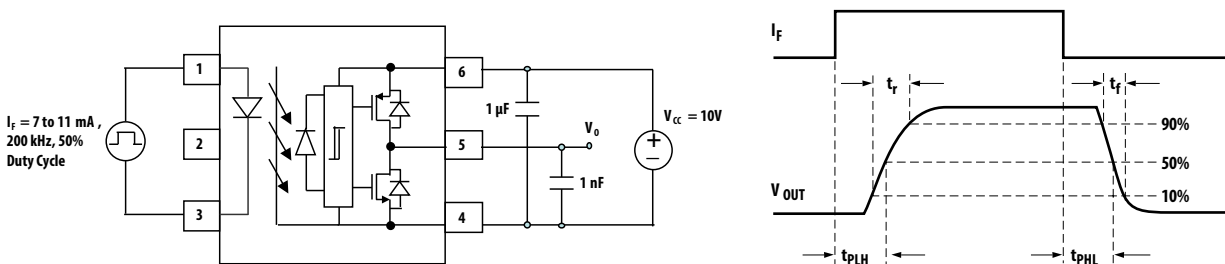
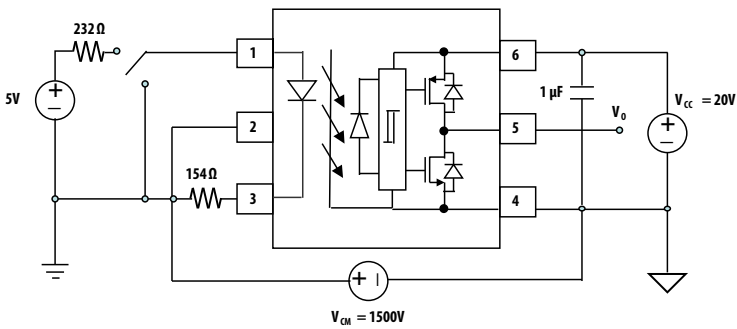


Figure 15: .CMR Test Circuit with Split Resistors Network



Application Information

Product Overview Description

The ACPL-P345/W345 is an optically isolated power output stage capable of driving power, GaN, or SiC MOSFET. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance and two times faster speed than the previous generation products.

The high peak output current and short propagation delay are needed for fast MOSFET switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the MOSFET's gate voltage is driven to the optimum intended level with no power loss across the MOSFET. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

It has very high CMR (common mode rejection) rating that allows the microcontroller and the MOSFET to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminate the need of additional Schmitt trigger circuit at the input LED.

The stretched SO6 package which is up to 50% smaller than conventional DIP package facilitates smaller and more compact design. These stretched packages are compliant to many industrial safety standards such as IEC/EN/DIN EN 60747-5-5, UL 1577 and CSA.

The stretched SO6 package which is up to 50% smaller than conventional DIP package facilitates smaller more compact design. These stretched packages are compliant to many industrial safety standards, such as IEC/EN/DIN EN 60747-5-5, UL 1577 and CSA.

Recommended Application Circuit

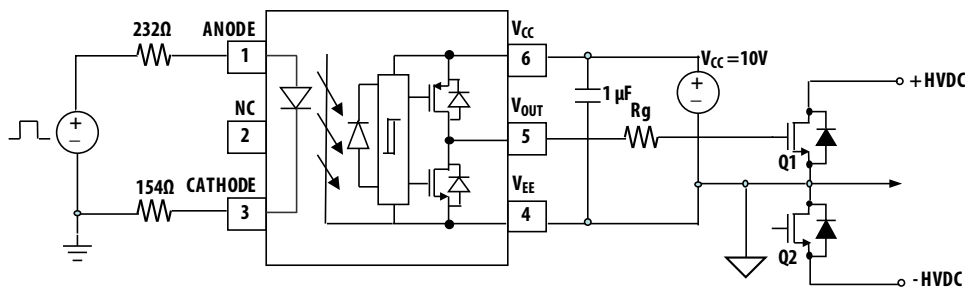
The recommended application circuit shown in [Figure 16](#) illustrates a typical gate drive implementation using the ACPL-P345.

The supply bypass capacitors (1 μ F) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (4.0 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1.5:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor R_G serves to limit gate charge current and controls the MOSFET switching times.

In PC board design, care should be taken to avoid routing the MOSFET drain or source traces close to the ACPL-P345 input as this can result in unwanted coupling of transient signals into ACPL-P345 and degrade performance.

Figure 16: Recommended Application Circuit with Split Resistors LED



Dead Time and Propagation Delay Specifications

The ACPL-P345/W345 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 16) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 18. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX} , which is specified to be 100 ns over the operating temperature range of $-40^{\circ}C$ to $105^{\circ}C$.

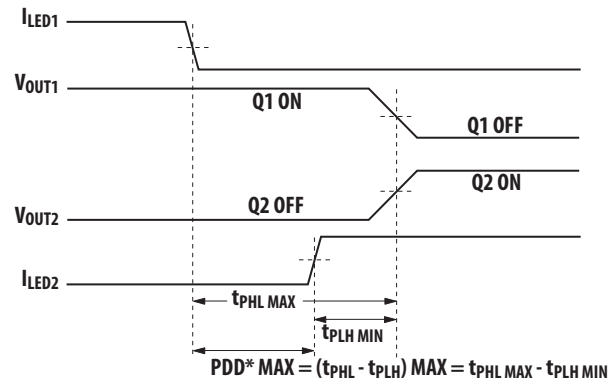
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 19. The maximum dead time for the ACPL-P345/W345 is 100 ns ($= 50 \text{ ns} - (-50 \text{ ns})$) over an operating temperature range of $-40^{\circ}C$ to $105^{\circ}C$.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical MOSFETs.

LED Current Input with Hysteresis

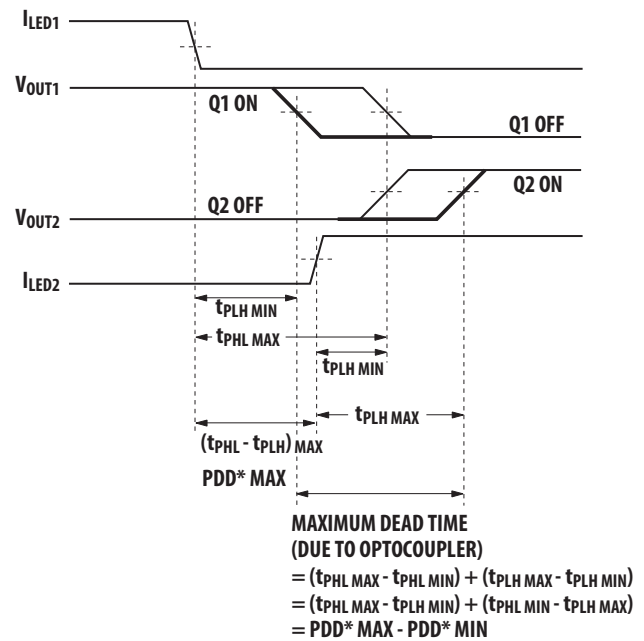
The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 6) provides differential mode noise immunity and minimizes the potential for output signal chatter.

Figure 18: Minimum LED Skew for Zero Dead Time



*PDD = Propagation Delay Difference
 Note: For PDD calculations, the propagation delays are taken at the same temperature and test conditions.

Figure 19: Waveforms for Dead Time



*PDD = Propagation Delay Difference
 Note: For Dead Time and PDD calculations, all propagation delays are taken at the same temperature and test conditions.

Thermal Model for ACPL-P347/ W347 Stretched SO6 Package Optocoupler

Definitions:

- R_{11} : Junction to Ambient Thermal Resistance of LED due to heating of LED
- R_{12} : Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)
- R_{21} : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.
- R_{22} : Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).
- P_1 : Power dissipation of LED (W).
- P_2 : Power dissipation of Detector/Output IC (W).
- T_1 : Junction temperature of LED (°C).
- T_2 : Junction temperature of Detector (°C).
- T_a : Ambient temperature.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above the optocoupler at ~23°C in still air

Thermal Resistance	°C/W
R_{11}	135
R_{12}	27
R_{21}	39
R_{22}	47

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm × 7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the following equations.

Equation 1:

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a$$

Equation 2:

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a$$

Using the given thermal resistances and thermal model formula in this data sheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperatures should be within the absolute maximum rating.

Related Documents

AV02-0421EN	Application Note 5336	<i>Gate Drive Optocoupler Basic Design for IGBT / MOSFET</i>
AV02-3698EN	Application Note 1043	<i>Common-Mode Noise: Sources and Solutions</i>
AV02-0310EN	Reliability Data	<i>Plastics Optocouplers Product ESD and Moisture Sensitivity</i>

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