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REVISION HISTORY

4/05—Revision 0: Initial Version

SPECIFICATIONS

Test conditions, unless otherwise noted

Table 1.

Parameters	Conditions	Unit
Supply Voltages (AV_{DD}, DV_{DD})	3.3	V
Ambient Temperature	25	°C
Input Signal	1 kHz, 0.8 V_{RMS} analog, 0 dBFS digital	Hz, V rms, dBFS
Input Sample Rate	48	kHz
Measurement Bandwidth	20 Hz to 14 kHz	kHz
Word Width	24	Bits
Load Capacitance	50	pF
Load Current	±1	mA
Input Voltage High	2.0	V
Input Voltage Low	0.8	V

Table 2. Analog Input Performance

Parameter	Min	Typ	Max	Unit
Maximum Input Level		1.0 (2.8)		V rms (V p-p)
Output Level		250		mV rms
Dynamic Range (20 Hz to 14 kHz, –60 dB Input) (Encoded Output, Left = Right)	68	74		dB
THD + Noise (Encoded Output, Left = Right, 20 Hz to 14 kHz)				
V_{IN} = 0 dBV rms		–72	–65	dB

Table 3. Digital Input Performance

Parameter	Min	Typ	Max	Unit
Resolution		24		Bits
Output Level		250		mV rms
Dynamic Range (20 Hz to 14 kHz, –60 dB Input) (Encoded Output, Left = Right)	81	87		dB
THD + Noise (Encoded Output, Left = Right, 20 Hz to 14 kHz)				
V_{IN} = 0 dBFS		–83	–74	dB

Table 4. Video Input

Parameter	Min	Typ	Max	Unit
Input Signal Level	0.35	1.0		V_{P-P}
Input Impedance		2		kΩ

Table 5. Crystal Oscillator

Parameter	Min	Typ	Max	Unit
Transconductance	7	10	13	mmhos

Table 6. BTSC Encoder Performance

Parameter	Min	Typ	Max	Unit
CHANNEL SEPARATION (–25 dB INPUT)				
30 Hz to 500 Hz	24	30		dB
500 Hz to 5 kHz	18	21		dB
5 kHz to 13.5 kHz	14	15		dB
CHANNEL SEPARATION AT 1 kHz				
0 dB Input	25	27		
–2 dB Input	24	26		
FREQUENCY RESPONSE				
30 Hz to 10 kHz	–1		+0.5	dB
30 Hz to 13.5 kHz	–1.5		+0.5	dB

Table 7. Digital I/O

Parameter	Min	Typ	Max	Unit
Input Voltage High (V_{IH})	2.0			V
Input Voltage Low (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 2.4 V)			10	µA
Input Leakage (I_{IL} @ V_{IL} = 0.4 V)			10	µA
High Level Output Voltage (V_{OH}) I_{OH} = 2 mA (except VID_PRES)	DVDD – 0.6			V
Low Level Output Voltage (V_{OL}) I_{OL} = 2 mA			0.4	V

Table 8. Power

Parameter	Min	Typ	Max	Unit
SUPPLIES				
Voltage, Analog, Digital, PLL	3.0	3.3	3.6	V
Analog Current	30	41	50	mA
Digital Current	30	38	48	mA
PLL Current	1	5	8	mA
DISSIPATION				
All Supplies		277		mW
Analog Supply		135		mW
Digital Supply		125		mW
PLL Supply		17		mW

Table 9. Temperature Range

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	0		70	°C
Storage	–55		+125	°C

Table 10. Digital Timing

Parameter		Min	Typ	Max	Unit
t_{DMD}	MCLK Duty Cycle, External 512 f_S Mode	40	50	60	%
t_{DBL}	MCLK Low Pulse Width, External 512 f_S Mode	15			ns
t_{DBH}	MCLK High Pulse Width, External 512 f_S Mode	15			ns
t_{DBL}	MCLK Low Pulse Width, PLL, 256 f_S or f_S Mode	15			ns
t_{DBH}	MCLK High Pulse Width, PLL, 256 f_S or f_S Mode	15			ns
t_{DLS}	LRCLK Setup	10			ns
t_{DLH}	LRCLK Hold	10			ns
t_{DDS}	SDATA Setup	10			ns
t_{DDH}	SDATA Hold	10			ns
t_{IBC}	I^2C Bus Clock Frequency			400	kHz
t_{ISST}	I^2C Setup Time for Start Condition	10			ns
t_{IH}	I^2C Hold Time for Start Condition	30			ns
t_{SDS}	SDA Setup Time	50			ns
t_{SDH}	SDA Hold Time	25			ns
t_{SDF}	SDA Fall Time at 3 mA Sink and 400 pF Load			25	ns
t_{SDR}	SDA Rise Time			300	ns
t_{PWS}	Pulse Width of Spikes Supressed by the Input Filter	50			ns
t_{PDRP}	RESETB Low Pulse Width	15			ns

ABSOLUTE MAXIMUM RATINGS

Table 11.

	Min	Max	Unit
DV_{DD} to DGND	–0.3	+3.95	V
ODV_{DD} to DGND	–0.3	+3.95	V
AV_{DD} to AGND	–0.3	+3.95	V
Digital Inputs	DGND – 0.3	DV_{DD} + 0.3	V
Analog Inputs	AGND – 0.3	AV_{DD} + 0.3	V
AGND to DGND	–0.3	+0.3	V
Reference Voltage		(AV_{DD} + 0.3)/2	V
Maximum Junction Temperature		+125	°C
Storage Temperature Range	–65	+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE CHARACTERISTICS (48-LEAD LQFP)

Table 12.

	Min	Typ	Max	Unit
θ_{JA} (Thermal Resistance [Junction-to-Ambient])		72		°C/W
θ_{JC} (Thermal Resistance [Junction-to-Case])		19.5		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

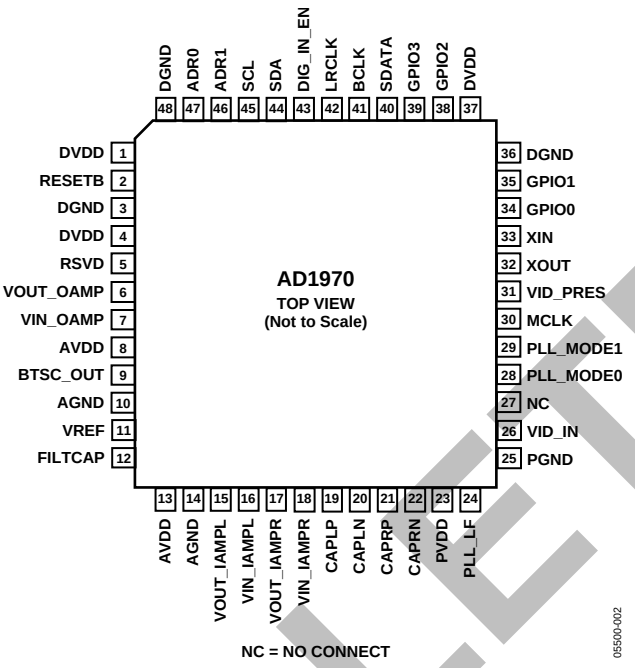

Figure 2. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Pin Name	Input/Output	Description
1	DVDD		Digital Power.
2	RESETB	IN	Reset—Active Low. After RESETB transitions from low to high, the AD1970 BTSC encoder core goes through an initialization sequence where all registers are set to 0. The initialization is completed after 1024 MCLK cycles. New values should not be written to the control port until the initialization is complete.
3	DGND		Digital Ground.
4	DVDD		Digital Power. 3.3 V nominal.
5	RSVD		Reserved—Connect to DGND.
6	VOUT_OAMP	OUT	Output voltage of internal op amp to be used for BTSC output low pass filter.
7	VIN_OAMP	IN	Negative input of internal op amp to be used for BTSC output low pass filter.
8	AVDD		Analog Power.
9	BTSC_OUT	OUT	Encoded BTSC Output. The nominal output voltage for a 300 Hz, 0 dB mono input signal is 250 mV rms.
10	AGND		Analog Ground.
11	VREF	OUT	Connection for voltage reference noise reduction capacitor. The nominal VREF voltage is 1.5 V; the analog gain scales directly with the voltage on this pin. Any ac signal on this pin causes distortion and therefore a large decoupling capacitor should be used to ensure the voltage on VREF is clean.
12	FILTCAP	OUT	Connection for DAC noise reduction capacitor. A 10 µF capacitor should be connected to this pin to reduce the noise on an internal DAC biasing point to provide the highest performance. It may not be necessary to connect this pin, depending on the quality of the layout and grounding used in the application circuit.
13	AVDD		Analog Power. 3.3 V nominal. Bypass capacitors should be placed close to the pins and connected directly to the analog ground plane.
14	AGND		Analog Ground.
15	VOUT_IAMPL	OUT	Output of internal op amp for left channel input amplifier.
16	VIN_IAMPL	IN	Negative input of internal op amp for left channel input amplifier.
17	VOUT_IAMPR	OUT	Output of internal op amp for right channel input amplifier.

Pin No.	Pin Name	Input/Output	Description
18	VIN_IAMPR	IN	Negative input of internal op amp for right channel input amplifier.
19	CAPLP	I/O	ADC Filter Capacitor Connection (positive left-channel input to modulator). A 1 nF capacitor should be placed between this pin and analog ground.
20	CAPLN	I/O	ADC Filter Capacitor Connection (negative left-channel input to modulator). A 1 nF capacitor should be placed between this pin and analog ground.
21	CAPRP	I/O	ADC Filter Capacitor Connection (positive right-channel input to modulator). A 1 nF capacitor should be placed between this pin and analog ground.
22	CAPRN	I/O	ADC Filter Capacitor Connection (negative right-channel input to modulator). A 1 nF capacitor should be placed between this pin and analog ground.
23	PVDD		PLL Power. 3.3 V nominal. Bypass capacitors should be placed close to this pin and connected directly to the PLL ground.
24	PLL_LF		PLL Loop Filter Connection.
25	PGND		PLL Ground. Connect to DGND.
26	VID_IN	IN	Composite Video Input. Composite video signal input to the sync separator. The sync output is connected to a PLL that generates the clocks for the AD1970. This pin has an input impedance of 2 kΩ.
27	NC		No Connect.
28	PLL_MODE0	IN	PLL Mode Select Pin 0. The setting of these pins indicates the source and frequency of the input clock to generate the internal MCLK for the AD1970.
29	PLL_MODE1	IN	PLL Mode Select Pin 1. The setting of these pins indicates the source and frequency of the input clock to generate the internal MCLK for the AD1970.
30	MCLK	IN	Master Clock Input. This input is used to generate the internal master clock if it is not derived from the composite video signal on VID_IN. The master clock frequency must be either fs or 256 × fs, where fs is the input sampling frequency. The PLL_CTRLx pins should be set to accept the appropriate MCLK input frequency.
31	VID_PRES	OUT	Video Present Flag. A high logic level on this pin indicates that a valid composite video signal is present on the VID_IN pin. Open-drain output.
32	XOUT	OUT	Crystal Oscillator Output. This pin is the output of the on-board oscillator and should be connected to one side of a crystal.
33	XIN	IN	Crystal Oscillator Input. This pin is the input to the on-board oscillator and should be connected to one side of a crystal.
34	GPIO0	IN/OUT	General Purpose I/O 0. This pin can be set to be either a static input or output, with levels and direction controlled through the I^2C port.
35	GPIO1	IN/OUT	General Purpose I/O 1. This pin can be set to be either a static input or output, with levels and direction controlled through the I^2C port.
36	DGND		Digital Ground.
37	DVDD		Digital Power.
38	GPIO2	IN/OUT	General Purpose I/O 2. This pin can be set to be either a static input or output, with levels and direction controlled through the I^2C port.
39	GPIO3	IN/OUT	General Purpose I/O 3. This pin can be set to be either a static input or output, with levels and direction controlled through the I^2C port.
40	SDATA	IN/OUT	Serial Data Input/Output (Before BTSC Encoding). Digital input to the BTSC encoder or output of the ADC. The serial format is selected by writing to Bits 3:2 of Control Register 1.
41	BCLK	IN/OUT	Bit Clock Input/Output. Serial bit clock for clocking in the serial data. The interpretation of BCLK changes according to the serial mode, which is set by writing to the control registers.
42	LRCLK	IN/OUT	Left/Right Clock Input/Output. Left/right clock for framing the serial input data. The interpretation of the LRCLK changes according to the serial mode, set by writing to the control registers.
43	DIG_IN_EN	IN	Digital Input Enable (active high).
44	SDA	IN/OUT	I^2C Serial Data Input/Output.
45	SCL	IN	I^2C Serial Clock Input.
46	ADR1	IN	I^2C Address 1. The address of the I^2C port is set by these pins according to Table 16.
47	ADR0	IN	I^2C Address 0. The address of the I^2C port is set by these pins according to Table 16.
48	DGND		Digital Ground.

THEORY OF OPERATION

The AD1970 is comprised of a BTSC encoder with stereo analog inputs and a sync separator to derive the pilot signal from the composite video stream. Figure 1 shows the block diagram of the device.

Signal processing parameters are stored in a parameter RAM, which is initialized on power-up by an internal boot ROM. The values stored in the parameter RAM control all the filter coefficients, mixing, and dynamics-processing code used in the BTSC algorithm.

The AD1970 has an I^2C port that supports complete read/write capability of the parameter RAM, as well as a control port and several other registers that allow the various signal processing parameters to be controlled. The AD1970 can run as a stand-alone processor without external control.

The AD1970 has a very flexible serial data input port that allows for glueless interconnection to a variety of digital signal sources. The AD1970 can be configured in left-justified, I^2S, right-justified, or DSP serial port-compatible modes. It can support 16, 20, and 24 bits in all modes. The AD1970 accepts serial audio data in MSB first, twos complement format.

The AD1970 operates from a single 3.3 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 48-pin LQFP package for operation over the temperature range of 0°C to 70°C.

SIGNAL PROCESSING

BACKGROUND OF BTSC

BTSC is the name of the standard for adding stereo audio capability to the US television system. It is in many ways similar to the algorithm used for FM stereo broadcasts, with the addition of a sophisticated compressor circuit to improve the signal-to-noise ratio.

To maintain compatibility with non-BTSC TV receivers, the processing of mono (L = R) signals is unchanged from the original pre-BTSC system. The L + R signal is applied to a 75 µs pre-emphasis filter, and is then applied to a 4.5 MHz FM modulator, which is later added to the video signal to create a composite video signal.

Stereo capability is added by taking the L − R signal, applying it to a 2-band dynamic compressor, and then multiplying this signal by a carrier signal at twice the horizontal scanning rate (F_h), or about 2 × 15.734 kHz. This multiplication is known as double sideband, suppressed-carrier modulation, and it effectively translates the compressed L − R spectrum up in frequency so that it sits above the audio band (see Figure 3).

For the receiver to recover this L − R signal, a pilot tone at the horizontal rate is added to the signal. The receiver has a PLL that locks to this pilot and generates a signal at the carrier frequency. This signal is then used to multiply the composite BTSC-encoded signal, which translates this component back down to baseband. Once the L + R and L − R signals are recovered, a simple addition/subtraction circuit (sometimes referred to as the matrix) can be used to recover the right signal. Since the pilot tone is added at 15.734 kHz, it is necessary to reduce the bandwidth of the signal so that audio signals cannot interfere with the pilot tone. In the AD1970, the bandwidth is limited to 14 kHz; above this frequency, the response decays very rapidly.

PERFORMANCE FACTORS

To maintain good separation between the left and right channels, it is necessary to closely match the filtering and companding standards set forth in the standard (FCC OET60). Even small errors can result in poor performance. The AD1970 has been programmed to match these standards as accurately as possible. Typical separation numbers range from 30 dB at frequencies below 500 Hz to 15 dB at 13.5 kHz. Measuring these numbers can be difficult, since significant differences exist between many units sold as reference decoders, which are all implemented with analog components.

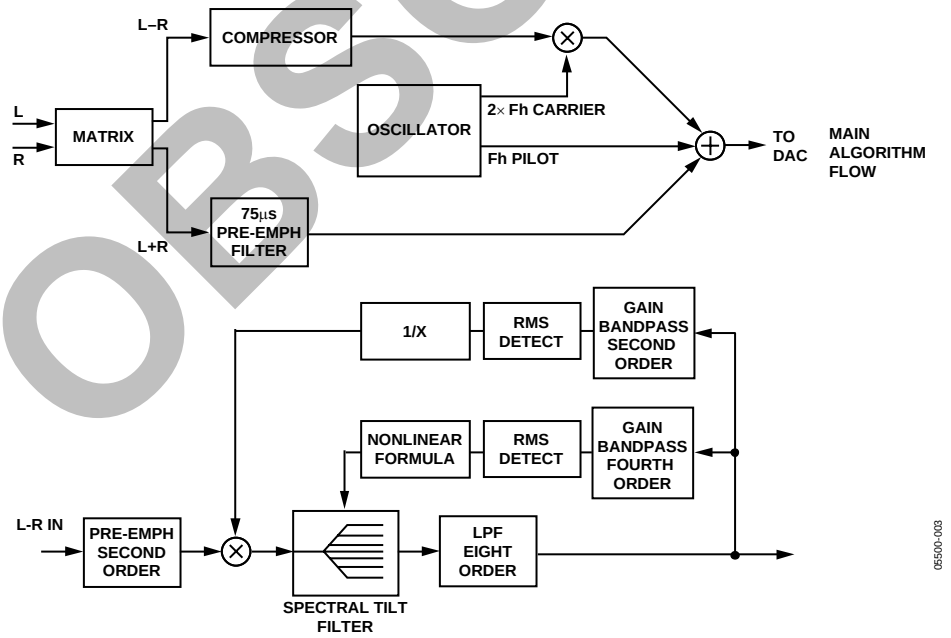

Figure 3. Signal Processing Flow

SEPARATION ALIGNMENT

The BTSC encoder outputs are all specified in terms of the deviation of the FM 4.5 MHz carrier. For the AD1970, a digital input level of 0 dB (mono signal) should cause a carrier deviation of ±25 kHz without the 75 µs pre-emphasis filter. In practice, the pre-emphasis filter can be left in for this adjustment, as long as the frequency is low enough to not be affected by the filter. It is critical to maintain the proper gain relationship between the BTSC encoder and the 4.5 MHz FM modulator. A common mistake is to assume that changing the gain between the BTSC encoder output and the FM modulator input has the same effect as changing the audio input level going in to the BTSC encoder. The presence of a complicated 2-band nonlinear dynamics processor means that the encoder output must be connected to the decoder input (through the FM modulation/demodulation process) with a known gain. If this gain is changed, then the separation significantly suffers.

When measuring the AD1970 on the bench, it is possible to use a BTSC reference decoder box, so that the FM modulation/demodulation process can be skipped. These units have a method of adjusting the input voltage sensitivity to achieve best separation. The output level of the AD1970 can also be adjusted over a wide range using either the I²C control port or by adjusting the values of the components used in the external analog low-pass filter that is between the BTSC encoder output and the input to the FM modulator.

PHASE LINEARITY OF THE EXTERNAL ANALOG FILTER

If the time-alignment of the pilot to the carrier signal is not close to 0°, a loss of separation can occur. This means that the external analog low-pass filter should be a linear-phase design to provide constant group delay over the range from dc to 50 kHz. A Bessel filter is recommended for this application. The typical applications circuit (see Figure 8) shows a recommended design for this filter.

INPUT LEVELS

The maximum input level to the AD1970 changes across frequency. Table 14 shows the maximum allowable input level for different frequencies. These values are part of the BTSC specification, not a function of this chip.

Table 14. Maximum Input Levels to the BTSC Encoder across Frequency

Frequency (Hz)	Maximum Input Level (dBFS)
20 to 1000	0
1600	−1
2500	−3
3150	−5
5000	−8
8000	−11
12500	−15

CLOCKING AND PLL

The AD1970's master clock either can be directly fed to the MCLK pin or generated by a PLL from a composite video signal input on the VID_IN pin. If the clock input is on the MCLK pin, the PLL can synthesize the internal clocks from either a clock at the digital audio frame sync frequency (f_S = 48 kHz) or 256 × f_S. The PLL mode is controlled by Pins PLL_MODE0 and PLL_MODE1. The settings are shown in Table 15.

Table 15. PLL Modes

PLL_MODE1	PLL_MODE0	Setting
0	0	Composite video input (on VID_IN)
0	1	256 × fs (on MCLK)
1	0	fs (on MCLK)
1	1	PLL bypass

CRYSTAL OSCILLATOR

The AD1970 has an on-board crystal oscillator to generate a clock that can be used by an RF modulator or other application. For example, a 4 MHz crystal can be connected as shown in the application circuit (see Figure 8). The AD1970 does not use this clock itself, so if it is not needed in an application the XIN pin should be grounded and the XOUT pin left unconnected.

GENERAL PURPOSE INPUT/OUTPUT (GPIO) PINS

Pins GPIO0, GPIO1, GPIO2, and GPIO3 are set to be inputs or outputs by Bits 19:16 of Control Register 2. All four default to input state. These pins do not take an input to or send an output from the main signal flow. When set as an output, the binary value on the pins is set according to Bits 15:12 of Control Register 2. These pins can be used to interface with I/O pins on a microcontroller and allow hardware control via the I²C bus.

POWER-UP SEQUENCE

The AD1970 has a built-in power-up sequence that initializes the contents of all internal RAMs. During this time, the parameter RAM is filled with values from its associated boot ROM. The data memories are also cleared during this time.

The boot sequence lasts for 1024 MCLK cycles and starts on the rising edge of the RESETB pin. The user should avoid writing to or reading from the I²C registers during this period of time.

CONTROL PORT

I²C PORT OVERVIEW

The AD1970 can be controlled using the I²C port. In general, there are three parameters that can be controlled: the encoder output level, the Phat Stereo image enhancement algorithm, and the dialog enhancement algorithm. It is also possible to write new data into the parameter RAM to alter the filter coefficients used in the BTSC encoding process. Since this is a fairly complex topic and is unnecessary for normal operation of the chip, the details are not included in this data sheet; please contact ADI sales if modifications to the BTSC filters are required.

The I²C port uses a 2-wire interface consisting of SDA, the bidirectional data line, and SCL, the clock.

The R/$\overline{W}$ bit is low for a write operation and high for a read operation. The 10-bit address word is decoded into either a location in the parameter RAM or one of the registers. The number of data bytes varies according to the register or memory being accessed. The detailed data format diagram for continuous-mode operation is given in the section.

I²C ADDRESS DECODING

Table 16 shows the address decoding used in the I²C port. Four different addresses are available to avoid conflicting addresses on an I²C bus. The I²C address space encompasses a set a registers and the parameter RAM. The parameter RAM is loaded on power-up from an on-board boot ROM.

Table 16. I²C Address Settings

ADR1	ADR0	I²C Address
0	0	0x20
0	1	0x21
1	0	0x22
1	1	0x23

Table 17. I²C Port Address Decoding

Register Address	Register Name	Read/Write Word Length
0	Input Level Control	Write: 22 bits Read: 22 bits
1 to 254	Parameter RAM	
255	Output Level Control	
256	Control Register 1	Write: 11 bits Read: 6 bits
257	Control Register 2	Write: 22 bits
258	ADC Volume Control	
259	Stereo Spreading Control	
260	Dialog Enhancement Control	

INPUT LEVEL CONTROL

This register location controls the input level of both the left and right channels to the AD1970 BTSC encoding algorithm. The register defaults to a value of 1.0 (01000000000000000000 in binary 2.20 format) and allows a maximum of 12 dB of gain at a full-scale value. This feature allows compatibility with the Dolby digital specification for proper operation in both RF mode and line mode. In RF mode, the dialog level is specified at 11 dB higher than the dialog level in line mode. A gain of 11 dB can be achieved by writing 1.8836 to Address 0.

OUTPUT LEVEL CONTROL

The level control of the BTSC-encoded output is controlled in this register location. The default value is 0.5 (–6 dB, 00100000000000000000 in binary 2.20 format), or 250 mV on the DAC output. The output level should not be used as a volume control. Its intended use, in conjunction with the output filter, is to match the level with the expected input of the BTSC decoder. Matching these allows maximum separation between the left and right encoded channels.

Control Register 1

Control Register 1 is an 11-bit register that controls serial modes, de-emphasis, mute, power-down, and I²C-to-memory transfers. Table 18 documents the contents of this register.

Bits 5:4 and 10:8 are reserved and should be set to 0 at all times.

The audio signal is muted with Bit 7 of the control register.

The soft power-down bit (Bit 6) stops the internal clocks to the DSP core, but does not reset the part. The digital power consumption is reduced to a low level when this bit is asserted. Reset can only be asserted using the external reset pin.

Bits 3:2 select the serial format from one of four modes. These different formats are discussed in the section of this data sheet.

The word length bits (1:0) are used in right-justified serial modes to determine where the MSB is located relative to the start of the audio frame.

Table 18. Control Register 1 Write

Register Bits	Function
10:8	Reserved, set to 000
7	Soft mute (1 = start mute sequence)
6	Soft power-down (1 = power-down)
5:4	Reserved, set to 00
3:2	Serial-In mode 00 = I²S 01 = Right-justified 10 = DSP 11 = Left-justified
1:0	Word length 00 = 24 bits 01 = 20 bits 10 = 16 bits 11 = 16 bits

Table 19. Control Register 1 Read

Register Bits	Function
5:2	GPIO 3:0 read back
1:0	Reserved

Control Register 2

Control Register 2 is a 22-bit write-only register that controls power down modes, PLL and sync separator controls, and digital I/O pin functions.

Table 20. Control Register 2

Register Bits	Function
21	Enable ADC output on serial audio interface
20	Reserved
19:16	GPIO output enable 3:0
15:12	GPIO data
11:9	PLL shift, default 100
8:4	Sync separator slicer voltage; default 10111
3	ADC power-down
2	Reference power-down
1	DAC power-down
0	PLL power-down

ADC Volume Control Register

This controls the input level of both ADC channels. The default value is 1.0 (01000000000000000000 in binary 2.20 format).

Stereo Spreading Register

This register controls ADI's patented Phat Stereo spatial enhancement algorithm. The default is all 0s, which corresponds to no effect. The maximum setting is 01000000000000000000 or a twos complement fractional value of 1.0. Note that the bass energy in each channel is increased using this algorithm, which may cause some digital clipping on full-scale signal peaks, especially at low frequencies.

Dialog Enhancement Register

This controls the built-in dialog enhancement algorithm, and defaults to 0. The maximum setting is 01000000000000000000 or a twos complement fractional value of 1.0. This algorithm is intended to solve the problem of playing back high dynamic range digital audio signals over a television's built-in speakers. It provides an amplitude boost to signals that are in the range where dialog signals are usually found, while at the same time preventing loud special effects passages from overloading the speakers or amplifiers.

I²C READ/WRITE DATA FORMATS

The read/write formats of the I²C port are designed to be byte oriented. This allows for easy programming of common microcontroller chips. In order to fit into a byte oriented format, 0s are appended to the data fields in order to extend the data word to the next multiple of 8 bits. For example, 22-bit words written to the parameter RAM are appended with two leading zeroes in order to reach 24 bits (3 bytes). These zero-extended data fields are appended to a 2-byte field consisting of a read/write bit and a 10-bit address. The I²C port knows how many data bytes to expect based on the address received in the first two bytes.

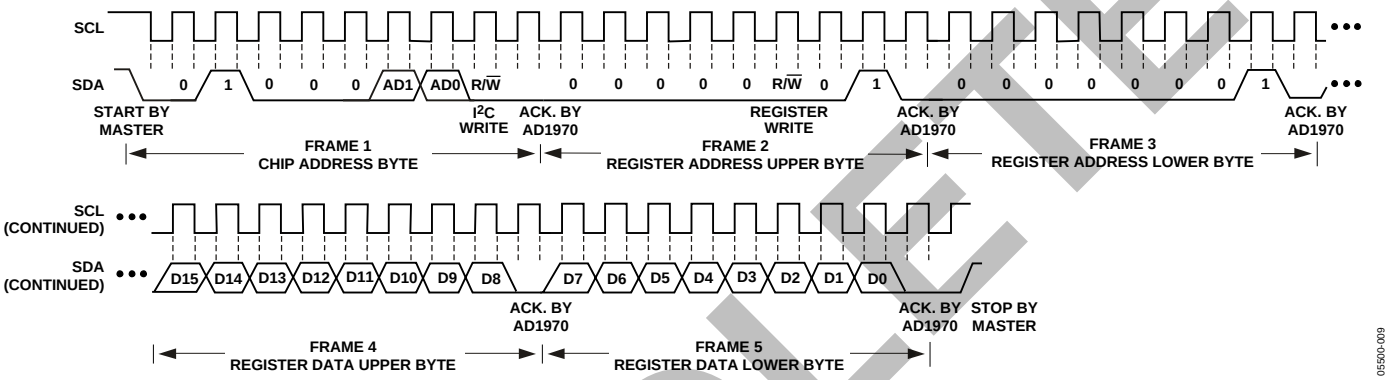

Figure 4. Sample of I²C Write Format (Control Register 1 Write)

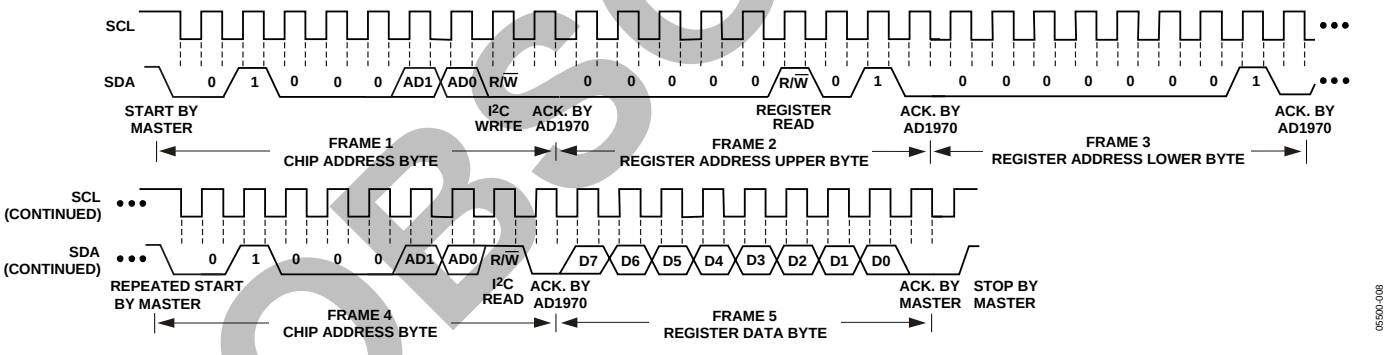

Figure 5. Sample of I²C Read Format (Control Register 1 Read)

Table 21. Control Register 1 Write Format

Byte 0	Byte1	Byte 2	Byte 3
00000, R/$\overline{W}$ = 0, Adr [9:8]	Adr [7:0]	00000, Bit [10:8]	Bit [7:0]

Table 22. Control Register 1 Read Format

Byte 0	Byte 1	Byte 2
00000, R/$\overline{W}$ = 1, Adr [9:8]	Adr [7:0]	00, Bit [5:0]

Table 23. Control Register 2 Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
00000, R/$\overline{W}$ = 0, Adr [9:8]	Adr [7:0]	00, Bit [21:16]	Bit [15:8]	Bit [7:0]

Table 24. Input/Output Level Control, ADC Volume Control, Stereo Spreading, and Dialog Enhancement Registers Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
00000, R/$\overline{W}$ = 0, Adr [9:8]	Adr [7:0]	00, Level [21:16]	Level [15:8]	Level [7:0]

ANALOG INPUT/OUTPUT

ADC INPUT

The AD1970 accepts an analog left-right signal on its input.

DAC OUTPUT

Figure 6 shows the block diagram of the analog output. A series of current sources are controlled by a digital Σ-Δ modulator. Depending on the digital code from the modulator, each current source is connected to the summing junction of either a positive I-to-V converter or a negative I-to-V converter. Two extra current sources that push instead of pull are added to set the midscale common-mode voltage.

All current sources are derived from the VREF input pin. The gain of the AD1970 is directly proportional to the magnitude of the current sources, and therefore the gain of the AD1970 is proportional to the voltage generated on the VREF pin. The nominal VREF voltage is 1.5 V.

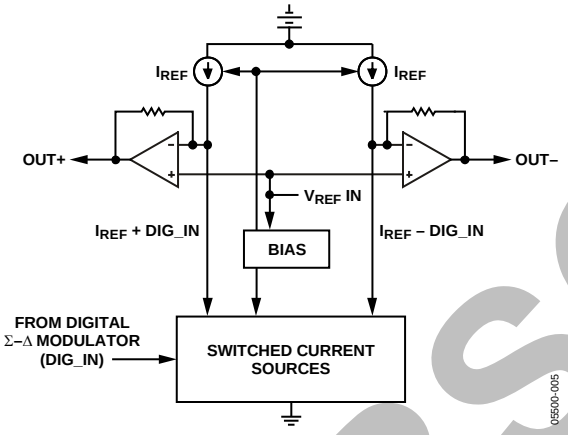

Figure 6. Internal DAC Analog Architecture

Since the VREF input effectively multiplies the signal, care must be taken to insure that no ac signals appear on this pin. This can be accomplished by using a large decoupling capacitor connected to VREF.

The AD1970 should be used with an external third order filter on each output channel, as shown in Figure 8. The values shown are for a 100 kHz Bessel filter. The use of a Bessel filter is important to maintain the time-alignment of the pilot to the carrier. If these signals are not in phase, a loss of separation occurs.

For best performance, a large (>10 μF) capacitor should be connected between the FILTCAP pin and analog ground.

SERIAL DATA PORT

The AD1970's flexible serial audio interface accepts and sends data in twos complement, MSB first format. The left channel data field always precedes the right channel data field. The serial mode is set by using mode select bits in the control register. In all modes except for the right justified mode, the serial port accepts an arbitrary number of bits up to a limit of 24 (extra bits do not cause an error, but they are truncated internally). In the right-justified mode, control register bits are used to set the word length to 16, 20, or 24 bits. The default on power-up is 24-bit mode. Proper operation of the right justified mode requires that there be exactly 64 BCLKs per audio frame.

SERIAL DATA MODES

Figure 7 shows the left-justified mode. LRCLK is high for the left channel, and low for the right channel. Data is sampled on the rising edge of BCLK. The MSB is left-justified to a LRCLK transition, with no MSB delay. The left-justified mode can accept any word length up to 24 bits.

Figure 7 shows the I2S mode, which is the default setting. LRCLK is low for the left channel and the MSB is delayed from the edge of the LRCLK by a single BCLK period. The I2S mode can be used to accept any number of bits up to 24.

Figure 7 shows the right-justified mode of the AD1970. LRCLK is high for the left channel, low for the right channel. Data is sampled on the rising edge of BCLK. The start of data is delayed from the LRCLK edge by 16, 12, or 8 BCLK intervals, depending on the selected word length. The default word length is 24 bits; other word lengths are set by writing to Bits 1:0 of the control register. In right-justified mode, it is assumed that there are 64 BCLKs per frame.

Figure 7 shows the DSP serial port mode. LRCLK must pulse high for at least one bit clock period before the MSB of the left channel is valid and LRCLK must pulse high again for at least one bit clock period before the MSB of the right channel is valid. Data is sampled on the falling edge of BCLK. The DSP serial port mode can be used with any word length up to 24 bits. In this mode, it is the responsibility of the DSP to ensure that the left data is transmitted with the first LRCLK pulse and that synchronism is maintained from that point forward.

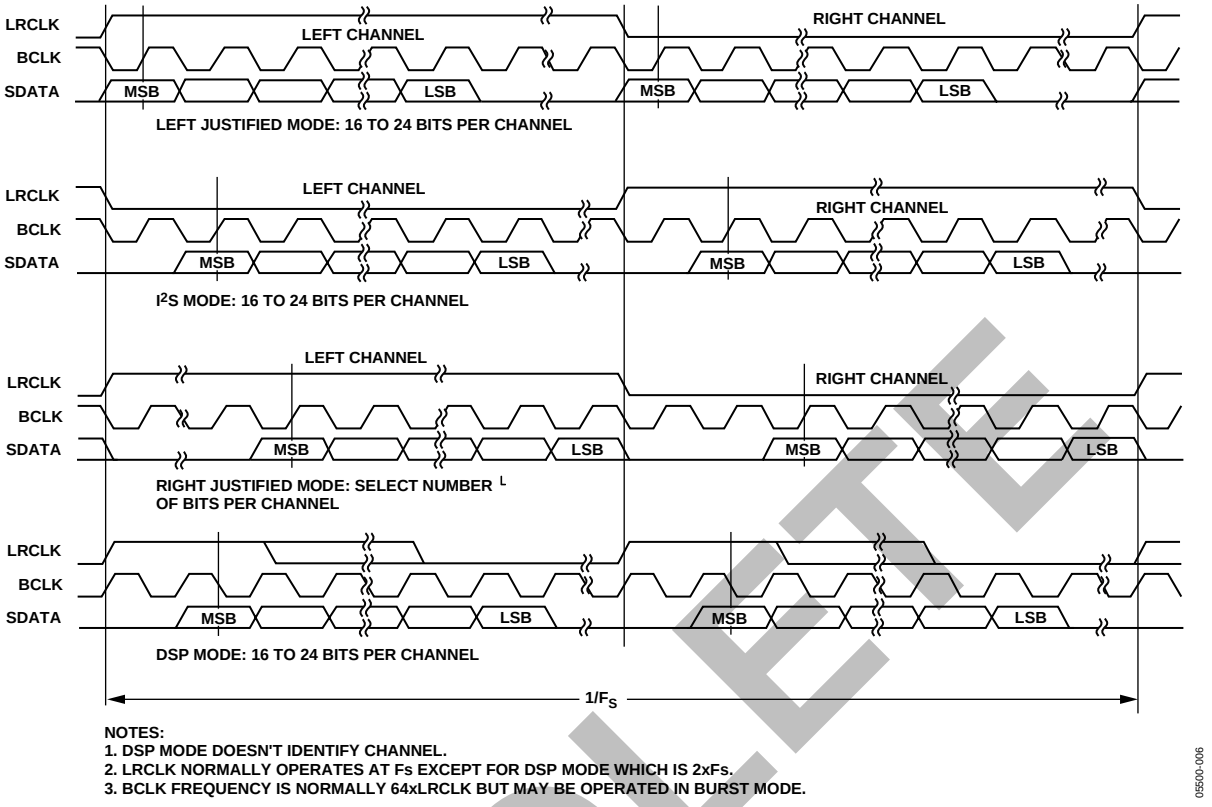

Figure 7. Serial Data Formats

TYPICAL APPLICATIONS CIRCUIT

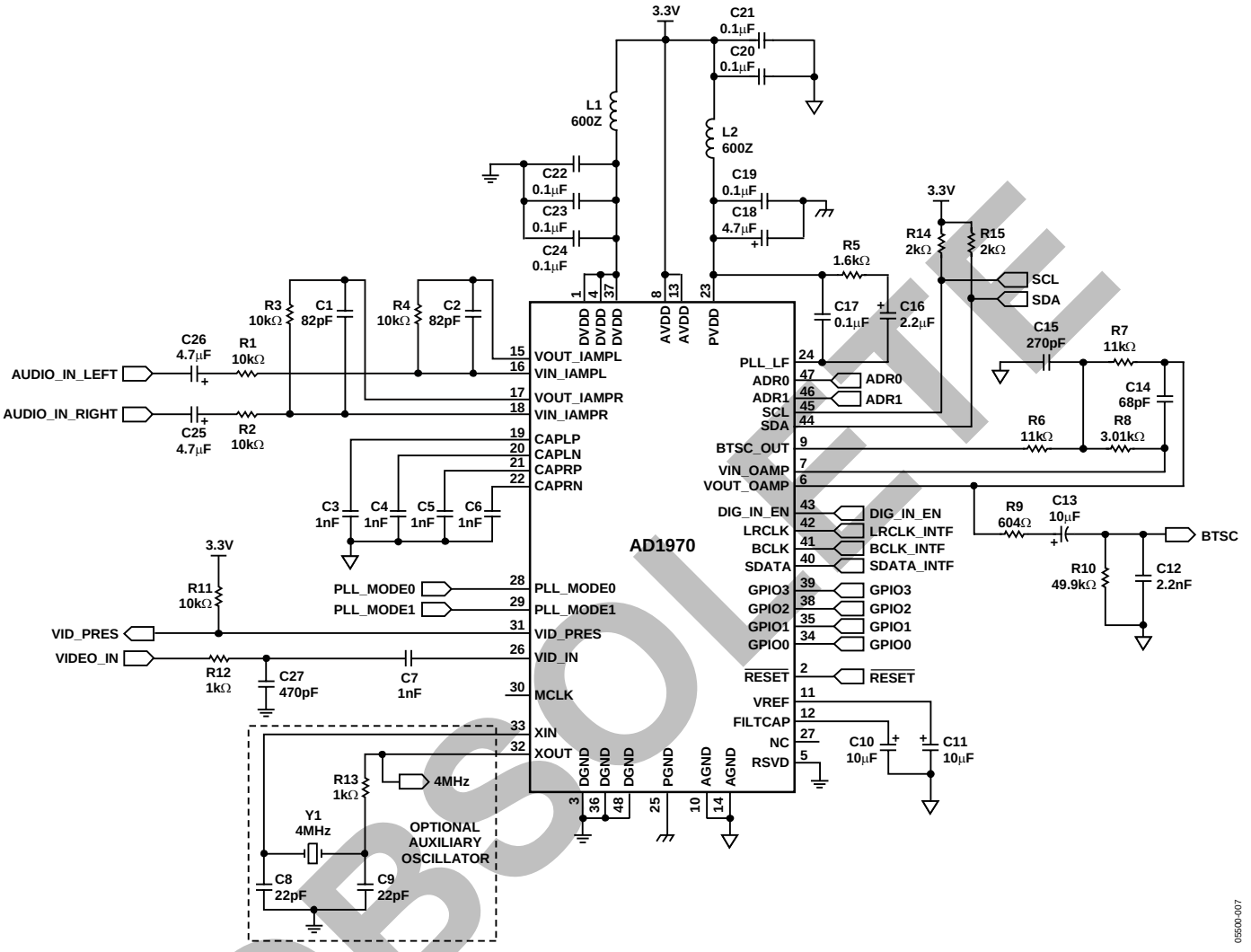

Figure 8. Typical Applications Circuit

OUTLINE DIMENSIONS

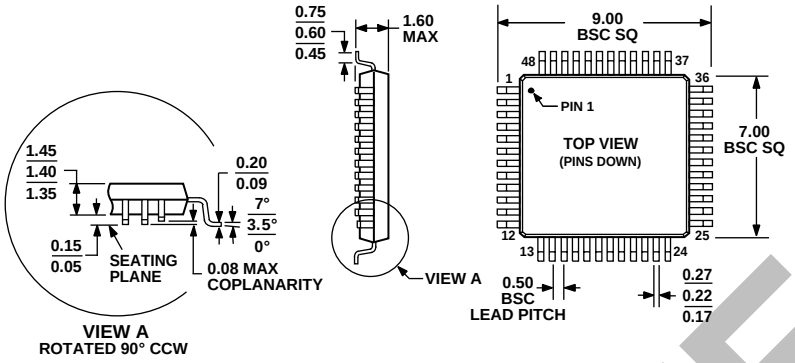

Figure 9. 48-Lead Low-Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions are shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1970JSTZ[1]	0°C to 70°C	48-Lead LQFP	ST-48
AD1970JSTZRL[1]	0°C to 70°C	48-Lead LQFP on 13-inch Reel	ST-48

[1] Z = Pb-free part.

NOTES

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