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REVISION HISTORY

| | | | |
|--|----|--|----|
| 12/11—Rev. 0 to Rev. A | | Changes to Table 7..... | 14 |
| Changes to Features Section..... | 1 | Changes to Table 8..... | 15 |
| Changes to Table 1..... | 3 | Changes to Table 9..... | 16 |
| Changes to Figure 6 and Figure 9..... | 7 | Changes to Table 12, Table 13, and Table 14..... | 17 |
| Changes to Figure 11 | 8 | Changes to Ordering Guide | 24 |
| Changes to One-Shot Mode Section and 1 SPS Mode Section..... | 10 | | |
| Changes to Shutdown Section and Figure 16 | 12 | 4/09—Revision 0: Initial Version | |

SPECIFICATIONS

$T_A = -55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{DD} = 2.7\text{ V}$ to 5.5 V ; unless otherwise noted.

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------------|---------------------|-------------|-------------|-----------------------------|--|
| TEMPERATURE SENSOR AND ADC | | | | | |
| Accuracy ¹ | | -0.05 | $\pm 0.4^2$ | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$ |
| | | | ± 0.44 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 2.7\text{ V}$ to 3.3 V |
| | | | ± 0.5 | $^{\circ}\text{C}$ | $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$ |
| | | | ± 0.5 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 2.7\text{ V}$ to 3.6 V |
| | | | ± 0.7 | $^{\circ}\text{C}$ | $T_A = -55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{DD} = 2.7\text{ V}$ to 3.6 V |
| | | | ± 0.8 | $^{\circ}\text{C}$ | $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 4.5\text{ V}$ to 5.5 V |
| | | | ± 1.0 | $^{\circ}\text{C}$ | $T_A = -55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{DD} = 2.7\text{ V}$ to 5.5 V |
| ADC Resolution | | 13 | | Bits | Twos complement temperature value of sign bit plus 12 ADC bits (power-up default resolution) |
| | | 16 | | Bits | Twos complement temperature value of sign bit plus 15 ADC bits (Bit 7 = 1 in the configuration register) |
| Temperature Resolution | | | | | |
| 13-Bit | | 0.0625 | | $^{\circ}\text{C}$ | 13-bit resolution (sign + 12-bit) |
| 16-Bit | | 0.0078 | | $^{\circ}\text{C}$ | 16-bit resolution (sign + 15-bit) |
| Temperature Conversion Time | | 240 | | ms | Continuous conversion and one-shot conversion mode |
| Fast Temperature Conversion Time | | 6 | | ms | First conversion on power-up only |
| 1 SPS Conversion Time | | 60 | | ms | Conversion time for 1 SPS mode |
| Temperature Hysteresis | | ± 0.002 | | $^{\circ}\text{C}$ | Temperature cycle = 25°C to 125°C , and back to 25°C |
| Repeatability ³ | | ± 0.015 | | $^{\circ}\text{C}$ | $T_A = 25^{\circ}\text{C}$ |
| DC PSRR | | 0.1 | | $^{\circ}\text{C}/\text{V}$ | $T_A = 25^{\circ}\text{C}$ |
| DIGITAL OUTPUTS (OPEN DRAIN) | | | | | |
| High Output Leakage Current, I_{OH} | | 0.1 | 5 | μA | CT and INT pins pulled up to 5.5 V |
| Output High Current | | | 1 | mA | $V_{OH} = 5.5\text{ V}$ |
| Output Low Voltage, V_{OL} | | | 0.4 | V | $I_{OL} = 2\text{ mA}$ @ 5.5 V , $I_{OL} = 1\text{ mA}$ @ 3.3 V |
| Output High Voltage, V_{OH} | $0.7 \times V_{DD}$ | | | V | |
| Output Capacitance, C_{OUT} | | 3 | | pF | |
| DIGITAL INPUTS | | | | | |
| Input Current | | | ± 1 | μA | $V_{IN} = 0\text{ V}$ to V_{DD} |
| Input Low Voltage, V_{IL} | | | 0.4 | V | |
| Input High Voltage, V_{IH} | $0.7 \times V_{DD}$ | | | V | |
| Pin Capacitance | | 5 | 10 | pF | |
| DIGITAL OUTPUT (DOUT) | | | | | |
| Output High Voltage, V_{OH} | $V_{OH} - 0.3$ | | | V | $I_{SOURCE} = I_{SINK} = 200\ \mu\text{A}$ |
| Output Low Voltage, V_{OL} | | | 0.4 | V | $I_{OL} = 200\ \mu\text{A}$ |
| Output Capacitance, C_{OUT} | | | 50 | pF | |
| POWER REQUIREMENTS | | | | | |
| Supply Voltage | 2.7 | | 5.5 | V | |
| Supply Current | | | | | |
| At 3.3 V | | 210 | 250 | μA | Peak current while converting, SPI interface inactive |
| At 5.5 V | | 250 | 300 | μA | Peak current while converting, SPI interface inactive |
| 1 SPS Current | | | | | |
| At 3.3V | | 46 | | μA | $V_{DD} = 3.3\text{ V}$, 1 SPS mode, $T_A = 25^{\circ}\text{C}$ |
| At 5.5V | | 65 | | μA | $V_{DD} = 5.5\text{ V}$, 1 SPS mode, $T_A = 25^{\circ}\text{C}$ |
| Shutdown Current | | | | | |
| At 3.3 V | | 2.0 | 15 | μA | Supply current in shutdown mode |
| At 5.5 V | | 5.2 | 25 | μA | Supply current in shutdown mode |
| Power Dissipation Normal Mode | | 700 | | μW | $V_{DD} = 3.3\text{ V}$, normal mode at 25°C |
| Power Dissipation 1 SPS | | 150 | | μW | Power dissipated for $V_{DD} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$ |

¹ Accuracy includes lifetime drift.

² The equivalent 3 σ limits are $\pm 0.33^{\circ}\text{C}$. This 3 σ specification is provided to enable comparison with other vendors who use these limits.

³ Based on a floating average of 10 readings.

SPI TIMING SPECIFICATIONS

$T_A = -55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{DD} = 2.7\text{ V}$ to 5.5 V , unless otherwise noted. All input signals are specified with rise time (t_r) = fall time (t_f) = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V .

Table 2.

| Parameter ^{1,2} | Limit at T_{MIN} , T_{MAX} (B Version) | Unit | Conditions/Comments |
|--------------------------|--|--------|--|
| t_1 | 0 | ns min | \overline{CS} falling edge to SCLK active edge setup time ³ |
| t_2 | 100 | ns min | SCLK high pulse width |
| t_3 | 100 | ns min | SCLK low pulse width |
| t_4 | 30 | ns min | Data valid to SCLK edge setup time |
| t_5 | 25 | ns min | Data valid to SCLK edge hold time |
| t_6 | 0 | ns min | SCLK active edge to data valid delay ³ |
| | 60 | ns max | $V_{DD} = 4.5\text{ V}$ to 5.5 V |
| | 80 | ns max | $V_{DD} = 2.7\text{ V}$ to 3.6 V |
| t_7^4 | 10 | ns min | Bus relinquish time after \overline{CS} inactive edge |
| | 80 | ns max | |
| t_8 | 0 | ns min | \overline{CS} rising edge to SCLK edge hold time |
| t_9 | 0 | ns min | \overline{CS} falling edge to DOUT active time |
| | 60 | ns max | $V_{DD} = 4.5\text{ V}$ to 5.5 V |
| | 80 | ns max | $V_{DD} = 2.7\text{ V}$ to 3.6 V |
| t_{10} | 10 | ns min | SCLK inactive edge to DOUT high |

¹ Sample tested during initial release to ensure compliance. All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V .

² See Figure 2.

³ SCLK active edge is falling edge of SCLK.

⁴ This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

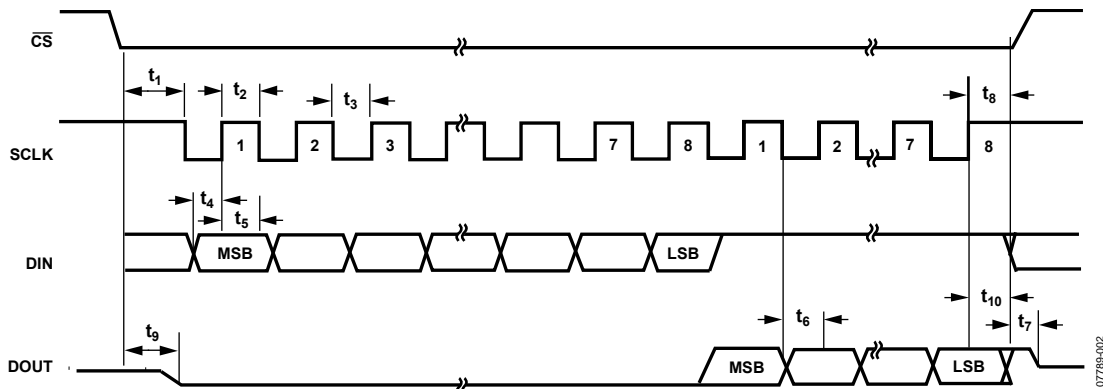


Figure 2. Detailed SPI Timing Diagram

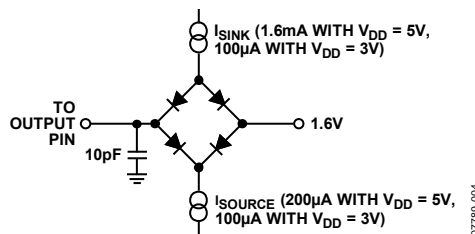


Figure 3. Load Circuit for Timing Characterization

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|---|--|
| V _{DD} to GND | -0.3 V to +7 V |
| DIN Input Voltage to GND | -0.3 V to V _{DD} + 0.3 V |
| DOOUT Voltage to GND | -0.3 V to V _{DD} + 0.3 V |
| SCLK Input Voltage to GND | -0.3 V to V _{DD} + 0.3 V |
| CS Input Voltage to GND | -0.3 V to V _{DD} + 0.3 V |
| CT and INT Output Voltage to GND | -0.3 V to V _{DD} + 0.3 V |
| ESD Rating (Human Body Model) | 2.0 kV |
| Operating Temperature Range | -55°C to +150°C |
| Storage Temperature Range | -65°C to +160°C |
| Maximum Junction Temperature, T _{JMAX} | 150°C |
| 8-Lead SOIC-N (R-8) | |
| Power Dissipation ¹ | $W_{MAX} = (T_{JMAX} - T_A) / \theta_{JA}$ |
| Thermal Impedance ³ | |
| θ _{JA} , Junction-to-Ambient (Still Air) | 121°C/W |
| θ _{JC} , Junction-to-Case | 56°C/W |
| IR Reflow Soldering | 220°C |
| Peak Temperature (RoHS-Compliant Package) | 260°C (0°C) |
| Time at Peak Temperature | 20 sec to 40 sec |
| Ramp-Up Rate | 3°C/sec maximum |
| Ramp-Down Rate | -6°C/sec maximum |
| Time from 25°C to Peak Temperature | 8 minutes maximum |

¹ Values relate to package being used on a standard 2-layer PCB. This gives a worst-case θ_{JA} and θ_{JC}. See Figure 4 for a plot of maximum power dissipation vs. ambient temperature (T_A).

² T_A = ambient temperature.

³ Junction-to-case resistance is applicable to components featuring a preferential flow direction, for example, components mounted on a heat sink. Junction-to-ambient is more useful for air-cooled, PCB-mounted components.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

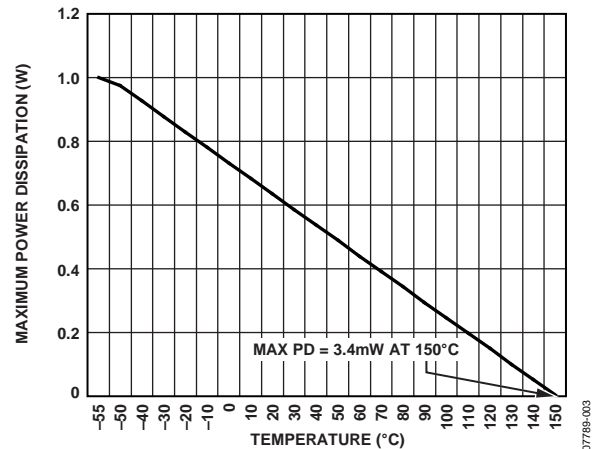


Figure 4. SOIC_N Maximum Power Dissipation vs. Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

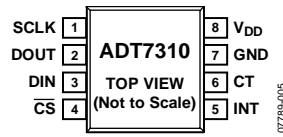


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------------|--|
| 1 | SCLK | Serial Clock Input. The serial clock is used to clock in and clock out data to and from any register of the ADT7310. |
| 2 | DOUT | Serial Data Output. Data is clocked out on the SCLK falling edge and is valid on the SCLK rising edge. |
| 3 | DIN | Serial Data Input. Serial data to be loaded to the part's control registers is provided on this input. Data is clocked into the registers on the rising edge of SCLK. |
| 4 | $\overline{\text{CS}}$ | Chip Select Input. The device is selected when this input is low. The device is disabled when this pin is high. |
| 5 | INT | Overtemperature and Undertemperature Indicator. Logic output. Power-up default setting is as an active low comparator interrupt. Open-drain configuration. A pull-up resistor is required, typically 10 k Ω . |
| 6 | CT | Critical Overtemperature Indicator. Logic output. Power-up default polarity is active low. Open-drain configuration. A pull-up resistor is required, typically 10 k Ω . |
| 7 | GND | Analog and Digital Ground. |
| 8 | V _{DD} | Positive Supply Voltage (2.7 V to 5.5 V). The supply should be decoupled with a 0.1 μF ceramic capacitor to ground. |

TYPICAL PERFORMANCE CHARACTERISTICS

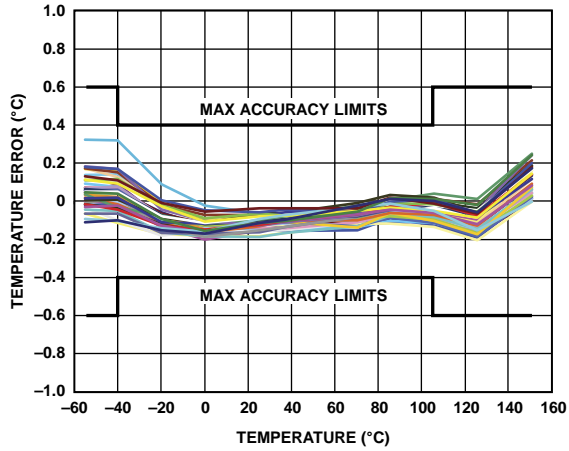


Figure 6. Temperature Accuracy at 3 V

07789-006

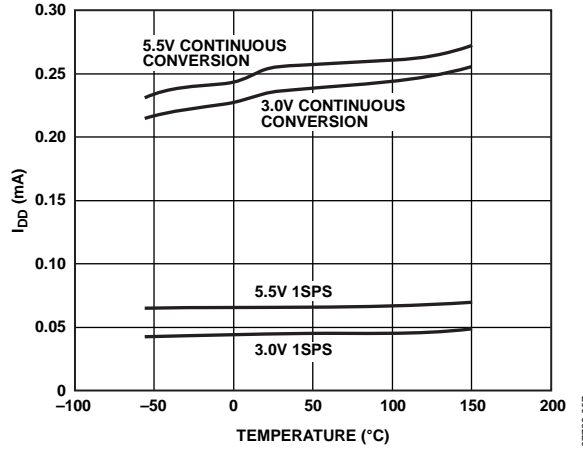


Figure 8. Operating Supply Current vs. Temperature

07789-007

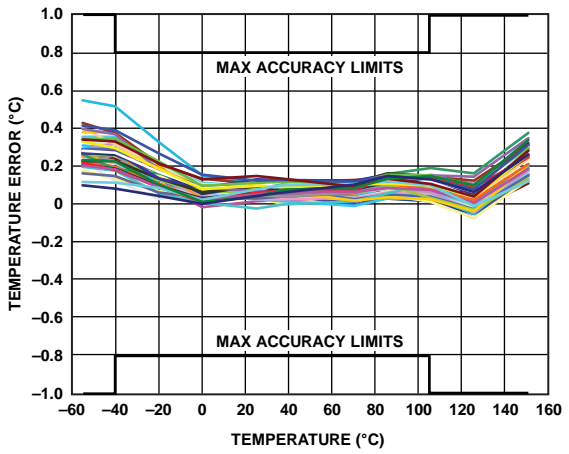


Figure 7. Temperature Accuracy at 5 V

07789-024

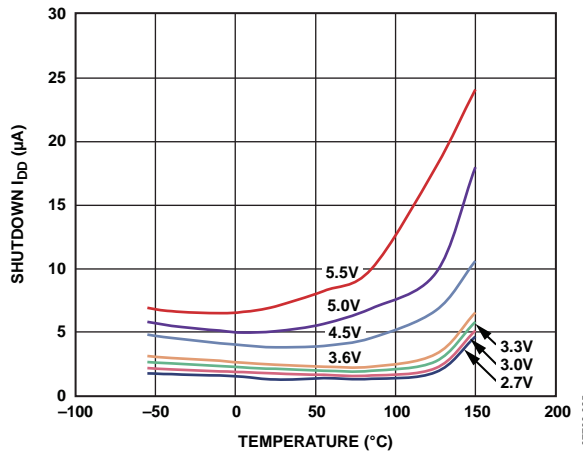


Figure 9. Shutdown Current vs. Temperature

07789-025

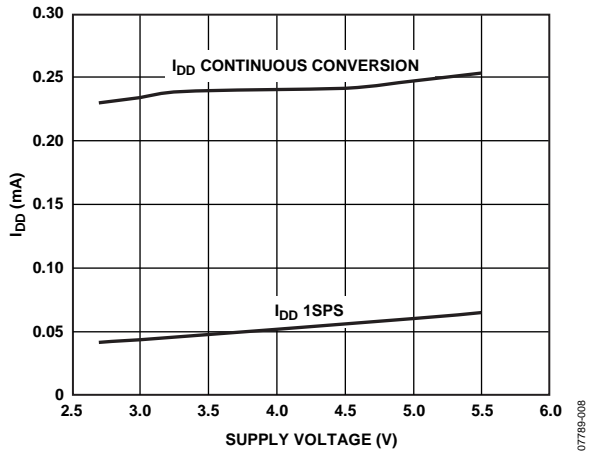


Figure 10. Average Operating Supply Current vs. Supply Voltage at 25°C

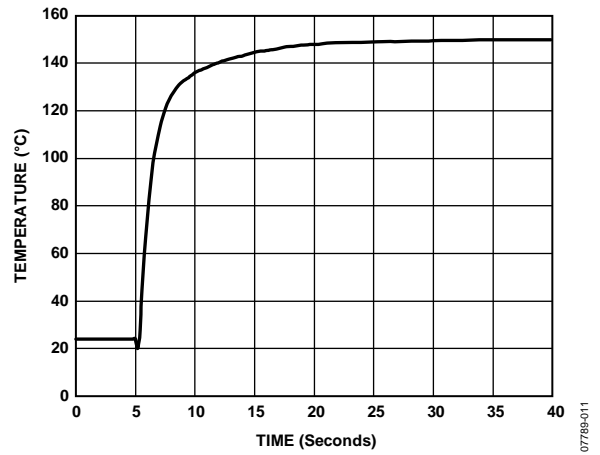


Figure 12. Response to Thermal Shock

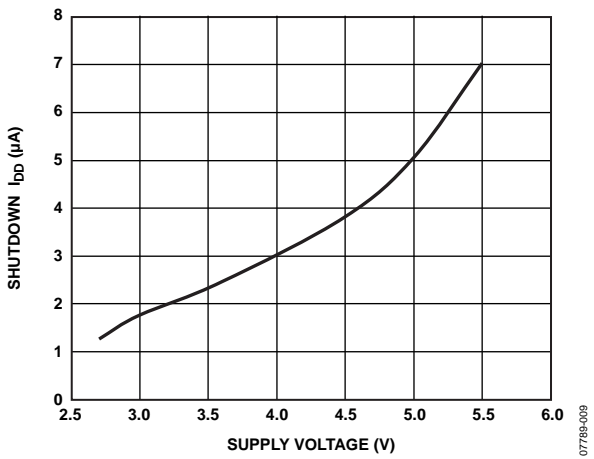


Figure 11. Shutdown Current vs. Supply Voltage at 25°C

THEORY OF OPERATION

CIRCUIT INFORMATION

The ADT7310 is a 13-bit digital temperature sensor that is extendable to 16-bits for greater resolution. An on-board temperature sensor generates a voltage proportional to absolute temperature, which is compared to an internal voltage reference and input to a precision digital modulator.

The on-board temperature sensor has excellent accuracy and linearity over the entire rated temperature range without needing correction or calibration by the user.

The sensor output is digitized by a sigma-delta (Σ - Δ) modulator, also known as the charge balance type analog-to-digital converter. This type of converter utilizes time-domain oversampling and a high accuracy comparator to deliver 16-bits of resolution in an extremely compact circuit.

Configuration register functions consist of

- Switching between 13-bit and 16-bit resolution
- Switching between normal operation and full power-down
- Switching between comparator and interrupt event modes on the INT and CT pins
- Setting the active polarity of the CT and INT pins
- Setting the number of faults that activate CT and INT
- Enabling the standard one-shot mode and 1 SPS mode

CONVERTER DETAILS

The Σ - Δ modulator consists of an input sampler, a summing network, an integrator, a comparator, and a 1-bit DAC. This architecture creates a negative feedback loop and minimizes the integrator output by changing the duty cycle of the comparator output in response to input voltage changes. The comparator samples the output of the integrator at a much higher rate than the input sampling frequency. This oversampling spreads the quantization noise over a much wider band than that of the input signal, improving overall noise performance and increasing accuracy.

The modulated output of the comparator is encoded using a circuit technique that results in SPI temperature data.

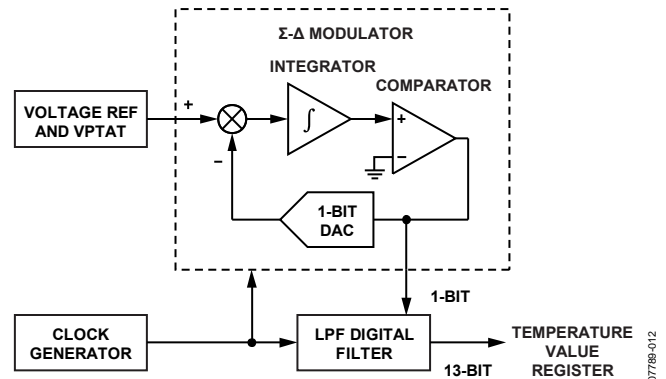


Figure 13. Σ - Δ Modulator

TEMPERATURE MEASUREMENT

In normal mode, the ADT7310 runs an automatic conversion sequence. During this automatic conversion sequence, a conversion takes 240 ms to complete and the ADT7310 is continuously converting. This means that as soon as one temperature conversion is completed, another temperature conversion begins. Each temperature conversion result is stored in the temperature value register and is available through the SPI interface. In continuous conversion mode, the read operation provides the most recent converted result.

On power-up, the first conversion is a fast conversion, taking typically 6 ms. If the temperature exceeds 147°C, the CT pin asserts low. If the temperature exceeds 64°C, the INT pin asserts low. Fast conversion temperature accuracy is typically within $\pm 5^\circ\text{C}$.

The conversion clock for the part is generated internally. No external clock is required except when reading from and writing to the serial port.

The measured temperature value is compared with a critical temperature limit (stored in the 16-bit T_{CRIT} setpoint read/write register), a high temperature limit (stored in the 16-bit T_{HIGH} setpoint read/write register), and a low temperature limit (stored in the 16-bit T_{LOW} setpoint read/write register). If the measured value exceeds these limits, the INT pin is activated; and if it exceeds the T_{CRIT} limit, the CT pin is activated. The INT and CT pins are programmable for polarity via the configuration register, and the INT and CT pins are also programmable for interrupt mode via the configuration register.

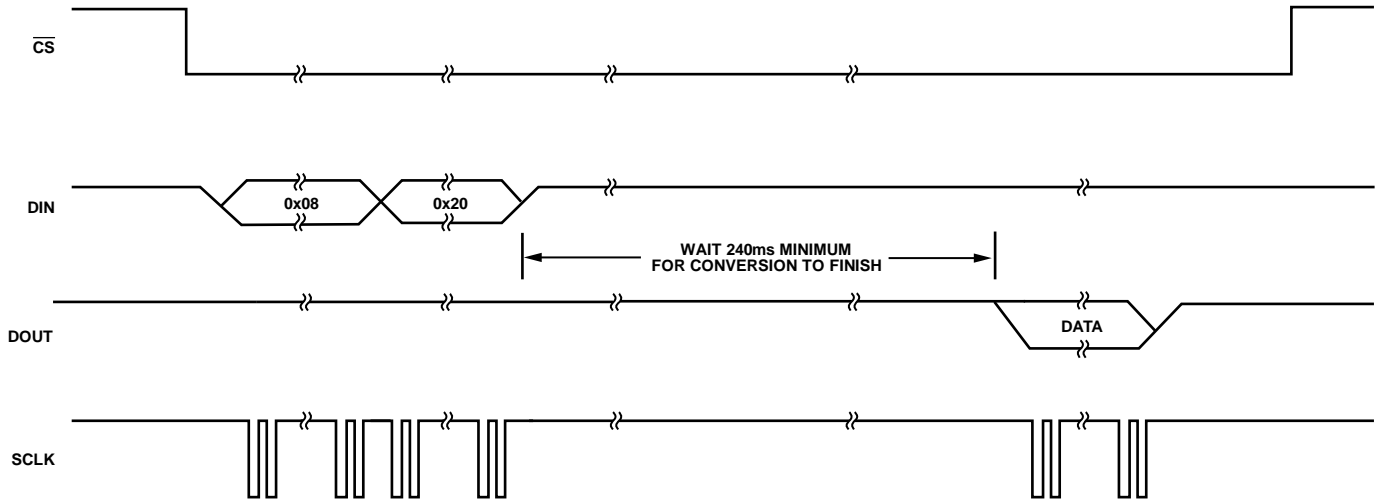


Figure 14. Typical SPI One-Shot Write to Configuration Register Followed by a Read from the Temperature Value Register

07789-026

ONE-SHOT MODE

When one-shot mode is enabled, the ADT7310 immediately completes a conversion and then goes into shutdown mode. The one-shot mode is useful when one of the circuit design priorities is to reduce power consumption.

To enable one-shot mode, set Bits[6:5] of the configuration register (Register Address 0x01) to 01.

After writing to the operation mode bits, wait at least 240 ms before reading back the temperature from the temperature value register. This delay ensures that the ADT7310 has adequate time to power up and complete a conversion.

To obtain an updated temperature conversion, reset Bits[6:5] of the configuration register (Register Address 0x01) to 01.

1 SPS MODE

In this mode, the part performs one measurement per second. A conversion takes only 60 ms, and it remains in the idle state for the remaining 940 ms period. This mode is enabled by writing 1 to Bit 6 and 0 to Bit 5 of the configuration register (Register Address 0x01).

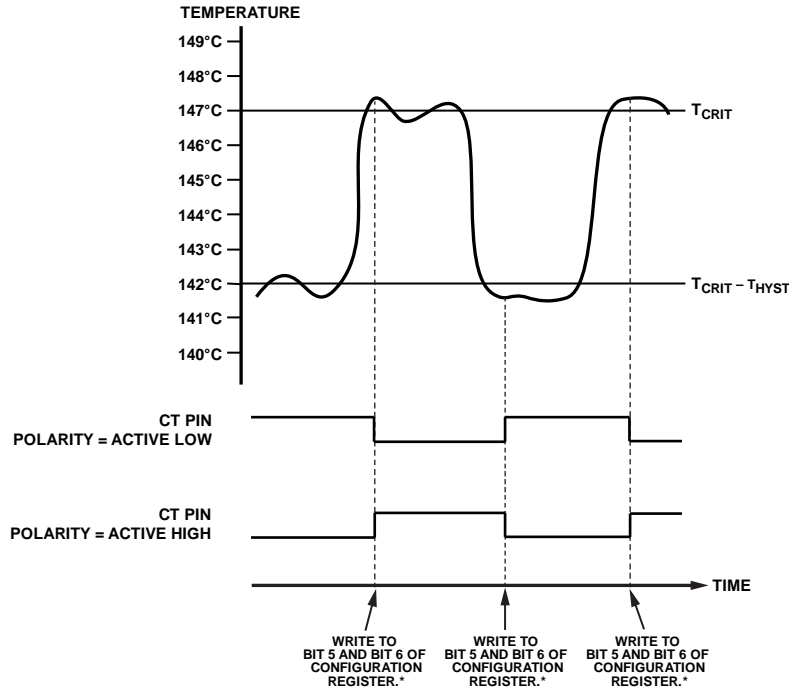
CT and INT Operation in One-Shot Mode

See Figure 15 for more information on one-shot CT pin operation for T_{CRIT} overtemperature events when one of the limits is exceeded. Note that in interrupt mode, a read from any register resets the INT and CT pins.

For the INT pin in the comparator mode, if the temperature drops below the $T_{HIGH} - T_{HYST}$ value or goes above the $T_{LOW} + T_{HYST}$ value, a write to the one-shot bits (Bit 5 and Bit 6 of the configuration register, Register Address 0x01) resets the INT pin.

For the CT pin in the comparator mode, if the temperature drops below the $T_{CRIT} - T_{HYST}$ value, a write to the one-shot bits (Bit 5 and Bit 6 of the configuration register, Register Address 0x01) resets the CT pin; see Figure 15.

Note that when using one-shot mode, ensure that the refresh rate is appropriate to the application being used.



*THERE IS A 240ms DELAY BETWEEN WRITING TO THE CONFIGURATION REGISTER TO START A STANDARD ONE-SHOT CONVERSION AND THE CT PIN GOING ACTIVE. THIS IS DUE TO THE CONVERSION TIME. THE DELAY IS 60ms IN THE CASE OF A ONE-SHOT CONVERSION.

07789-013

Figure 15. One-Shot CT Pin

CONTINUOUS READ MODE

When the command byte = 01010100 (0x54), the contents of the temperature value register can be read out without requiring repeated writes to the communications register. By sending 16 SCLK clocks to the ADT7310, the contents of the temperature value register are output onto the DOUT pin.

To exit the continuous read mode, the Command Byte 01010000 (0x50) must be written to the ADT7310.

While in continuous read mode, the part monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on the DIN pin. Therefore, hold DIN low in continuous read mode until an instruction is to be written to the device.

In continuous read mode, the temperature value register cannot be read when a conversion is taking place. If an attempt is made to read the temperature value register while a conversion is taking place, then all 0s are read. This is because the continuous read mode blocks read access to temperature value register during a conversion.

SHUTDOWN

The ADT7310 can be placed in shutdown mode by writing 1 to Bit 6 and 1 to Bit 5 of the configuration register (Register Address 0x01). The ADT7310 can be taken out of shutdown mode by writing 0 to Bit 6 and 0 to Bit 5 of the configuration register (Register Address 0x01). The ADT7310 typically takes 1 ms (with a 0.1 μ F decoupling capacitor) to come out of shutdown mode. The conversion result from the last conversion prior to shutdown can still be read from the ADT7310 even when it is in shutdown mode. When the part is taken out of shutdown mode, the internal clock is started and a conversion is initiated.

FAULT QUEUE

Bit 0 and Bit 1 of the configuration register (Register Address 0x01) are used to set up a fault queue. Up to four faults are provided to prevent false tripping of the INT and CT pins when the ADT7310 is used in a noisy temperature environment. The number of faults set in the queue must occur consecutively to set the INT and CT outputs. For example, if the number of faults set in the queue is four, then four consecutive temperature conversions must occur, with each result exceeding a temperature limit in any of the limit registers, before the INT and CT pins are activated. If two consecutive temperature conversions exceed a temperature limit and the third conversion does not, the fault count is reset to zero.

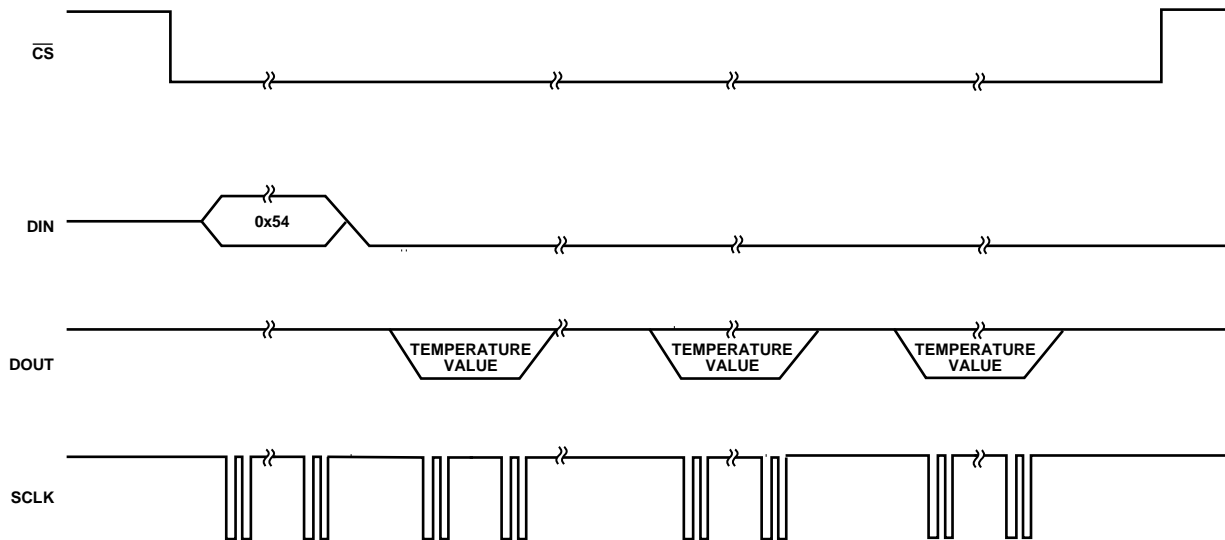


Figure 16. Continuous Read Mode

07789-027

TEMPERATURE DATA FORMAT

One LSB of the ADC corresponds to 0.0625°C in 13-bit mode. The ADC can theoretically measure a temperature range of 255°C, but the ADT7310 is guaranteed to measure a low value temperature limit of -55°C to a high value temperature limit of +150°C. The temperature measurement result is stored in the 16-bit temperature value register and is compared with the high temperature limits stored in the T_{CRIT} setpoint register and the T_{HIGH} setpoint register. It is also compared with the low temperature limit stored in the T_{LOW} setpoint register.

Temperature data in the temperature value register, the T_{CRIT} setpoint register, the T_{HIGH} setpoint register, and the T_{LOW} setpoint register are represented by a 13-bit twos complement word. The MSB is the temperature sign bit. The three LSBs, Bit 0 to Bit 2, on power-up, are not part of the temperature conversion result and are flag bits for T_{CRIT} , T_{HIGH} , and T_{LOW} . Table 5 shows the 13-bit temperature data format without Bit 0 to Bit 2.

The number of bits in the temperature data-word can be extended to 16 bits, twos complement, by setting Bit 7 to 1 in the configuration register (Register Address 0x01). When using a 16-bit temperature data value, Bit 0 to Bit 2 are not used as flag bits and are instead the LSB bits of the temperature value. The power-on default setting has a 13-bit temperature data value.

Reading back the temperature from the temperature value register requires a 2-byte read. Designers that use a 9-bit temperature data format can still use the ADT7310 by ignoring the last four LSBs of the 13-bit temperature value. These four LSBs are Bit 3 to Bit 6 in Table 5.

Table 5. 13-Bit Temperature Data Format

| Temperature | Digital Output (Binary) Bits[15:3] | Digital Output (Hex) |
|-------------|------------------------------------|----------------------|
| -55°C | 1 1100 1001 0000 | 0x1C90 |
| -50°C | 1 1100 1110 0000 | 0x1CE0 |
| -25°C | 1 1110 0111 0000 | 0x1E70 |
| -0.0625°C | 1 1111 1111 1111 | 0x1FFF |
| 0°C | 0 0000 0000 0000 | 0x000 |
| +0.0625°C | 0 0000 0000 0001 | 0x001 |
| +25°C | 0 0001 1001 0000 | 0x190 |
| +50°C | 0 0011 0010 0000 | 0x320 |
| +125°C | 0 0111 1101 0000 | 0x7D0 |
| +150°C | 0 1001 0110 0000 | 0x960 |

TEMPERATURE CONVERSION FORMULAS

16-Bit Temperature Data Format

$$\text{Positive Temperature} = \text{ADC Code}(\text{dec})/128$$

$$\text{Negative Temperature} = (\text{ADC Code}(\text{dec}) - 65,536)/128$$

where *ADC Code* uses all 16 bits of the data byte, including the sign bit.

$$\text{Negative Temperature} = (\text{ADC Code}(\text{dec}) - 32,768)/128$$

where the MSB is removed from the ADC code.

13-Bit Temperature Data Format

$$\text{Positive Temperature} = \text{ADC Code}(\text{dec})/16$$

$$\text{Negative Temperature} = (\text{ADC Code}(\text{dec}) - 8192)/16$$

where *ADC Code* uses all 13 bits of the data byte, including the sign bit.

$$\text{Negative Temperature} = (\text{ADC Code}(\text{dec}) - 4096)/16$$

where the MSB is removed from the ADC code.

10-Bit Temperature Data Format

$$\text{Positive Temperature} = \text{ADC Code}(\text{dec})/2$$

$$\text{Negative Temperature} = (\text{ADC Code}(\text{dec}) - 1024)/2$$

where *ADC Code* uses all 10 bits of the data byte, including the sign bit.

$$\text{Negative Temperature} = (\text{ADC Code}(\text{dec}) - 512)/2$$

where the MSB is removed from the ADC code.

9-Bit Temperature Data Format

$$\text{Positive Temperature} = \text{ADC Code}(\text{dec})$$

$$\text{Negative Temperature} = \text{ADC Code}(\text{dec}) - 512$$

where *ADC Code* uses all nine bits of the data byte, including the sign bit.

$$\text{Negative Temperature} = \text{ADC Code}(\text{dec}) - 256$$

where the MSB is removed from the ADC code.

REGISTERS

The ADT7310 contains eight registers:

- A status register
- A configuration register
- Five temperature registers
- An ID register

The status register, temperature value register, and the ID register are read-only.

Table 6. ADT7310 Registers

| Register Address | Description | Power-On Default |
|------------------|----------------------------|------------------|
| 0x00 | Status | 0x80 |
| 0x01 | Configuration | 0x00 |
| 0x02 | Temperature value | 0x0000 |
| 0x03 | ID | 0xCX |
| 0x04 | T _{CRIT} setpoint | 0x4980 (147°C) |
| 0x05 | T _{HYST} setpoint | 0x05 (5°C) |
| 0x06 | T _{HIGH} setpoint | 0x2000 (64°C) |
| 0x07 | T _{LOW} setpoint | 0x0500 (10°C) |

STATUS REGISTER

This 8-bit read-only register (Register Address 0x00) reflects the status of the overtemperature and undertemperature interrupts that can cause the CT and INT pins to go active. It also reflects the status of a temperature conversion operation. The interrupt flags in this register are reset by a read operation to the status register and/or when the temperature value returns within the temperature limits including hysteresis. The RDY bit is reset after a read from the temperature value register. In one-shot and 1 SPS modes, the RDY bit is reset after a write to the one-shot bits.

Table 7. Status Register (Register Address 0x00)

| Bit | Default Value | Type | Name | Description |
|-------|---------------|------|-------------------|---|
| [3:0] | 0000 | R | Unused | Reads back 0. |
| 4 | 0 | R | T _{LOW} | This bit is set to 1 when the temperature goes below the T _{LOW} temperature limit. The bit clears to 0 when the status register is read and/or when the temperature measured goes back above the limit set in the T _{LOW} + T _{HYST} setpoint registers. |
| 5 | 0 | R | T _{HIGH} | This bit is set to 1 when the temperature goes above the T _{HIGH} temperature limit. The bit clears to 0 when the status register is read and/or when the temperature measured goes back below the limit set in the T _{HIGH} – T _{HYST} setpoint registers. |
| 6 | 0 | R | T _{CRIT} | This bit is set to 1 when the temperature goes above the T _{CRIT} temperature limit. This bit clears to 0 when the status register is read and/or when the temperature measured goes back below the limit set in the T _{CRIT} – T _{HYST} setpoint registers. |
| 7 | 1 | R | RDY | This bit goes low when the temperature conversion result is written into the temperature value register. It is reset to 1 when the temperature value register is read. In one-shot and 1 SPS modes, this bit is reset after a write to the one-shot bits. |

CONFIGURATION REGISTER

This 8-bit read/write register stores various configuration modes for the ADT7310, including shutdown, overtemperature and

undertemperature interrupts, one-shot, continuous conversion, interrupt pins polarity, and overtemperature fault queues.

Table 8. Configuration Register (Register Address 0x01)

| Bit | Default Value | Type | Name | Description |
|-------|---------------|------|------------------|--|
| [1:0] | 00 | R/W | Fault queue | These two bits set the number of undertemperature/overtemperature faults that can occur before setting the INT and CT pins. This helps to avoid false triggering due to temperature noise. 00 = 1 fault (default). 01 = 2 faults. 10 = 3 faults. 11 = 4 faults. |
| 2 | 0 | R/W | CT pin polarity | This bit selects the output polarity of the CT pin. 0 = active low. 1 = active high. |
| 3 | 0 | R/W | INT pin polarity | This bit selects the output polarity of the INT pin. 0 = active low. 1 = active high. |
| 4 | 0 | R/W | INT/CT mode | This bit selects between comparator mode and interrupt mode. 0 = interrupt mode. 1 = comparator mode. |
| [6:5] | 00 | R/W | Operation mode | These two bits set the operational mode for the ADT7310. 00 = continuous conversion (default). When one conversion is finished, the ADT7310 starts another. 01 = one shot. Conversion time is typically 240 ms. 10 = 1 SPS mode. Conversion time is typically 60 ms. This operational mode reduces the average current consumption. 11 = shutdown. All circuitry except interface circuitry is powered down. |
| 7 | 0 | R/W | Resolution | This bit sets up the resolution of the ADC when converting. 0 = 13-bit resolution. Sign bit + 12 bits gives a temperature resolution of 0.0625°C. 1 = 16-bit resolution. Sign bit + 15 bits gives a temperature resolution of 0.0078125°C. |

TEMPERATURE VALUE REGISTER

The temperature value register stores the temperature measured by the internal temperature sensor. The temperature is stored as a 16-bit twos complement format. The temperature is read back from the temperature value register (Register Address 0x02) as a 16-bit value.

Bit 2, Bit 1, and Bit 0 are event alarm flags for T_{CRIT} , T_{HIGH} , and T_{LOW} . When the ADC is configured to convert the temperature to a 16-bit digital value, Bit 2, Bit 1, and Bit 0 are no longer used as flag bits and are, instead, used as the LSB bits for the extended digital value.

ID REGISTER

This 8-bit read-only register stores the manufacturer ID in Bit 7 to Bit 3 and the silicon revision in Bit 2 to Bit 0.

T_{CRIT} SETPOINT REGISTER

The 16-bit T_{CRIT} setpoint register (Register Address 0x04) stores the critical overtemperature limit value. A critical overtemperature event occurs when the temperature value stored in the temperature value register exceeds the value stored in this register. The CT pin is activated if a critical overtemperature event occurs. The temperature is stored in twos complement format with the MSB being the temperature sign bit.

The default setting for the T_{CRIT} setpoint is 147°C.

Table 9. Temperature Value Register (Register Address 0x02)

| Bit | Default Value | Type | Name | Description |
|--------|---------------|------|----------------------|--|
| 0 | 0 | R | T_{LOW} flag/LSB0 | Flags a T_{LOW} event if the configuration register, Register Address 0x01[7] = 0 (13-bit resolution). When the temperature value is below T_{LOW} , this bit is set to 1. Contains the Least Significant Bit 0 of the 15-bit temperature value if the configuration register, Register Address 0x01[7] = 1 (16-bit resolution). |
| 1 | 0 | R | T_{HIGH} flag/LSB1 | Flags a T_{HIGH} event if the configuration register, Register Address 0x01[7] = 0 (13-bit resolution). When the temperature value is above T_{HIGH} , this bit is set to 1. Contains the Least Significant Bit 1 of the 15-bit temperature value if the configuration register, Register Address 0x01[7] = 1 (16-bit resolution). |
| 2 | 0 | R | T_{CRIT} flag/LSB2 | Flags a T_{CRIT} event if the configuration register, Register Address 0x01[7] = 0 (13-bit resolution). When the temperature value exceeds T_{CRIT} , this bit is set to 1. Contains the Least Significant Bit 2 of the 15-bit temperature value if the configuration register, Register Address 0x01[7] = 1 (16-bit resolution). |
| [7:3] | 00000 | R | Temp | Temperature value in twos complement format. |
| [14:8] | 0000000 | R | Temp | Temperature value in twos complement format. |
| 15 | 0 | R | Sign | Sign bit, indicates if the temperature value is negative or positive. |

Table 10. ID Register (Register Address 0x03)

| Bit | Default Value | Type | Name | Description |
|-------|---------------|------|----------------|--|
| [2:0] | XXX | R | Revision ID | Contains the silicon revision identification number. |
| [7:3] | 11000 | R | Manufacture ID | Contains the manufacturer identification number. |

Table 11. T_{CRIT} Setpoint Register (Register Address 0x04)

| Bit | Default Value | Type | Name | Description |
|--------|---------------|------|------------|--|
| [15:0] | 0x4980 | R/W | T_{CRIT} | 16-bit critical overtemperature limit, stored in twos complement format. |

T_{HYST} SETPOINT REGISTER

The T_{HYST} setpoint 8-bit register (Register Address 0x05) stores the temperature hysteresis value for the T_{HIGH}, T_{LOW}, and T_{CRIT} temperature limits. The temperature hysteresis value is stored in straight binary format using four LSBs. Increments are possible in steps of 1°C from 0°C to 15°C. The value in this register is subtracted from the T_{HIGH} and T_{CRIT} values and added to the T_{LOW} value to implement hysteresis.

The default setting for the T_{HYST} setpoint is 5°C.

T_{HIGH} SETPOINT REGISTER

The 16-bit T_{HIGH} setpoint register (Register Address 0x06) stores the overtemperature limit value. An overtemperature event occurs when the temperature value stored in the temperature value register exceeds the value stored in this register. The INT pin

is activated if an overtemperature event occurs. The temperature is stored in twos complement format with the most significant bit being the temperature sign bit.

The default setting for the T_{HIGH} setpoint is 64°C.

T_{LOW} SETPOINT REGISTER

The 16-bit T_{LOW} setpoint register (Register Address 0x07) stores the undertemperature limit value. An undertemperature event occurs when the temperature value stored in the temperature value register is less than the value stored in this register. The INT pin is activated if an undertemperature event occurs. The temperature is stored in twos complement format with the MSB being the temperature sign bit.

The default setting for the T_{LOW} setpoint is 10°C.

Table 12. T_{HYST} Setpoint Register (Register Address 0x05)

| Bit | Default Value | Type | Name | Description |
|-------|---------------|-------------------|-------------------|---|
| [3:0] | 0101 | R/ \overline{W} | T _{HYST} | Hysteresis value, from 0°C to 15°C. Stored in straight binary format. The default setting is 5°C. |
| [7:4] | 0000 | R/ \overline{W} | N/A | Not used. |

Table 13. T_{HIGH} Setpoint Register (Register Address 0x06)

| Bit | Default Value | Type | Name | Description |
|--------|---------------|-------------------|-------------------|---|
| [15:0] | 0x2000 | R/ \overline{W} | T _{HIGH} | 16-bit overtemperature limit, stored in twos complement format. |

Table 14. T_{LOW} Setpoint Register (Register Address 0x07)

| Bit | Default Value | Type | Name | Description |
|--------|---------------|-------------------|------------------|--|
| [15:0] | 0x0500 | R/ \overline{W} | T _{LOW} | 16-bit undertemperature limit, stored in twos complement format. |

SERIAL INTERFACE

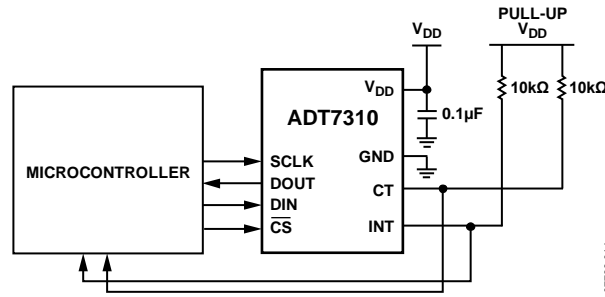


Figure 17. Typical SPI Interface Connection

The ADT7310 has a 4-wire serial peripheral interface (SPI). The interface has a data input pin (DIN) for inputting data to the device, a data output pin (DOUT) for reading data back from the device, and a data clock pin (SCLK) for clocking data into and out of the device. A chip select pin (\overline{CS}) enables or disables the serial interface. \overline{CS} is required for correct operation of the interface. Data is clocked out of the ADT7310 on the negative edge of SCLK, and data is clocked into the device on the positive edge of SCLK.

SPI COMMAND BYTE

All data transactions on the bus begin with the master taking \overline{CS} from high to low and sending out the command byte. This indicates to the ADT7310 whether the transaction is a read or a write and provides the address of the register for the data transfer. Table 15 shows the command byte.

Table 15. Command Byte

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|----|-----|------------------|----|----|-----------------|----|----|
| 0 | R/W | Register address | | | Continuous read | 0 | 0 |

Bit C7 of the command byte must be set to 0 to successfully begin a bus transaction. The SPI interface does not work correctly if a 1 is written into this bit.

Bit C6 is the read/write bit; 1 indicates a read, and 0 indicates a write.

Bits[C5:C3] contain the target register address. One register can be read from or written to per bus transaction.

Bit C2 activates a continuous read mode on the temperature value register only. When this bit is set, the serial interface is configured so that the temperature value register can be continuously read. When the command word is 01010100 (0x54), the contents of the temperature value register can be read out without requiring repeated writes to set the address bits. Simply sending 16 SCLK clocks to the ADT7310 clocks the contents of the temperature value register onto the DOUT pin.

WRITING DATA

Data is written to the ADT7310 in eight bits or 16 bits, depending on the addressed register. The first byte written to the device is the command byte, with the read/write bit set to 0. The master then supplies the 8-bit or 16-bit input data on the DIN line. The ADT7310 clocks the data into the register addressed in the command byte on the positive edge of SCLK. The master finishes the write by pulling \overline{CS} high.

Figure 18 shows a write to an 8-bit register, and Figure 19 shows a write to a 16-bit register.

The master must begin a new write transaction on the bus for every register write. Only one register is written to per bus transaction.

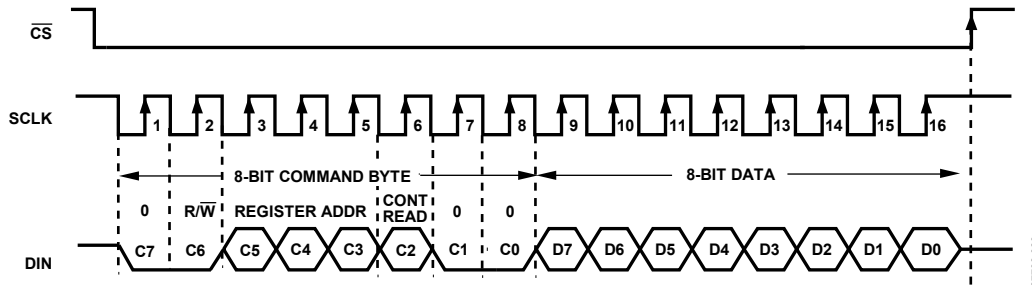


Figure 18. Writing to an 8-Bit Register

07789-028

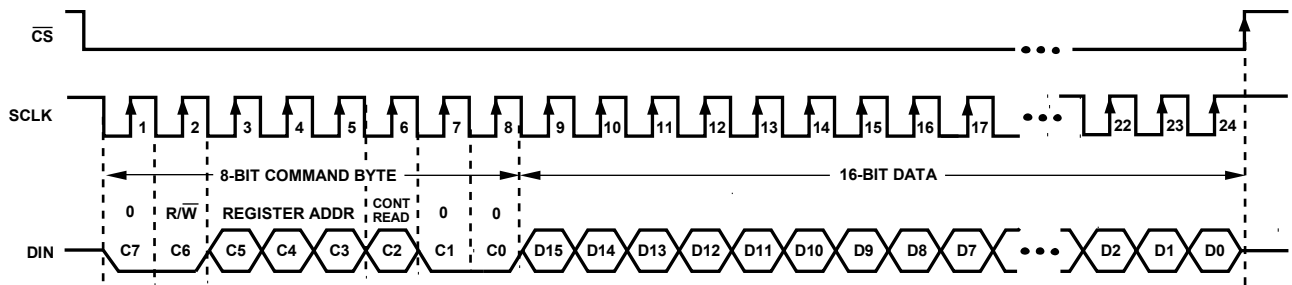


Figure 19. Writing to a 16-Bit Register

07789-029

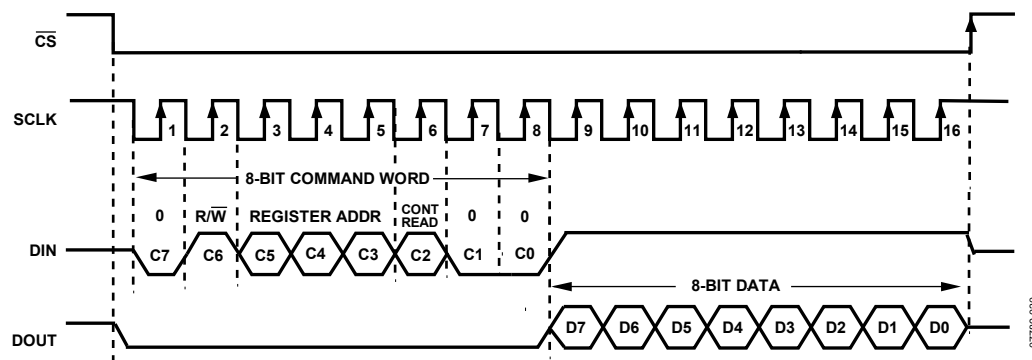


Figure 20. Read from an 8-Bit Register

07789-030

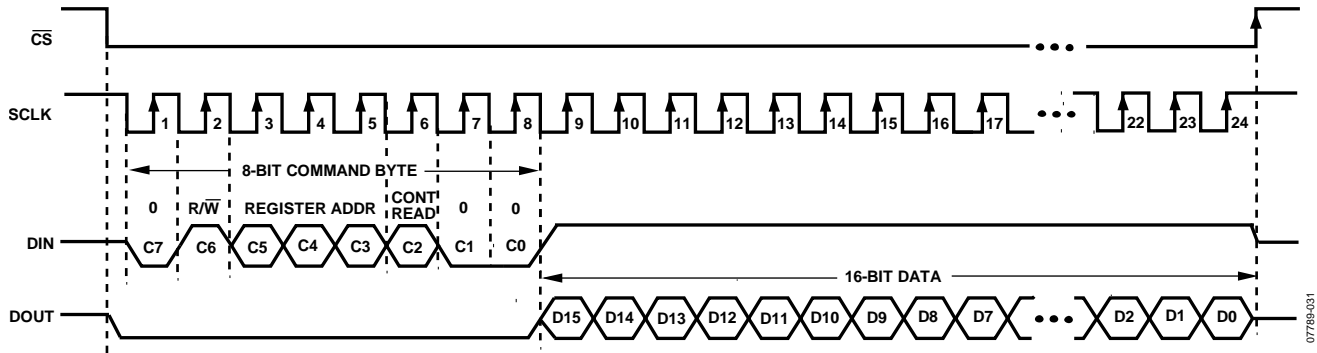


Figure 21. Read from a 16-Bit Register

READING DATA

A read transaction begins when the master writes the command byte to the ADT7310 with the read/write bit set to 1. The master then supplies 8 or 16 clock pulses, depending on the addressed register, and the ADT7310 clocks out data from the addressed register on the DOUT line. Data is clocked out on the first falling edge of SCLK following the command byte.

The read transaction finishes when the master takes $\overline{\text{CS}}$ high.

The master must begin a new read transaction on the bus for every register read. Only one register is read per bus transaction. However, in continuous read mode, Command Byte C2 = 1, and the temperature value register can be read from continuously. The master sends 16 clock pulses on SCLK, and the temperature value is clocked out on DOUT.

INTERFACING TO DSPs OR MICROCONTROLLERS

The ADT7310 can be operated with $\overline{\text{CS}}$ used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{\text{CS}}$ because $\overline{\text{CS}}$ normally occurs after the falling edge of SCLK in

DSPs. SCLK can continue to run between data transfers, provided that the timing numbers are obeyed.

$\overline{\text{CS}}$ can be tied to ground, and the serial interface can be operated in a 3-wire mode. DIN, DOUT, and SCLK are used to communicate with the ADT7310 in this mode.

For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

SERIAL INTERFACE RESET

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the ADT7310 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, the user should allow a period of 500 μs before addressing the serial interface.

INT AND CT OUTPUTS

The INT and CT pins are open drain outputs, and both pins require a 10 kΩ pull-up resistor to V_{DD}.

UNDERTEMPERATURE AND OVERTEMPERATURE DETECTION

The INT and CT pins have two undertemperature/over-temperature modes: comparator mode and interrupt mode. The interrupt mode is the default power-up overtemperature mode. The INT output pin becomes active when the temperature is greater than the temperature stored in the T_{HIGH} setpoint register or less than the temperature stored in the T_{LOW} setpoint register. How this pin reacts after this event depends on the overtemperature mode selected.

Figure 22 illustrates the comparator and interrupt modes for events exceeding the T_{HIGH} limit with both pin polarity settings. Figure 23 illustrates the comparator and interrupt modes for events exceeding the T_{LOW} limit with both pin polarity settings.

Comparator Mode

In comparator mode, the INT pin returns to its inactive status when the temperature drops below the T_{HIGH} - T_{HYST} limit or rises above the T_{LOW} + T_{HYST} limit.

Putting the ADT7310 into shutdown mode does not reset the INT state in comparator mode.

Interrupt Mode

In interrupt mode, the INT pin goes inactive when any ADT7310 register is read. Once the INT pin is reset, it goes active again only when the temperature is greater than the temperature stored in the T_{HIGH} setpoint register or less than the temperature stored in the T_{LOW} setpoint register.

Placing the ADT7310 into shutdown mode resets the INT pin in the interrupt mode.

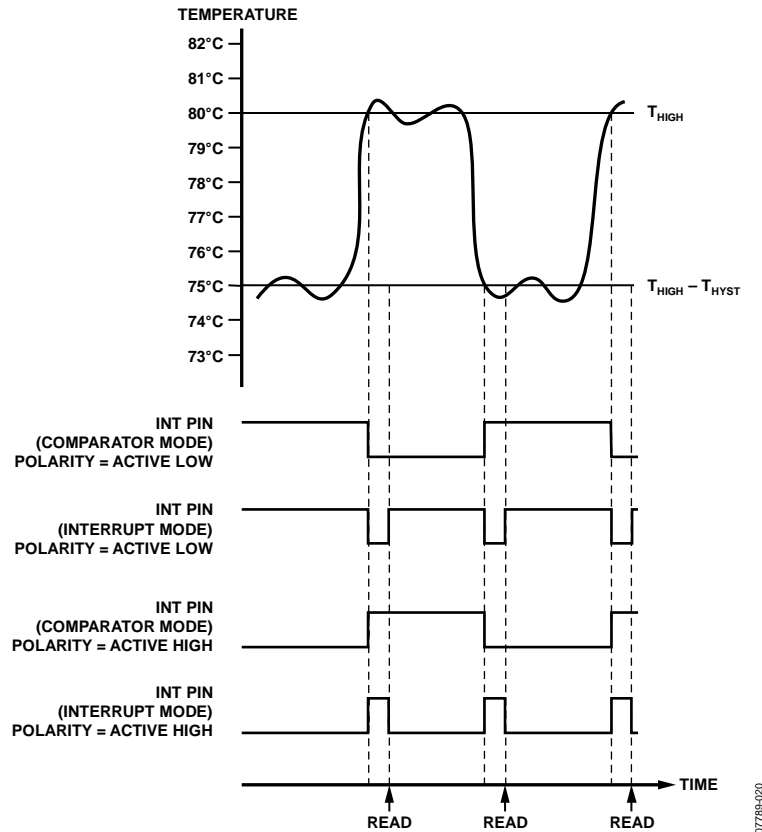


Figure 22. INT Output Temperature Response Diagram for T_{HIGH} Overtemperature Events

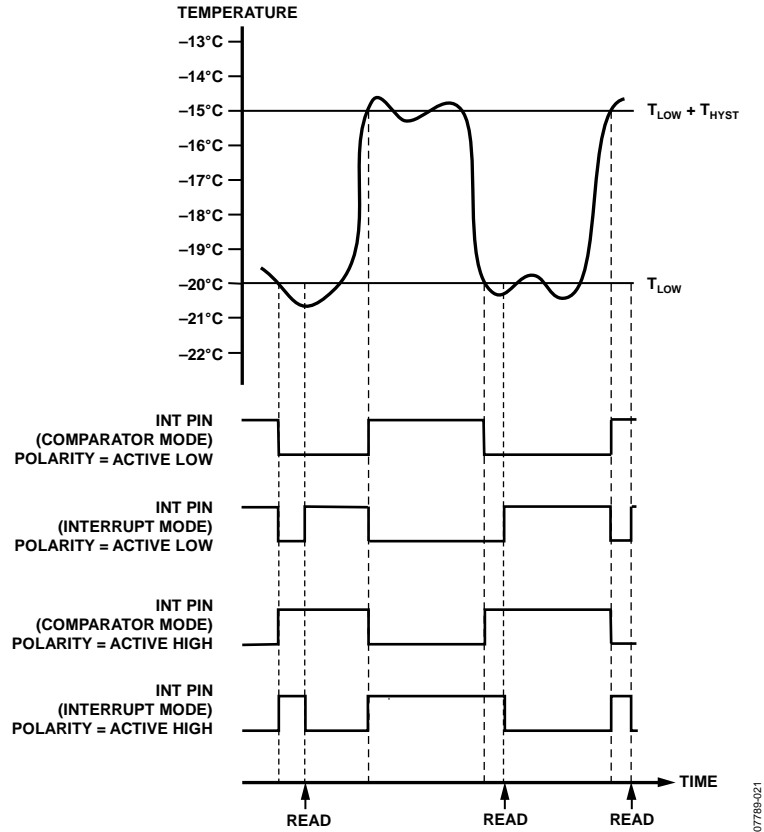


Figure 23. INT Output Temperature Response Diagram for T_{LOW} Undertemperature Events

APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

The time required for a temperature sensor to settle to a specified accuracy is a function of the thermal mass of the sensor and the thermal conductivity between the sensor and the object being sensed. Thermal mass is often considered equivalent to capacitance. Thermal conductivity is commonly specified using the symbol, Q , and can be thought of as thermal resistance. It is commonly specified in units of degrees per watt of power transferred across the thermal joint. The time required for the part to settle to the desired accuracy is dependent on the thermal contact established in that particular application, and the equivalent power of the heat source. In most applications, the settling time is best determined empirically.

SUPPLY DECOUPLING

The ADT7310 should be decoupled with a 0.1 μF ceramic capacitor between V_{DD} and GND. This is particularly important when the ADT7310 is mounted remotely from the power supply. Precision analog products, such as the ADT7310, require a well-filtered power source.

Because the ADT7310 operates from a single supply, it may seem convenient to tap into the digital logic power supply. Unfortunately, the logic supply is often a switch-mode design, which generates noise in the 20 kHz to 1 MHz range. In addition, fast logic gates can generate glitches hundreds of millivolts in amplitude due to wiring resistance and inductance.

If possible, the ADT7310 should be powered directly from the system power supply. This arrangement, shown in Figure 24, isolates the analog section from the logic-switching transients. Even if a separate power supply trace is not available, generous supply bypassing reduces supply-line induced errors. Local supply bypassing consisting of a 0.1 μF ceramic capacitor is critical for the temperature accuracy specifications to be achieved. This decoupling capacitor must be placed as close as possible to the V_{DD} pin of the ADT7310.

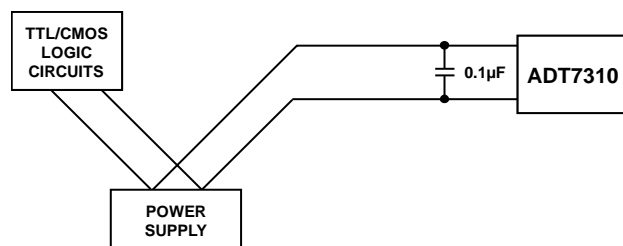


Figure 24. Use of Separate Traces to Reduce Power Supply Noise

TEMPERATURE MONITORING

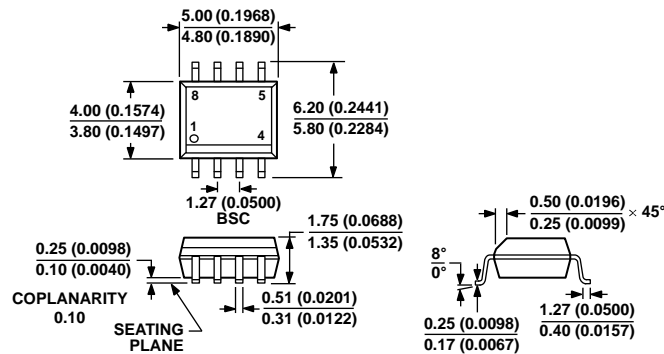
The ADT7310 is ideal for monitoring the thermal environment within hazardous automotive applications. The die accurately reflects the exact thermal conditions that affect nearby integrated circuits.

The ADT7310 measures and converts the temperature at the surface of its own semiconductor chip. When the ADT7310 is used to measure the temperature of a nearby heat source, the thermal impedance between the heat source and the ADT7310 must be considered.

When the thermal impedance is determined, the temperature of the heat source can be inferred from the ADT7310 output. As much as 60% of the heat transferred from the heat source to the thermal sensor on the ADT7310 die is discharged via the copper tracks and the bond pads. Of the pads on the ADT7310, the GND pad transfers most of the heat. Therefore, to measure the temperature of a heat source, it is recommended that the thermal resistance between the ADT7310 GND pad and the GND of the heat source be reduced as much as possible.

07789-022

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 25. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

| Model ¹ | Temperature Range | Temperature Accuracy ² | Package Description | Package Option |
|--------------------|-------------------|-----------------------------------|---------------------|----------------|
| ADT7310TRZ | -55°C to +150°C | ±0.5°C | 8-Lead SOIC_N | R-8 |
| ADT7310TRZ-REEL | -55°C to +150°C | ±0.5°C | 8-Lead SOIC_N | R-8 |
| ADT7310TRZ-REEL7 | -55°C to +150°C | ±0.5°C | 8-Lead SOIC_N | R-8 |
| EVAL-ADT7X10EBZ | | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

² Maximum accuracy over the -40°C to +105°C temperature range.

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