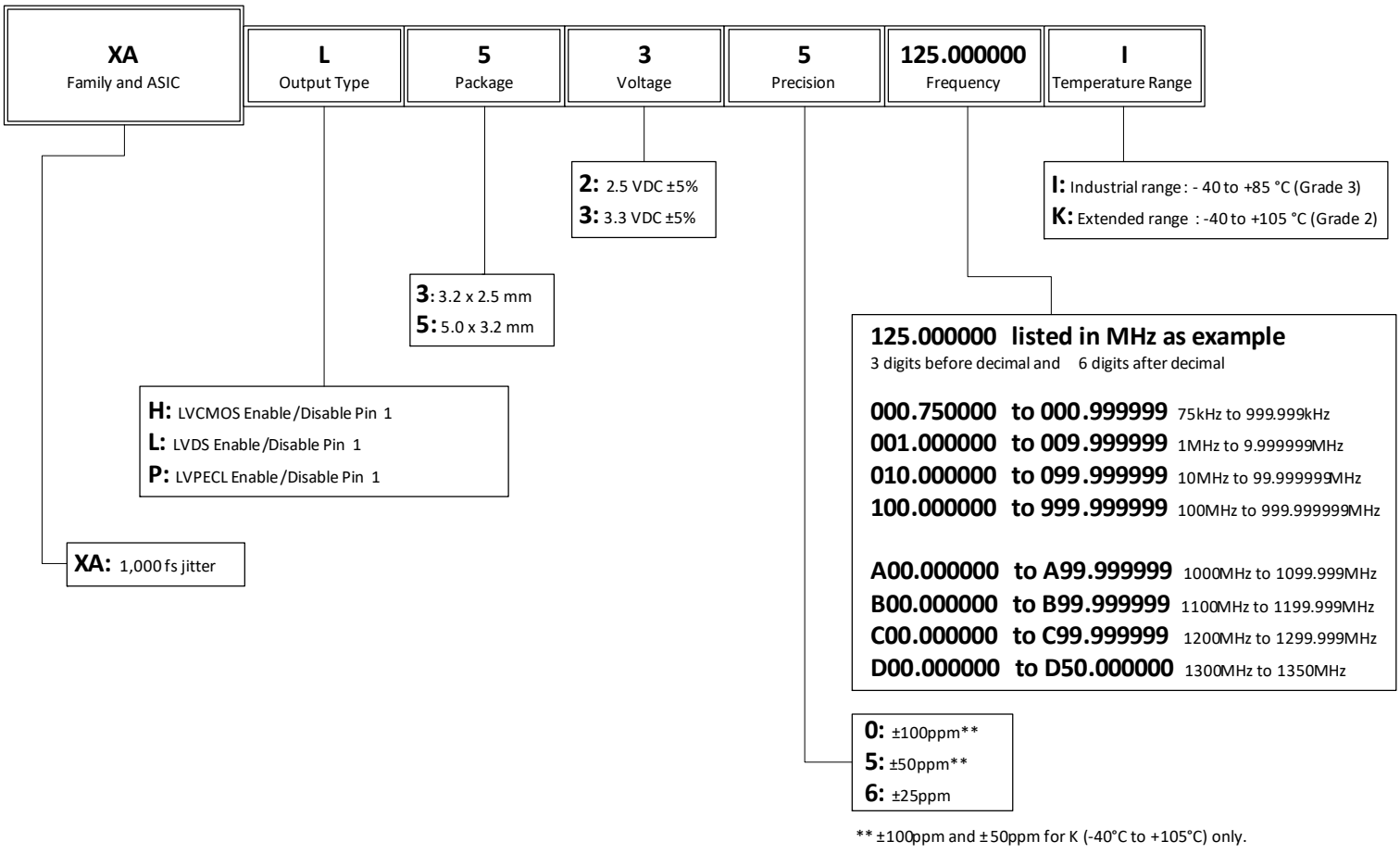
Ordering Information



** ±100ppm and ±50ppm for K (-40°C to +105°C) only.

Contents

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

Item	Rating			
V_{DD}	-0.5 to +5.0V			
E/D	-0.5V to V_{DD} + 0.5V			
OUT	-0.5V to V_{DD} + 0.5V			
Storage Temperature	-55°C to 125°C			
Maximum Junction Temperature	125°C			
Core Current	65mA maximum			
Theta J_A	JS6 5.0 × 3.2 × 1.2 mm	89.6 °C/W	JX6 3.2 × 2.5 × 1.0 mm	94.7 °C/W
Theta J_B		54.3 °C/W		66.8 °C/W

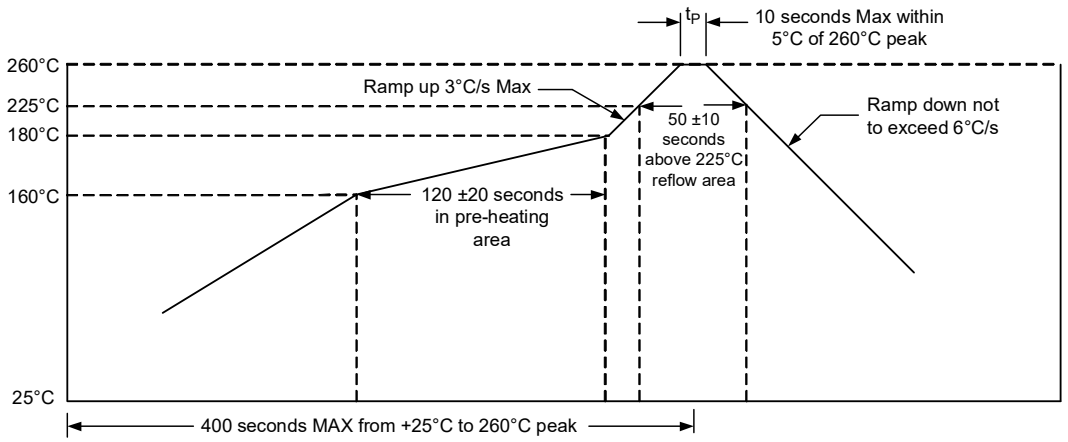
ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times.
Mechanical Vibration	10–55Hz, 1.5mm amplitude, 1 minute sweep; 2 hours each in 3 directions (X, Y, Z).
High Temperature Burn-in	Under power at 125°C for 2000 hours.
Hermetic Seal	He pressure: 4 ±1kgf/cm^2 2 hour soak.

Solder Reflow Profile



DC Electrical Characteristics

Table 3. 3.3V IDD DC Electrical Characteristics

V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current	LVDS	—	—	—	100	mA
		LVPECL	—	—	—	120	
		LVCMOS	0.75MHz to 20MHz.	—	—	32	
			20+MHz to 50MHz.	—	—	35	
			50+MHz to 130MHz.	—	—	47	
			130+MHz to 200MHz.	—	—	55	
			200+MHz to 250MHz.	—	—	60	

Table 4. 2.5V IDD DC Electrical Characteristics

V_{DD} = 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current	LVDS	0.75MHz to 20MHz.	—	—	26	mA
			20+MHz to 220MHz.	—	—	34	
			220+MHz to 630MHz.	—	—	44	
			630+MHz to 1000MHz.	—	—	65	
		LVPECL	0.75MHz to 20MHz.	—	—	33	
			20+MHz to 220MHz.	—	—	41	
			220+MHz to 630MHz.	—	—	63	
			630+MHz to 1000MHz.	—	—	72	
		LVCMOS	0.75MHz to 20MHz.	—	—	22	
			20+MHz to 50MHz.	—	—	25	
			50+MHz to 100MHz.	—	—	29	
			100+MHz to 130MHz.	—	—	32	
			130+MHz to 160MHz.	—	—	35	
			160+MHz to 180MHz.	—	—	37	

Table 5. LVDS DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	V_{DD} = 3.3V ±5%.	—	—	0.6	V
		V_{DD} = 2.5V ±5%.	—	—	0.4	
V_{OS}	Output Offset Voltage	V_{DD} = 3.3V ±5%.	—	—	1.3	
		V_{DD} = 2.5V ±5%.	—	—	1.25	
V_{IH}	Enable/Disable Input High Voltage (Output enabled)	—	70% V_{DD}	—	—	
V_{IL}	Enable/Disable Input Low Voltage (Output disabled)	—	—	—	30% V_{DD}	

Table 6. LVPECL DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	V_{DD} = 3.3V ±5%.	2.055		2.405	V
		V_{DD} = 2.5V ±5%.	—	1.4	—	
V_{OS}	Output Offset Voltage	V_{DD} = 3.3V ±5%.	1.305		1.65	
		V_{DD} = 2.5V ±5%.	—	0.68	—	
V_{IH}	Enable/Disable Input High Voltage (Output enabled)	—	70% V_{DD}	—	—	
V_{IL}	Enable/Disable Input Low Voltage (Output disabled)	—	—	—	30% V_{DD}	

Table 7. LVCMOS DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 3.3V ±5%.	0.75MHz to 150MHz.	90% V_{DD}	—	—	V
			150+MHz to 250MHz.	80% V_{DD}	—	—	
		V_{DD} = 2.5V ±5%.	0.75MHz to 160MHz.	90% V_{DD}	—	—	
			160+MHz to 180MHz.	80% V_{DD}	—	—	
V_{OL}	Output Low Voltage	V_{DD} = 3.3V ±5%.	0.75MHz to 150MHz.	—	—	10% V_{DD}	
			150+MHz to 250MHz.	—	—	20% V_{DD}	
		V_{DD} = 2.5V ±5%.	0.75MHz to 160MHz.	—	—	10% V_{DD}	
			160+MHz to 180MHz.	—	—	20% V_{DD}	
V_{IH}	Enable/Disable Input High Voltage (Output enabled)	—	—	70% V_{DD}	—	—	
V_{IL}	Enable/Disable Input Low Voltage (Output disabled)	—	—	—	—	30% V_{DD}	

AC Electrical Characteristics

Table 8. 3.3V AC Electrical Characteristics

V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.75	—	1350	MHz
		LVPECL.		0.75	—	1350	
		LVCMOS.		0.75	—	250	
	Frequency Stability	Temperature = -40°C to +85°C.		±25	—	±100	ppm
		Temperature = -40°C to +105°C.		±50	—	±100	ppm
	Aging (1st year)	T_A = 25°C.		—	—	±3	ppm
	Aging (10 years)	T_A = 25°C.		—	—	±10	ppm
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	V_{DD} - 2.0V.	—	50	—	
		LVCMOS.	To GND.	—	15	—	pF
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	—	10	ms
t_R	Output Rise Time	LVDS.	20% to 80% Vpp.	—	—	400	ps
		LVPECL.		—	—	400	
		LVCMOS.	10% to 90% V_{DD}.	—	—	3	ns
t_F	Output Fall Time	LVDS.	80% to 20% Vpp.	—	—	400	ps
		LVPECL.		—	—	400	
		LVCMOS.	90% to 10% V_{DD}.	—	—	3	ns
O_{DC}	Output Clock Duty Cycle	LVDS.		45	—	55	%
		LVPECL.		45	—	55	
		LVCMOS.	$F_{OUT} \leq$ 62.5MHz.	45	—	55	
			$F_{OUT} \geq$ 62.5MHz.	40	—	60	
T_{OE}	Output Enable/ Disable Time	—		—	—	100	ns
J_{PER}	Period Jitter, RMS	LVDS.		—	3	—	ps
		LVPECL.		—	5.8	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	5	—	
R_J	Random Jitter	LVDS.		—	1.3	—	ps
		LVPECL.		—	1.29	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	0.6	—	
D_J	Deterministic Jitter	LVDS.		—	5.8	—	ps
		LVPECL.		—	9.3	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	10	—	

Table 8. 3.3V AC Electrical Characteristics (Cont.)

V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
T_J	Total Jitter	LVDS.		—	23.6	—	ps
		LVPECL.		—	27.7	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	19	—	
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.		—	890	—	fs
		LVPECL.		—	860	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	750	—	

Table 9. 2.5V AC Electrical Characteristics

V_{DD} = 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.75	—	1000	MHz
		LVPECL.		0.75	—	1000	
		LVCMOS.		0.75	—	180	
	Frequency Stability	Temperature = -40°C to +85°C.		±25	—	±100	ppm
		Temperature = -40°C to +105°C.		±50	—	±100	ppm
	Aging (1st year)	T_A = 25°C.		—	—	±3	ppm
	Aging (10 years)	T_A = 25°C.		—	—	±10	ppm
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	V_{DD} - 2.0V.	—	50	—	
		LVCMOS.	To GND.	—	15	—	pF
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	—	10	ms
t_R	Output Rise Time	LVDS.	20% to 80% Vpp.	—	—	400	ps
		LVPECL.		—	—	400	
		LVCMOS.	10% to 90% V_{DD}.	—	—	3.5	ns
t_F	Output Fall Time	LVDS.	80% to 20% Vpp.	—	—	400	ps
		LVPECL.		—	—	400	
		LVCMOS.	90% to 10% V_{DD}.	—	—	3	ns
O_{DC}	Output Clock Duty Cycle	LVDS.		45	—	55	%
		LVPECL.		45	—	55	
		LVCMOS.		45	—	55	
T_{OE}	Output Enable/ Disable Time	—		—	—	100	ns

Table 9. 2.5V AC Electrical Characteristics (Cont.)

V_{DD} = 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

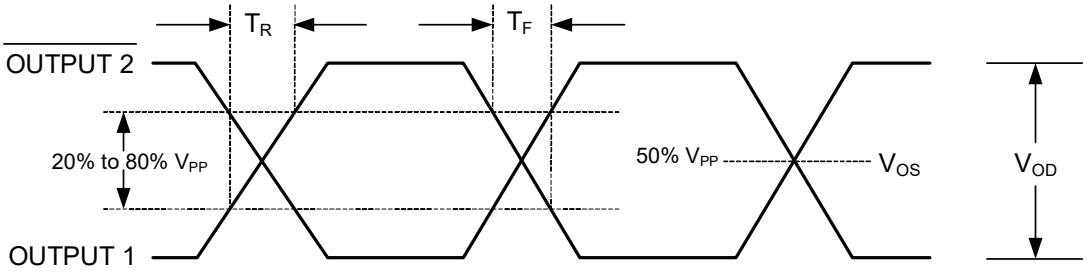
Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
J_{PER}	Period Jitter, RMS	LVDS.		—	4	—	ps
		LVPECL.		—	5.12	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	3.3	—	
R_J	Random Jitter	LVDS.		—	1.4	—	ps
		LVPECL.		—	1.36	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	1.3	—	
D_J	Deterministic Jitter	LVDS.		—	9.2	—	ps
		LVPECL.		—	10	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	6.7	—	
T_J	Total Jitter	LVDS.		—	29.2	—	ps
		LVPECL.		—	29.3	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	25.6	—	
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.		—	1040	—	fs
		LVPECL.		—	1200	—	
		LVCMOS.	F_{OUT} = 125MHz.	—	850	—	

Notes for all AC Electrical Characteristics tables:

[1] All jitter values provided at 156.25MHz, unless noted otherwise.

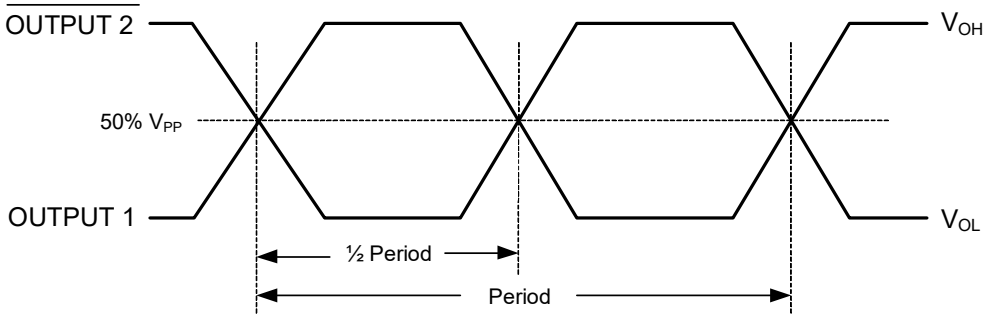
Output Waveforms – LVDS

Output Levels/Rise Time/Fall Time Measurements



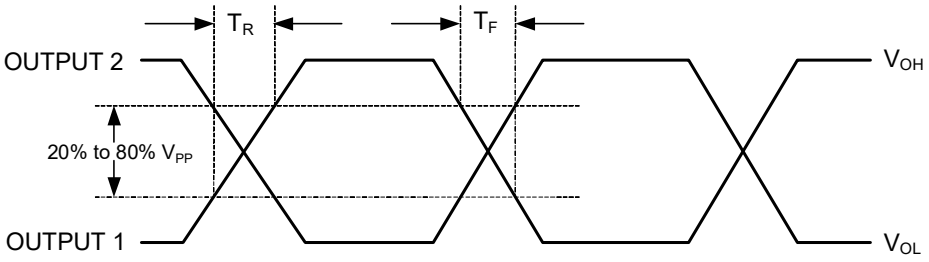
Oscillator Symmetry

Ideally, Symmetry should be 50/50 for ½ period –Other expressions are 45/55 or 55/45

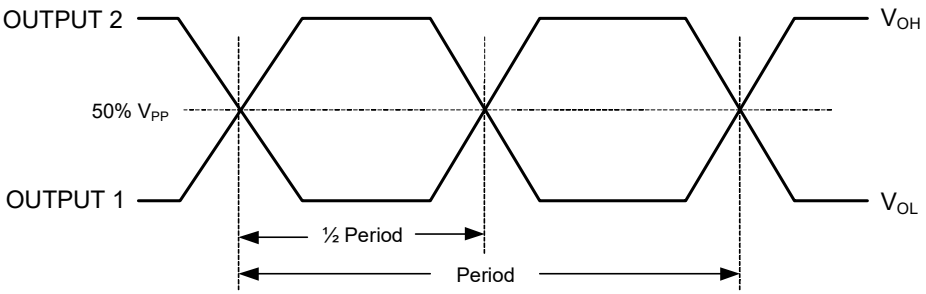


Output Waveforms – LVPECL

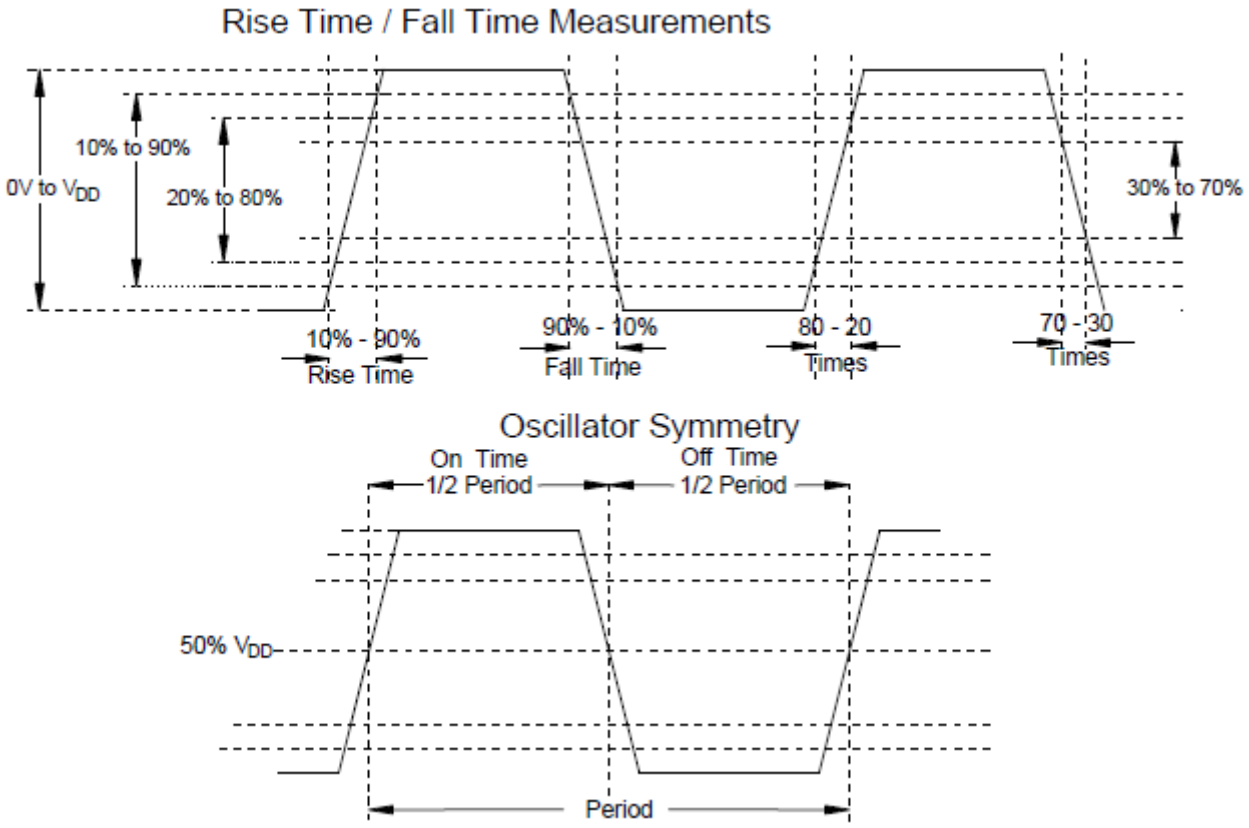
Rise Time/Fall Time Measurements



Oscillator Symmetry



Output Waveforms – LVCMOS

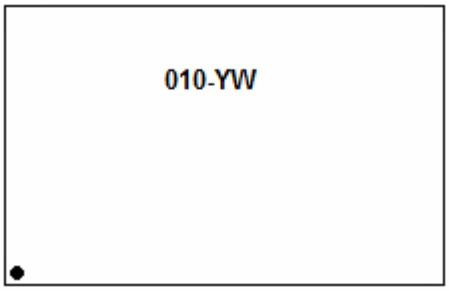


Package Outline Drawings

The package outline drawings (JS6, JX6) are appended at the end of this document. The package information is the most current data available.

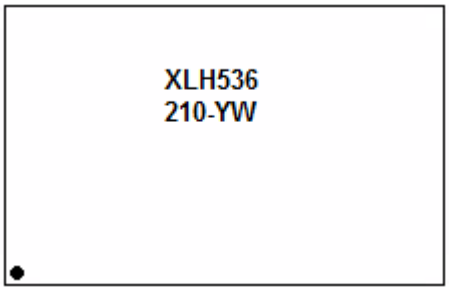
Marking Diagrams

JX6 3.2 × 2.5 mm Package Option (example based on XLH320010.000000I)



- Line 1:
  - "010" denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - "YW" denotes the last digit of the year and work week the part was assembled.

JS6 5.0 × 3.2 mm Package Option (example based on XLH536210.380000I)

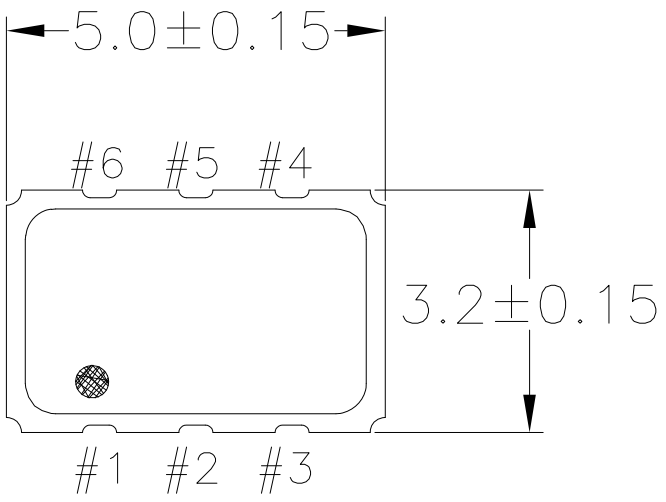


- Line 1:
  - "XL" = family; "H" = output type; "5" = package size; "3" = voltage; "6" = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
  - "210" denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - "YW" denotes the last digit of the year and work week the part was assembled.

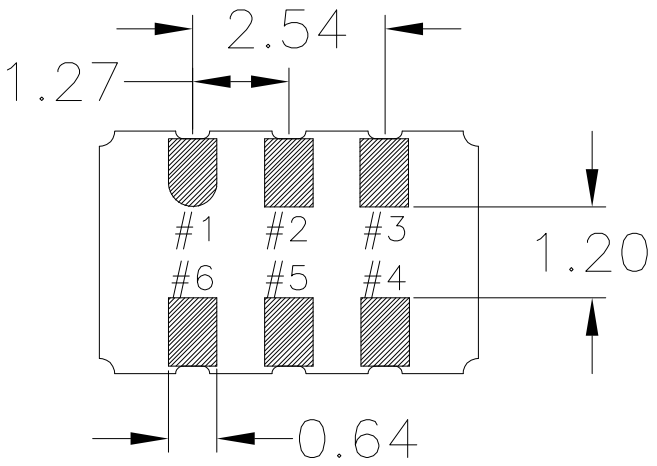
Revision History

Revision Date	Description of Change
August 18, 2021	Moved Ordering Information table to just after Pin Descriptions.
January 15, 2021	▪ Removed 4-pin package description table, figure, and package drawing references. ▪ Added footnote for pin 5 in Table 1. ▪ Updated "H:" description under "Output Type" in Ordering Information.
January 13, 2021	Added Marking Diagrams section and updated Package Outline Drawings links.
May 24, 2018	Updated LVCMOS Output Clock Duty Cycle, FOUT test condition.
April 27, 2018	Initial release.

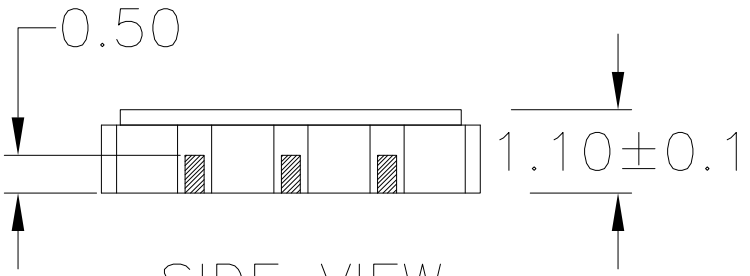
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



TOP VIEW



BOTTOM VIEW



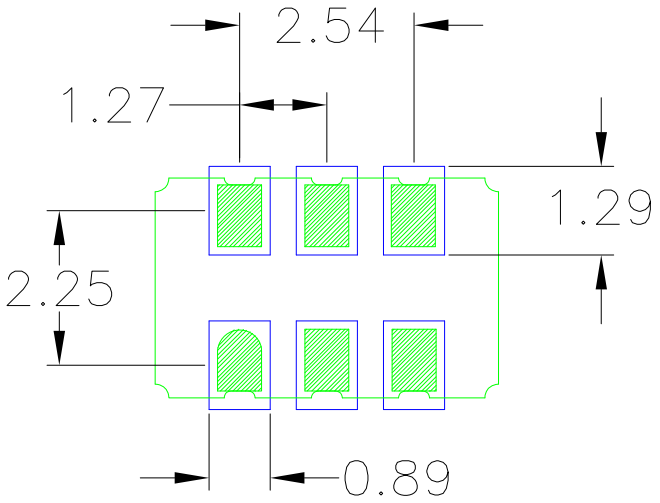
SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
DRAWN RAC	04/2/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4411 REV 03
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



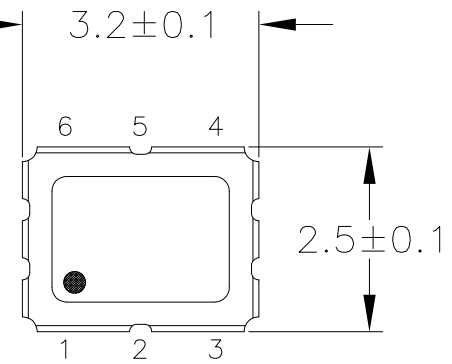
RECOMMENDED LAND PATTERN

NOTES:

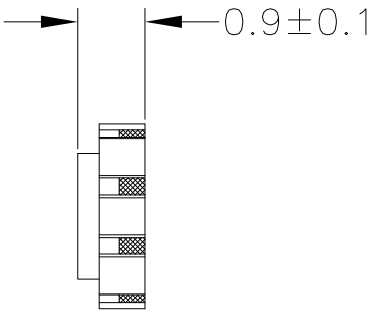
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
DRAWN PEAC	04/2/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4411 REV 03
		DO NOT SCALE DRAWING	SHEET 2 OF 2

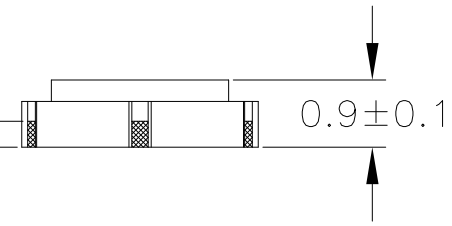
REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
00	INITIAL RELEASE	8/11/14	J.HUA
01	ADD PITCH	11/17/16	J.HUA
REFER TO DCP FOR OFFICIAL RELEASE DATE			



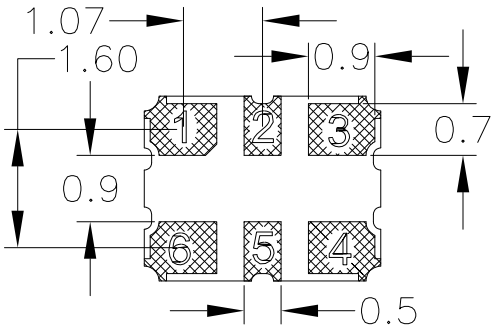
TOP VIEW



END VIEW



SIDE VIEW



BOTTOM VIEW

MM.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
	TITLE JX6 PACKAGE OUTLINE 3.2 x 2.5 mm BODY 0.9 mm Thick
	SIZE C · DRAWING No. PSC-4412 · REV 01
	DO NOT SCALE DRAWING · SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
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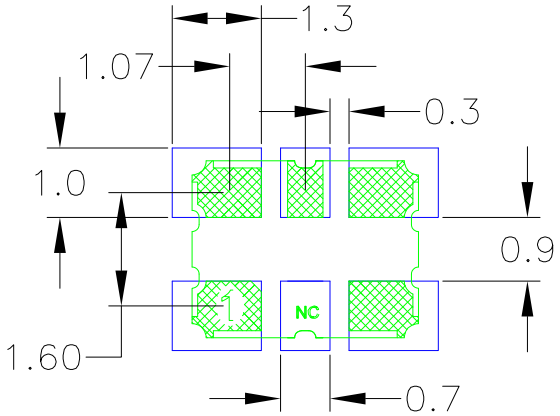
01	ADD PITCH	11/17/16	J.HUA
REFER TO DCP FOR OFFICIAL RELEASE DATE			



RECOMMENDED LAND PATTERN DIMENSION

S ARE IN MM. ANGLES IN DEGREES.
W. AS VIEWED ON PCB.
UTLINE SHOWS FOR REFERENCE IN GREEN.
IN BLUE. NSMD PATTERN ASSUMED.
RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT
MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
	TITLE	JX6 PACKAGE OUTLINE 3.2 x 2.5 mm BODY 0.9 mm Thick
	SIZE: C / DRAWING No.: PSC-4412	REV: 01
	DO NOT SCALE DRAWING	SHEET 2 OF 2

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