1.0 GENERAL DESCRIPTION

Each PATA NANDrive contains an integrated PATA NAND flash memory controller and discrete NAND flash die(s) in a LBGA package. Refer to Figure 2-1 for the PATA NANDrive block diagram.

1.1 Optimized PATA NANDrive

The heart of the PATA NANDrive is the PATA NAND flash memory controller, which translates standard PATA signals into flash media data and control signals. The following components contribute to the PATA NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU transfers the ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The PATA NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The PMU controls the power consumption of the PATA NANDrive. The PMU dramatically reduces the power consumption of the PATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the PATA NANDrive performance is an SRAM buffer. The buffer optimizes the Host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the PATA NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes to increase the longevity of flash media
3. Keeps track of data file structures

1.1.6 Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. During the design process, always provide access to the SCI port in the PCB design to aid in design validation.

1.1.8 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program and Erase operations to multiple flash media devices.

1.2 Advanced NAND Management

Advanced NAND management technology balances the wear on erased blocks with an advanced wear-leveling scheme. Advanced NAND management technology tracks the number of program/erase cycles within a group. When the Host updates data, higher priority is given to the less frequently written erase blocks; thereby, evenly distributing host writes within a wear-leveling group.

Advanced NAND management technology enhances the PATA NANDrive security with password protection and four independent protection zones, which can be set to Read-only or Hidden.

2.0 FUNCTION BLOCKS

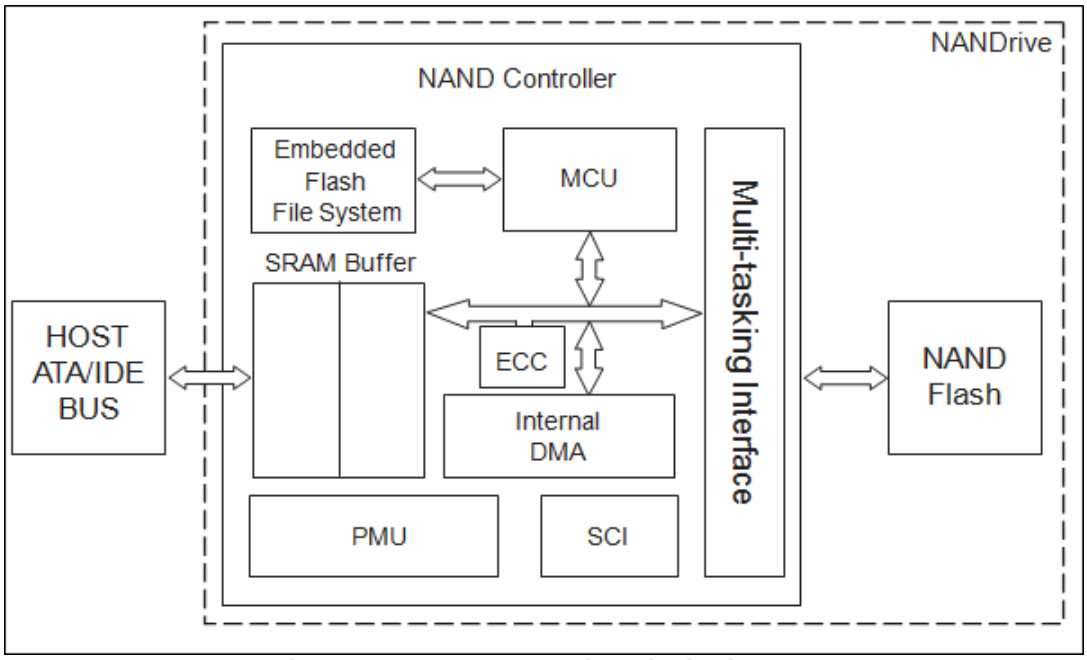


Figure 2-1: PATA NANDrive Block Diagram

3.0 PIN ASSIGNMENT

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output. Signals that the Host sources are designated as inputs, while signals that the PATA NANDrive sources are outputs.

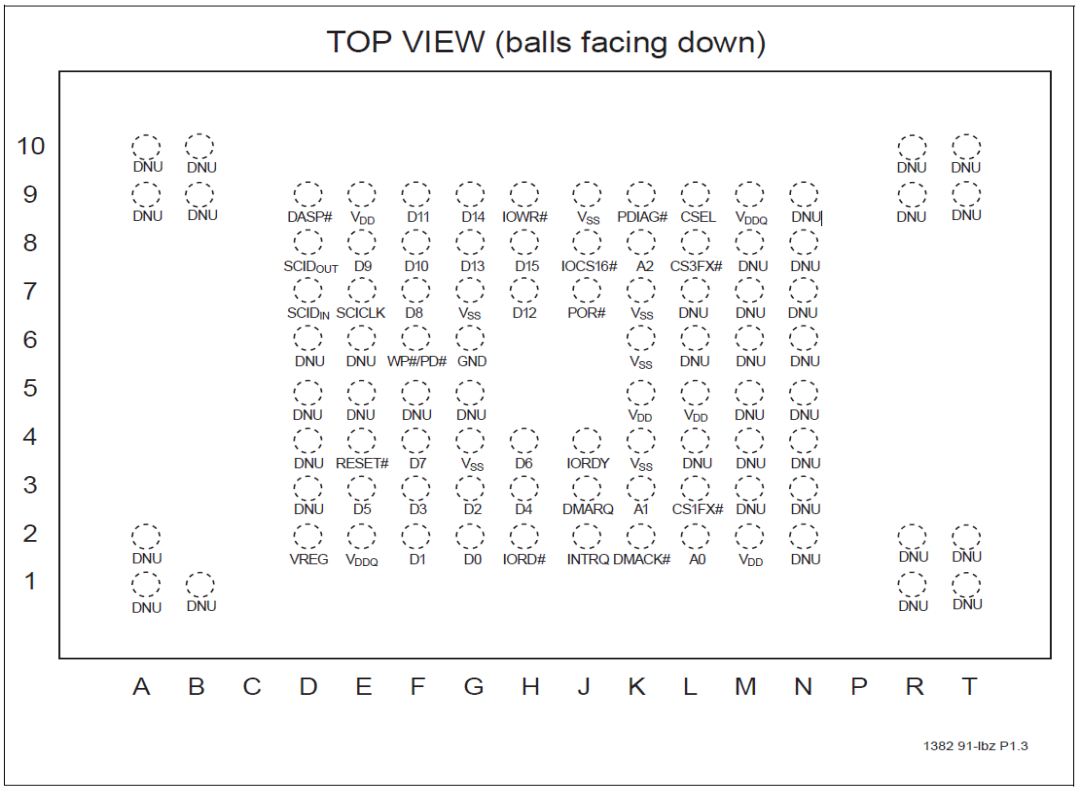


Figure 3-1: Pin Assignments for 91-Ball LBGA

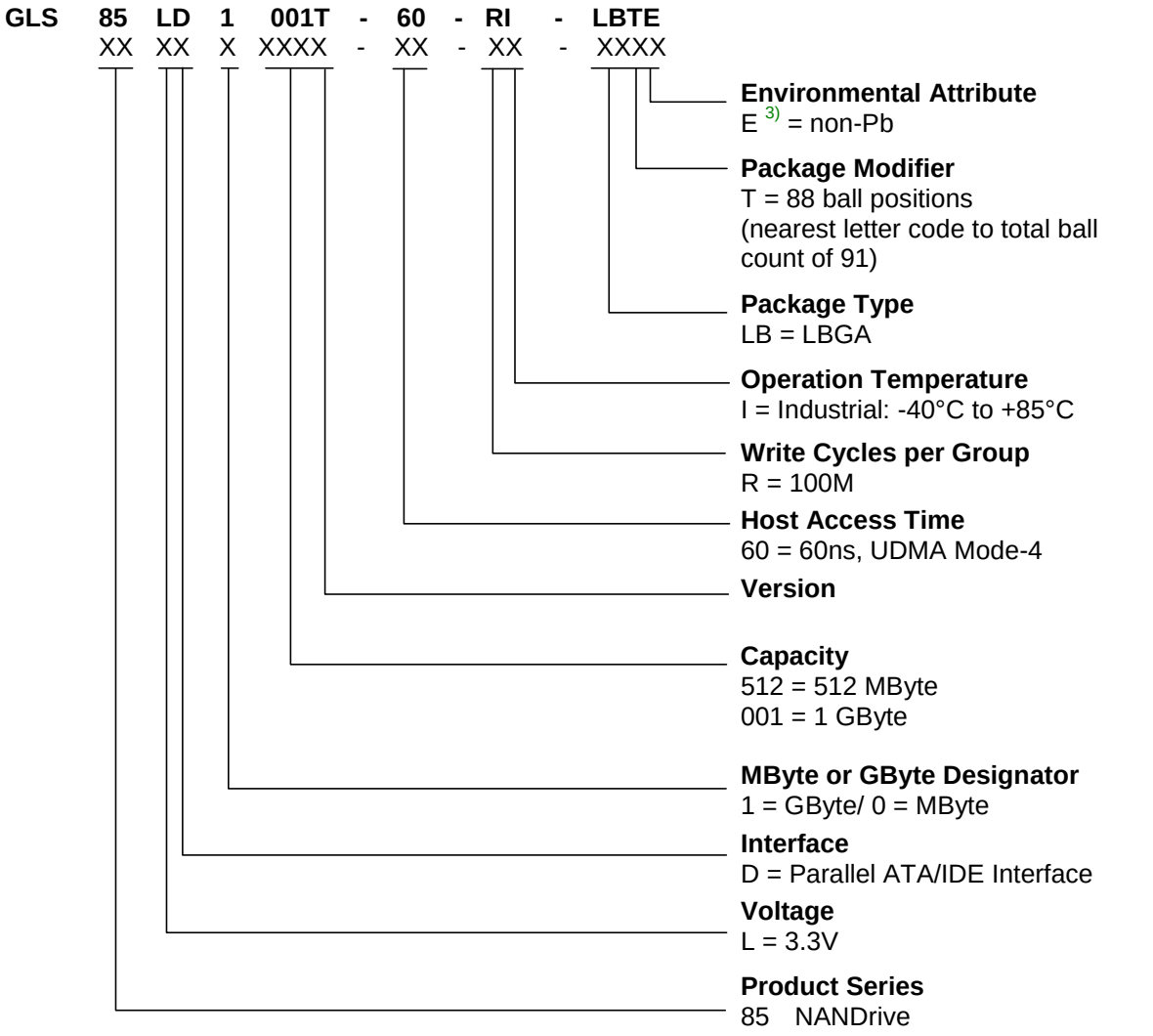
Table 3-1: Pin Assignments (1 of 2)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	K3			
A0	L2			
D15	H8	I/O	I1Z/O2	D[15:0] Data bus
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7			
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK#	K2	I	I2U	DMA Acknowledge - input from Host
DMARQ	J3	O	O1	DMA Request to Host
CS1FX#	L3	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	L8			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	IORD#: This is an I/O Read Strobe generated by the Host. When Ultra DMA mode is not active, this signal gates I/O data from the device. (This pin supports three functions)
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the Host to indicate that the Host is ready to receive Ultra DMA data-in bursts. The Host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the Host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The Host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	H9	I	I2Z	IOWR#: This is an I/O Write Strobe generated by the Host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device. (This pin supports two functions)
				STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst

Table 3-1: Pin Assignments (2 of 2)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
IORDY	J4	O	O1	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions) DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer. DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the Host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
IOCS16#	J8	O	O2	This output signal is asserted low when the device is indicating a Word data transfer cycle.
INTRQ	J2	O	O1	This signal is the active high Interrupt Request to the Host.
PDIAG#	K9	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the Host.
WP#/PD#	F6	I	I3U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
Serial Communication Interface (SCI)				
$SCID_{OUT}$	D8	O	O4	SCI data output. No external pull-up or pull-down resistor should connect to this signal.
$SCID_{IN}$	D7	I	I3U	SCI data input
SCICLK	E7	I	I3U	SCI clock
Miscellaneous				
V_{SS}	G4, G6, G7, K4, K6, K7, J9	PWR		Ground
V_{DD}	E9, K5, L5, M2	PWR		V_{DD} (3.3V)
V_{DDQ}	E2, M9	PWR		V_{DDQ} (5V/3.3V) for Host interface
POR#	J7	I	Analog Input	Power-on Reset (POR). Active low. Analog input for supply voltage detection
V_{REG}	D2	O		External capacitor pin
DNU	A1, A2, A9, A10, B1, B9, B10, D3, D4, D5, D6, E5, E6, F5, G5, L4, L6, L7, M3, M4, M5, M6, M7, M8, N2, N3, N4, N5, N6, N7, N8, N9, R1, R2, R9, R10, T1, T2, T9, T10			Do not use. All these pins should not be connected.

4.0 Product Ordering Information



3) Environmental suffix "E" denotes non-Pb solder. Greenliant non-Pb solder devices are "RoHS Compliant."

Valid Combinations [4]

PATA NANDrive Product

GLS85LD0512-60-RI-LBTE/ GLS85LD1001T-60-RI-LBTE

PATA NANDrive Evaluation Board (xxCN: xx-pin ATA Interface EVB, K: Kit)

GLS85LD0512-60-RI-40CN-K, GLS85LD1001T-60-RI-40CN-K,
GLS85LD0512-60-RI-44CN-K, GLS85LD1001T-60-RI-44CN-K

4) Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

4.1 Package Diagram

4.1.1 LBTE Package

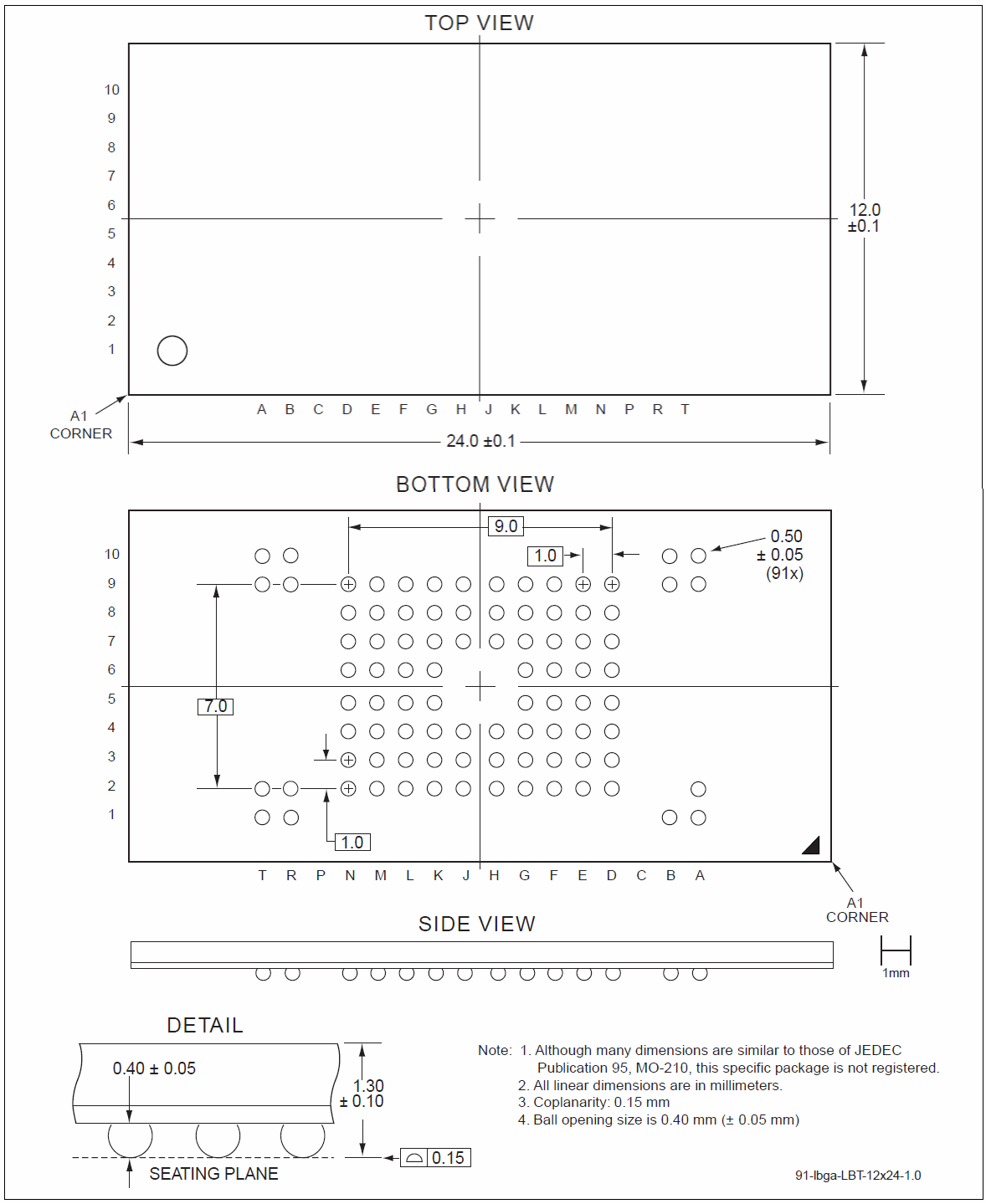


Figure 4-1: PATA NANDrive 91-Ball, Ball Grid Array (BGA) Greenliant Package Code: LBTE

4.2 Reference Documents

Table 4-1: Reference Documents

Title	Revision	Date
NANDrive SMART Specification	02.000	February 10, 2011
WindowsPT2 User Guide	02.000	March 1, 2011

4.3 Revision History

Table 4-2: Revision History

Number	Description	Date
01.000	- Initial release (based on GLS85LD1001T/LD0512 PATA NANDrive Data Sheet Rev06.001, 10/30/2012)	October 30, 2012

Mouser Electronics

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GLS85LD1001T-60-RI-44CN-K GLS85LD0512-60-RI-44CN-K GLS85LD0512-60-RI-LBTE-TM023 GLS85LD1001T-60-RI-LBTE GLS85LD0512-60-RI-LBTE (Rev. AD0) GLS85LD0512-60-RI-LBTE (Rev AC0) GLS85LD0512-60-RI-40CN-K GLS85LD1001T-60-RI-40CN-K GLS85LD0512-60-RI-LBTE