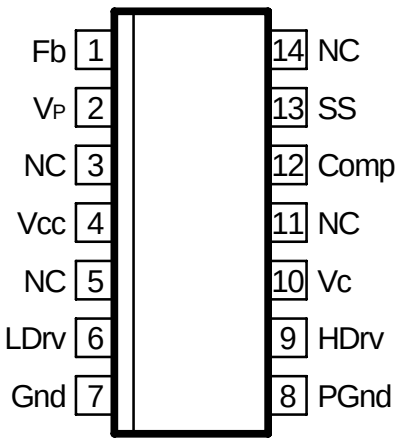
ABSOLUTE MAXIMUM RATINGS

Caution: *Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.*

(Voltages referenced to GND)

- Vcc Supply Voltage ..... -0.5V to 16V
- Vc Supply Voltage ..... -0.5V to 25V
- Storage Temperature Range ..... -65°C To 150°C
- Operating Junction Temperature Range ..... 0°C To 150°C
- ESD Classification ..... JEDEC, JESD22-A114
- Moisture Sensitivity Level ..... JEDEC Level 2 @ 260ºC

Package Information



14-Pin SOIC NB (S)

Θ_{JA} = 88º C/W

Block Diagram

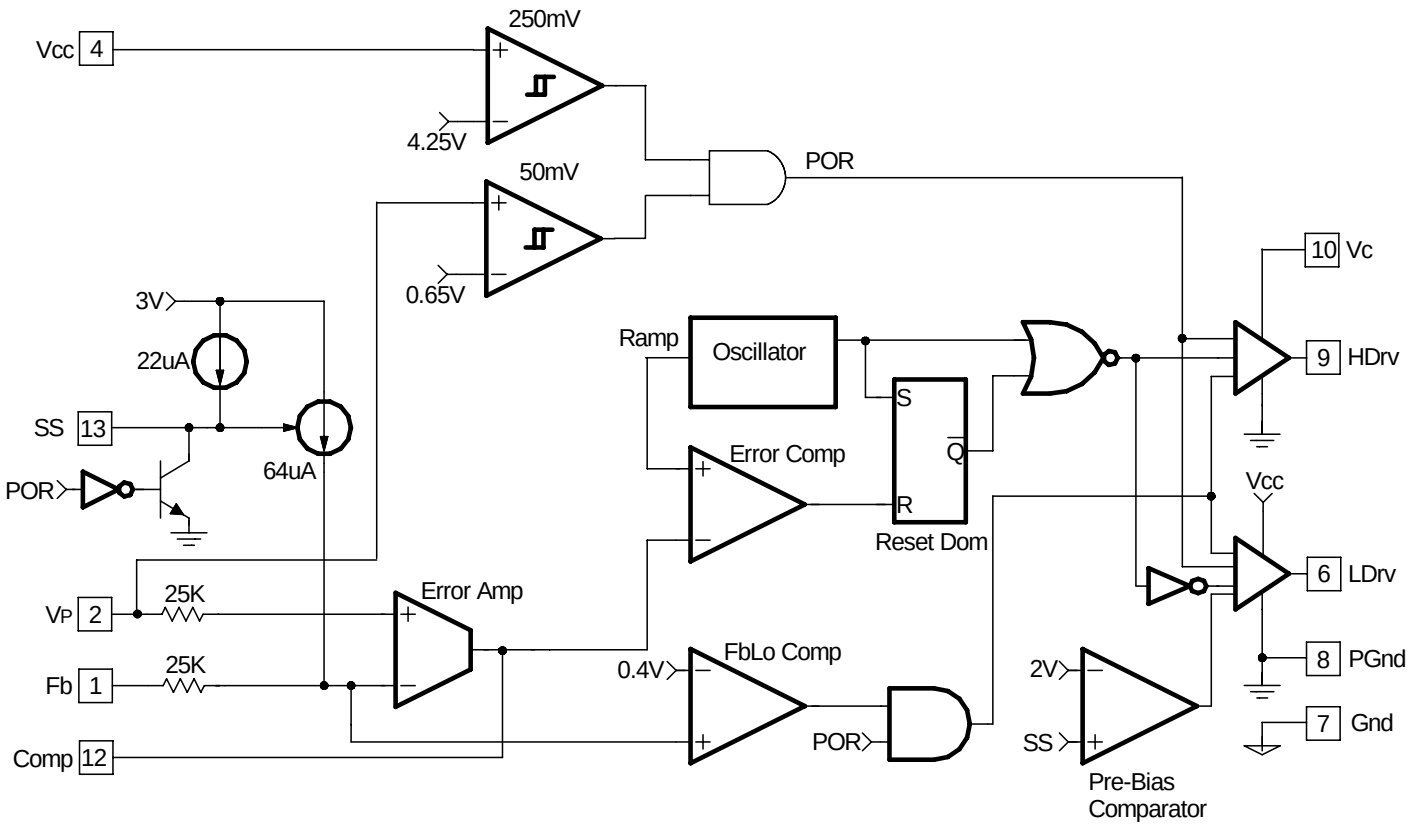


Fig. 2: Simplified block diagram of the IR3638

Pin Description

Pin	Name	Description
1	Fb	Inverting input to the error amplifier. This pin is connected to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	Vp / Enable	Dual function pin. Non inverting input to the error amplifier. Enable input.
3	NC	No Connect
4	Vcc	This pin provides power for the internal blocks of the IC as well as powers the low side driver. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to power ground.
5	NC	No Connect
6	LDrv	Output driver for low side MOSFET.
7	Gnd	IC ground for internal control circuitry.
8	PGnd	Power Ground. This pin serves as a separate ground for the MOSFET drivers and should be connected to the system's power ground plane.
9	HDrv	Output driver for high side MOSFET. The negative voltage at this pin may cause instability for the gate drive circuit. To prevent this, a low forward voltage drop diode (e.g. BAT54 or 1N4148) is required between this pin and Power Ground.
10	Vc	This pin powers the high side driver.
11	NC	No Connect
12	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
13	SS	Soft start. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to ground to set the start up time of the output voltage.
14	NC	No Connect

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{cc}	Supply Voltage	5	13.2	V
V_c	Supply Voltage	Converter Voltage + 5V	20	V
T_j	Junction Temperature	0	125	^oC

Electrical Specifications

Unless otherwise specified, these specification apply over V_{cc}=Vc=12V, 0ºC<T_j< 125ºC

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Supply Current						
V_{CC} Supply Current (Static)	$I_{CC(Static)}$	Enable=0V, No Switching		6.5	10	mA
V_{CC} Supply Current (Dynamic)	$I_{CC(Dynamic)}$	F_s=400kHz, C_{LOAD}=1.5nF		15	25	mA
V_C Supply Current (Static)	$I_{C(Static)}$	Enable=0V, No Switching		3.3	10	mA
V_C Supply Current (Dynamic)	$I_{C(Dynamic)}$	F_s=400kHz, C_{LOAD}=1.5nF		13	20	mA
Under Voltage Lockout						
Vcc-Start-Threshold	Vcc UVLO(R)	Supply ramping up	4.0	4.25	4.5	V
Vcc-Stop-Threshold	Vcc UVLO(F)	Supply ramping down	3.8	4.0	4.2	
Vcc-Hysteresis	Vcc(Hyst)	Supply ramping up and down	0.2	0.25	0.35	V
Enable-Start-Threshold	En UVLO (R)	Supply ramping up	0.6	0.65	0.7	V
Enable-Stop-Threshold	En UVLO (F)	Supply ramping down	0.56	0.6	0.66	
Enable-Hysteresis	En(Hyst)	Supply ramping up and down	25	42.5	60	mV
Fb_UVLO	Fb_UVLO	Fb ramping down	0.3	0.4	0.5	V
Oscillator						
Frequency	F_S		360	400	440	kHz
Ramp Amplitude	V_{ramp}	*Note1*		1.25		V
Min Duty Cycle	D_{min}	Fb=1V, Vp=0.8V			0	%
Max Duty Cycle	D_{max}	F_s=400kHz, Fb=0.6V, Vp=0.8V	81	85	95	%
Error Amplifier						
Fb Input Bias Current	I_{FB1}	SS=3V		-0.1	-0.5	µA
Fb Input Bias current	I_{FB2}	SS=0V		64		uA
Vp Input Bias Current	I_{vp}	SS=3V		-0.1	-0.5	uA
Transconductance	gm		440		1300	µmho
Input Offset Voltage	Vos	Vp=0.8V	-6	0	+6	mV
Vp Common Mode Range	Vcomn		0.6		1.5	V

Note1: Guaranteed by Design but not tested in production.

Electrical Specifications

Unless otherwise specified, these specification apply over V_{cc}=Vc=12V, 0°C<T_j< 125°C

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Soft Start						
Soft Start Current	I_{SS}	SS=0V	12	22	32	µA
Soft Start Turn On	SS (on)		1.8	2	2.2	V
Output Drivers						
LO, Drive Rise Time	Tr(Lo)	CL=1.5nF, See Fig 3		30	60	ns
HI Drive Rise Time	Tr(Hi)	CL=1.5nF, See Fig 3		30	60	ns
LO Drive Fall Time	Tf(Lo)	CL=1.5nF, See Fig 3		30	60	ns
HI Drive Fall Time	Tf(Hi)	CL=1.5nF, See Fig 3		30	60	ns
Dead Band Time	Tdead	See Fig 3	35	90	150	ns

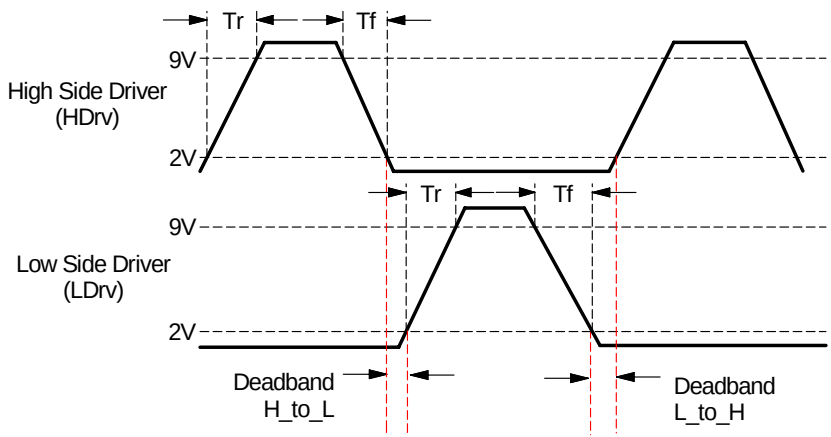


Fig. 3: Definition of Rise/Fall time and Deadband Time

Circuit Description

THEORY OF OPEARTION

Introduction

The IR3638 is a voltage mode PWM synchronous controller and operates with a fixed 400kHz switching frequency, allowing the use of small external components. The output voltage is set by feedback pin (Fb) and the external reference voltage (Vp). These are two inputs to error amplifier. The error signal between these two inputs is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle (D) which drivers N-channel external MOSFETs.

The timing of the IC is controlled by an internal oscillator circuit that uses on-chip capacitor to set the switching frequency.

Under-Voltage Lockout

The under-voltage lockout circuit monitors the Vcc and Enable input and assures that the MOSFET driver outputs remain in the off state whenever the Vcc or Enable voltages drop below set thresholds.

Pre-Bias Startup

IR3638 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.
The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the soft start reaches about 2.0V. Figure 4 shows a typical Pre-Bias condition at start up.
Depends on system configuration, specific amount of output capacitors may be required to prevent discharging the output voltage**.**

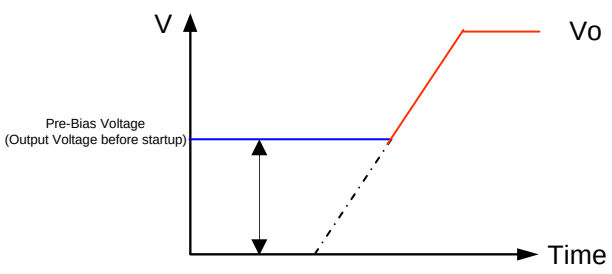


Fig. 4: Pre-Bias start up

Error Amplifier

The IR3638 is a voltage mode controller. The error amplifier is of transconductance type and it is capable of operating with Type III compensation control scheme using low ESR output capacitance.

Short Circuit Protection

The output is protected against the short-circuit. The IR3638 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The device shuts down the PWM signals and latches off when the output voltage drops below 0.4V.

Start Up / Down Considerations

The “Typical Application” on page1 shows a standard configuration where multiple input supplies are available.
This configuration minimizes the required extra components compared with a single input supply configuration. As it is shown the converter voltage (Bus Voltage) is set to 5V while the IC including the gate driver voltage are biased with 12V supply.
In order to maintain a proper start up, it is required that the Bus Voltage ramps up first followed by Vcc, Vc supply.
The system will be enabled when the Vp voltage passes the under voltage lock out threshold.

Figure 5 shows start up / down sequencing.

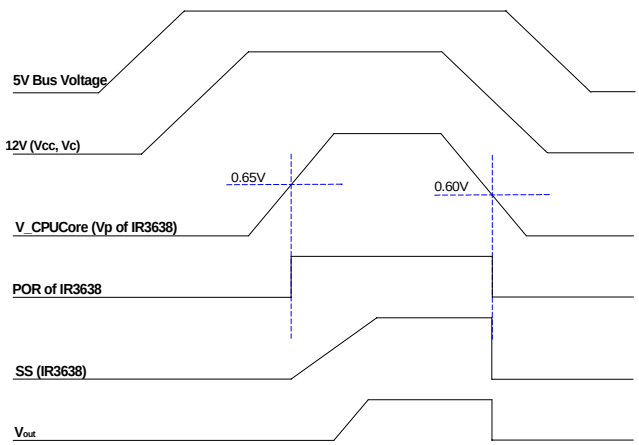


Fig. 5: Start Up / Down Sequence
(Refer to Figure1)

Soft-Start

The IR3638 has programmable soft-start to control the output voltage rise and limit the inrush current during start-up.

To ensure correct start-up, the soft-start sequence initiates when Vcc and Enable rise above their threshold and generate the Power On Ready (POR) signal. The soft-start function operates by sourcing current to charge an external capacitor to about 3V.

Initially, the soft-start function clamps the output of error amplifier by injecting a current (64uA) into the Fb pin and generates a voltage about 1.6V (64ux25K) across the negative input of error amplifier (see figure 6).

The magnitude of the injected current is inversely proportional to the voltage at the soft-start pin. As the soft-start voltage ramps up, the injected current decreases linearly and so does the voltage at negative input of error amplifier.

When the soft-start capacitor is around 1V, the voltage at the negative input of the error amplifier is approximately 0.8V (32uAx25K).

As soon as the Fb reaches the Vp voltage, the output of error amplifier will start increasing and generating the first PWM signal. As the soft-start capacitor voltage continues to ramp up, the current flowing into the Fb pin will keep decreasing.

The feedback voltage increases linearly as the soft start voltage ramps up. When soft-start voltage is around 2V the output voltage is reached the steady state and the injected current is zero.

Figure 7 shows the theoretical operational waveforms during soft-start.

The output voltage start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V.

The start-up time will be dependent on the size of the external soft-start capacitor and can be estimate by:

$$22\mu A * \frac{T_{start}}{C_{ss}} = 2V - 1V$$

For a given start-up time, the soft-start capacitor (nF) can be estimated as:

$$C_{ss} \cong 22\mu A * T_{start}(ms) \quad \text{--(1)}$$

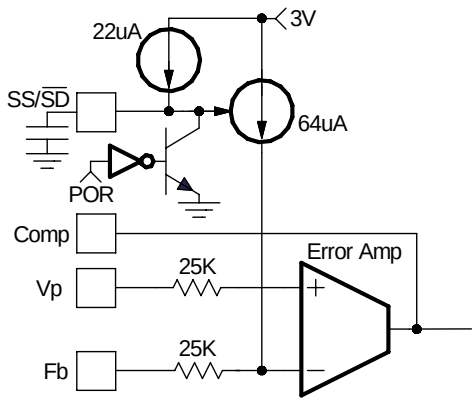


Fig. 6: Soft-Start circuit for IR3638

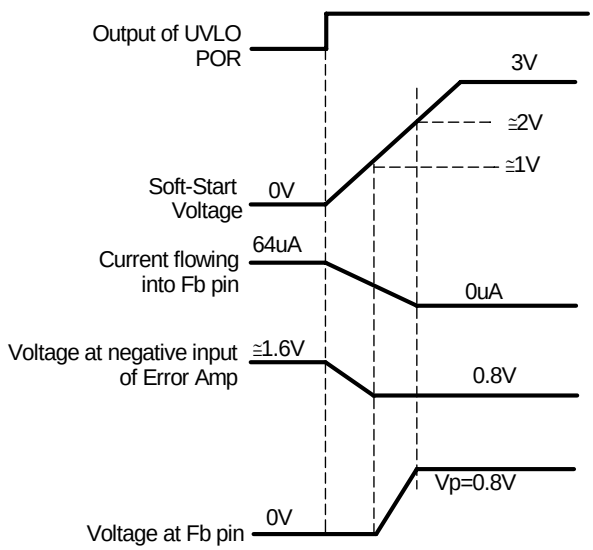


Fig. 7: Theoretical operation waveforms during soft-start

Application Information

Design Example:

The following is a design of typical application for IR3638. The application circuit is shown on page 14.

$V_{in} = 5V$
$V_{cc} = V_c = 12V$
$V_p = 1V$
$V_o = 1.2V$
$I_o = 6A$
$\Delta V_o \leq 30mV$

Output Voltage Programming

Output voltage is programmed by Vp voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is externally referenced to Vp. The divider is set to provide a voltage equal to Vp (in this case 1V) when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_p * \left(1 + \frac{R_1}{R_2}\right) \quad --(2)$$

When an external resistor divider is connected to the output as shown in figure 8.

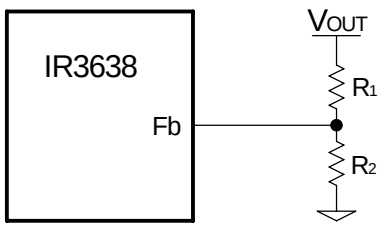


Fig. 8: Typical application of the IR3638 for programming the output voltage

Equation (2) can be rewritten as:

$$R_2 = R_1 * \left(\frac{V_p}{V_O - V_p}\right) \quad --(3)$$

Select R1 =1kOhm, this will result in R2=5kOhm.

Select the closest Standard value of 4.99kOhm.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 22\mu A * T_{start} \quad --(1)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 5ms, the soft-start capacitor will be 0.1uF. Choose a ceramic capacitor at 0.1uF.

Input Capacitor Selection

The input filter capacitor should be selected based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad --(4)$$

Where: $D = \frac{V_o}{V_{in}}$

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For Io=6A and D=0.24, the I_{RMS}=2.6A.

Ceramic capacitors are recommended due to their peak current capabilities, they also feature low ESR and ESL at higher frequency which enhance better efficiency,

Use two 10uF, 16V ceramic capacitor from Panasonic.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

Inductor Selection (Cont..)

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\ \ \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{--(5)}$$

V_{in} = *Maximum input voltage*

V_o = *Output Voltage*

Δi = *Inductor ripple current*

F_s = *Switching frequency*

Δt = *Turn on time*

D = *Duty cycle*

If $\Delta i \approx 40\%(I_o)$, then the output inductor will be:

L = 0.95uH

The coilcraft DO3316H-102ML (1uH, 10A, 6mOhm) is suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determines the output capacitors types and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components, these components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \quad \text{--(6)}$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = *Output voltage ripple*

ΔI_L = *Inductor ripple current*

It is recommended to select output capacitor with low enough ESR to meet output voltage ripple and step load transient requirements.

PosCap capacitors offer low ESR with large storage capacity per unit volume. These capacitors offer a cost effective output capacitor solution.

Sanyo 2R5TPF470M (2.5V, 470uF, 10mOhm) is selected for this design.

Equation (6) can be used to calculate the required ESR for the specific voltage ripple.

One Capacitor would meet the voltage ripple requirement.

Power MOSFET Selection

The IR3638 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{gs}), maximum output current, On-resistance $R_{DS(on)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{in}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{gs} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{cond} = (upper switch) = I_{load}^2 * R_{ds(on)} * D * \vartheta$$

$$P_{cond} = (lower switch) = I_{load}^2 * R_{ds(on)} * (1 - D) * \vartheta$$

$\vartheta = R_{ds(on)}$ *temperature dependency*

The $R_{DS(on)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF8910 is a good choice. The device provides two N-MOSFETs in a compact SO-8 package.

Power MOSFET Selection (Cont..)

The IRF8910 has the following data:

$$V_{ds} = 20V, I_d = 10A$$
$$R_{ds(on)} = 13.4m\Omega @ V_{gs} = 10V$$

The conduction losses will be: P_{con}=0.724W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turn-off delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{sw} = \frac{V_{ds(off)}}{2} * \frac{t_r + t_f}{T} * I_{load} \quad ---(7)$$

Where:
V ds(off) = Drain to source voltage at the off time
t_r = Rise time
t_f = Fall time
T = Switching period
Iload = Load current
The switching time waveforms is shown in figure9.

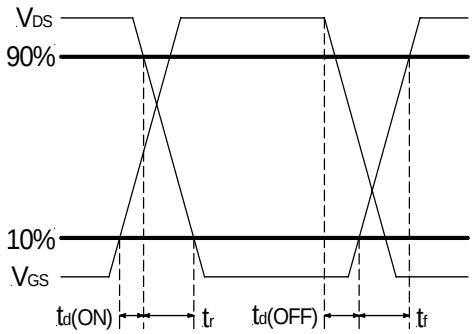


Fig. 9: switching time waveforms

From IRF8910 data sheet:

t_r = 10ns, t_f = 4.1ns

These values are taken under a certain condition test. For more details please refer to the IRF8910 data sheet.

By using equation (7), we can calculate the switching losses. P_{sw}=0.37W

Feedback Compensation

The IR3638 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 10). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2 * \pi \sqrt{L_o * C_o}} \quad ---(8)$$

Figure 10 shows gain and phase of the LC filter. Since we already have 180º phase shift just from the output filter, the system risks being unstable.

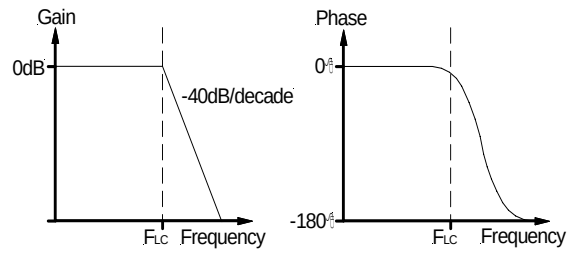


Fig. 10: Gain and Phase of LC filter

The IR3638's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or typeIII compensation. When it is used in typeII compensation the transconductance properties of the error amplifier become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in figure 11.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2 * \pi * ESR * C_o} \quad ---(9)$$

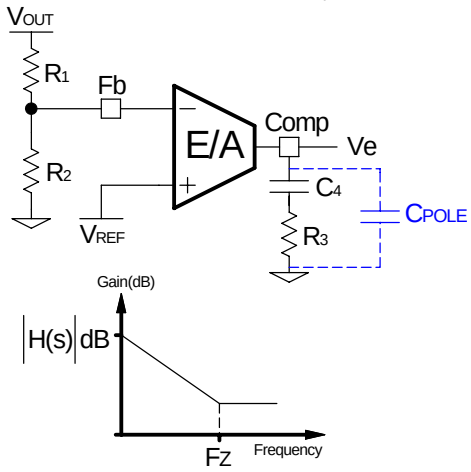


Fig. 11: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = \left(g_m * \frac{R_9}{R_9 + R_8} \right) * \frac{1 + sR_3C_4}{sC_4} \quad ---(10)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_9}{R_9 + R_8} \right) * R_3 \quad ---(11)$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad ---(12)$$

The gain is determined by the voltage divider and error amplifier's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * (R_1 + R_2)}{V_{in} * F_{LC}^2 * R_2 * g_m} \quad ---(13)$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_1 and R_2 = Feedback Resistor Dividers
g_m = Error Amplifier Transconductance

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad ---(14)$$

Using equations (15) and (16) to calculate C9.

One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s} \quad ---(15)$$

$$For\ F_P << \frac{F_s}{2}$$

Based on the frequency of the zero generated by output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
TypII(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
TypeIII(PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
TypeIII(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from IR Web-Site.

For this design we have:

V_{in}=5V
V_o=1.2V
V_{osc}=1.25V
V_p=1.0V
g_m=450umoh
L_o=1.0uH
C_o=1x470uF, ESR=10mOhm
F_s=400kHz

These result to:

F_{LC}=7.3kHz
F_{ESR}=33.8kHz
$F_{s/2}$=200kHz

Select crossover frequency:

Fo=40kHz

Since: $F_{LC}<F_{ESR}<F_o<F_{s/2}$, typeII compensation is selected to place the poles and zeros.

Using equations 12, 13 and 15 will result to the following compensation values:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * (R_1 + R_2)}{V_{in} * F_{LC}^2 * R_2 * g_m} \quad ---(13)$$

$$R_3 = 16.76K, \text{ Select } R_3 = 16.2K$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad ---(12)$$

$$C_4 = 1.78nF, \text{ Select } C_4 = 1.8nF$$

$$C_{POLE} \cong \frac{1}{\pi * R_3 * F_s} \quad ---(15)$$

$$C_{POLE} = 49pF, \text{ Select } C_{POLE} \le 22pF$$

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas.

The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vcc and Vc should be close to respective pins. It is important to place the feedback components include feedback resistors and compensation components close to Fb and Comp pins.

In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

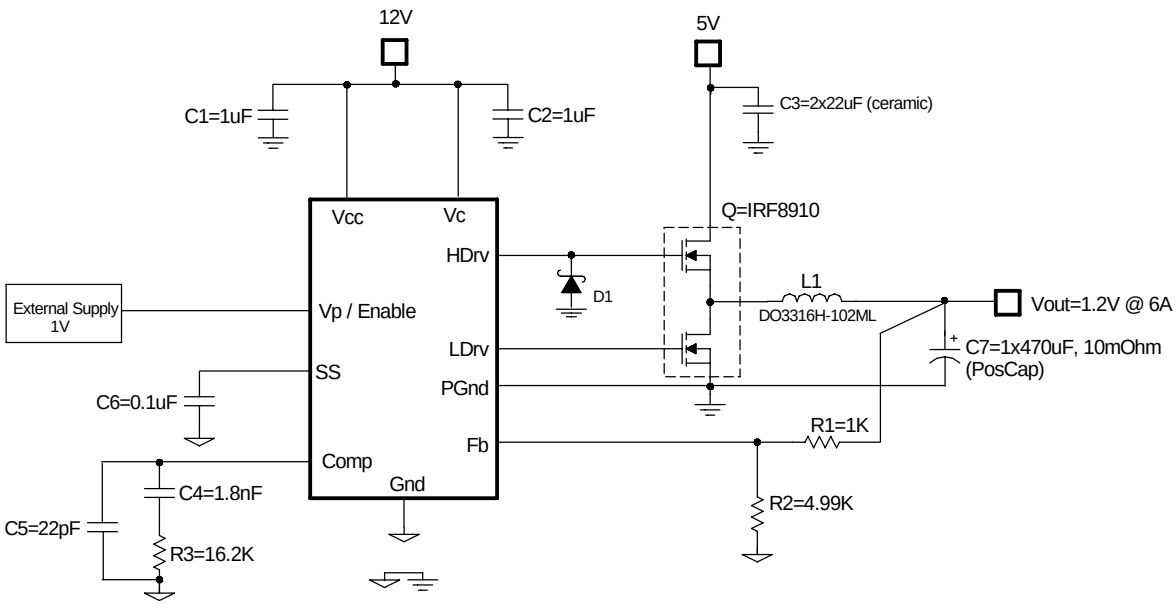
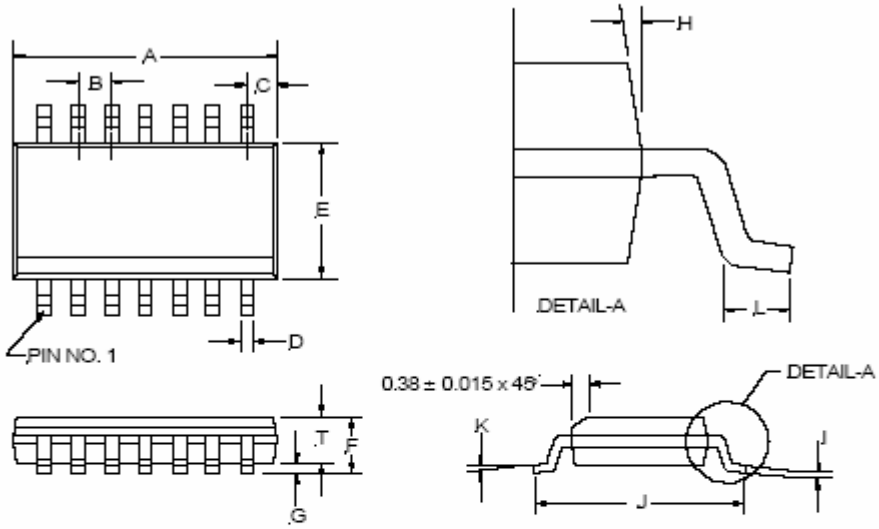


Fig.16: Application circuit for 5V to 1.2V @ 6A

(S) SOIC Package
14-Pin Surface Mount, Narrow Body



14-PIN		
SYMBOL	MIN	MAX
A	8.56	8.74
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

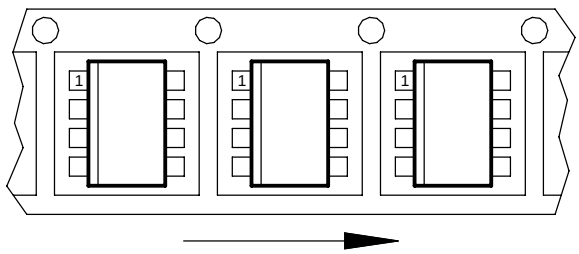


Figure A

International
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