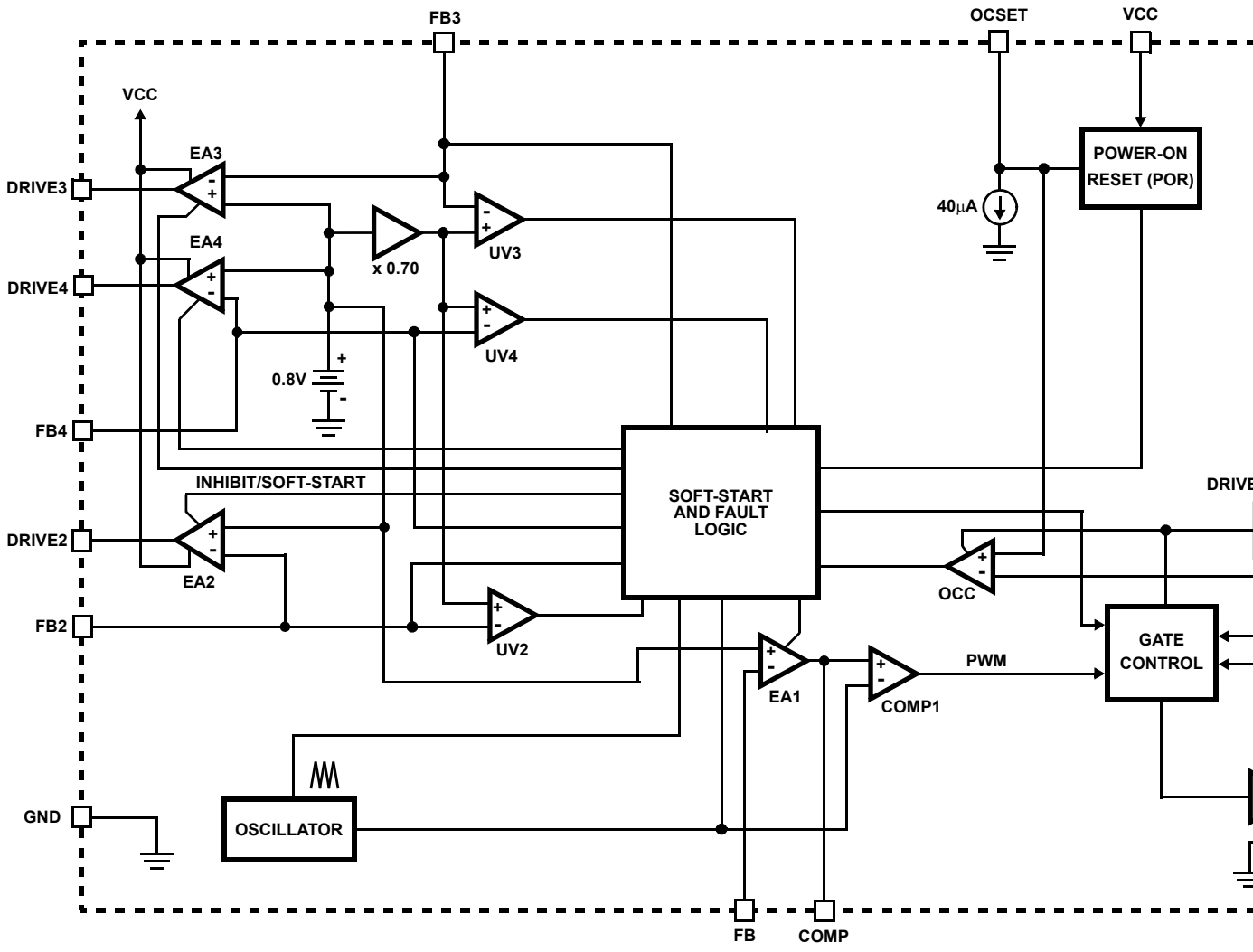
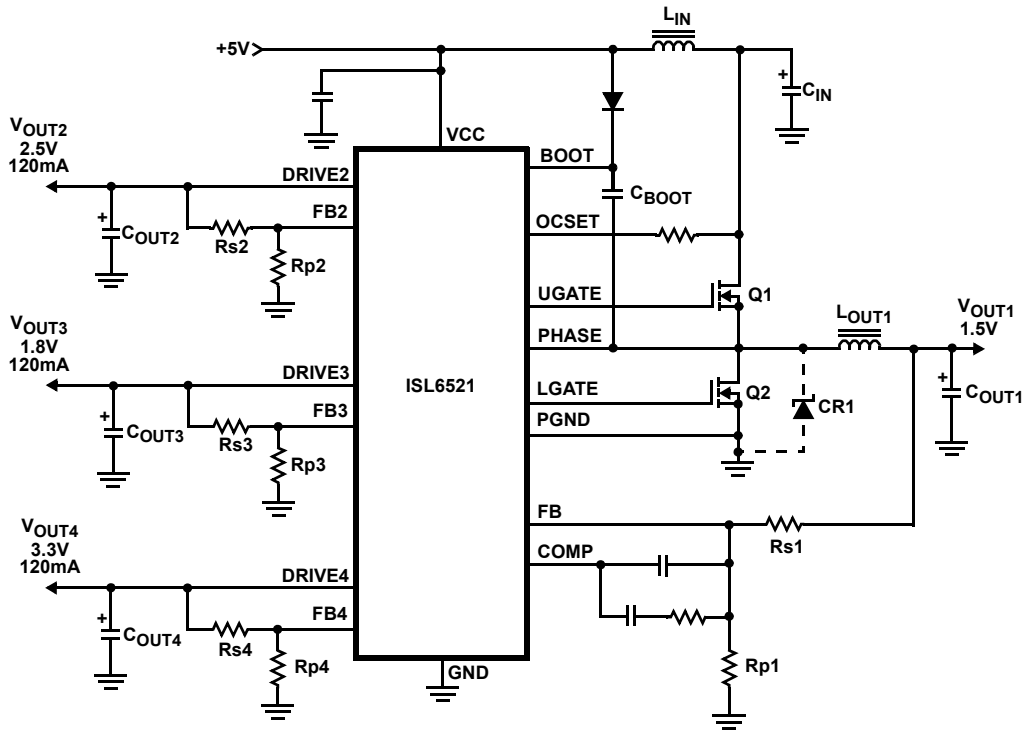
Block Diagram

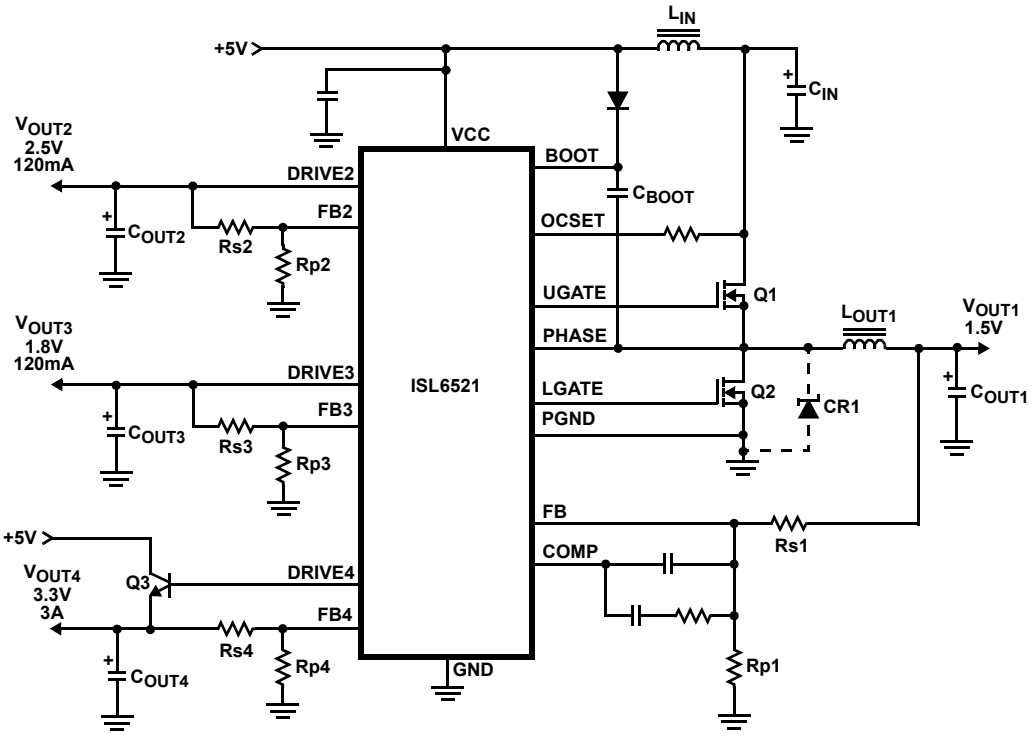


Typical Applications

High Output Current PWM Converter With Simple Triple Linears Regulators



High Output Current PWM Converter and Auxiliary 3.3V Linear Regulator



Absolute Maximum Ratings

UGATE, BOOT . . . . . GND - 0.3V to 15V
VCC, PHASE . . . . . GND - 0.3V to +7V
DRIVE, LGATE, all other pins . . . . . GND - 0.3V to VCC + 0.3V

Operating Conditions

Supply Voltage on VCC . . . . . +5V ±10%
Ambient Temperature Range
ISL6521CBZ . . . . . 0°C to 70°C
ISL6521IBZ . . . . . -40°C to 85°C
Junction Temperature Range. . . . . -40°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 74
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Operating Conditions: VCC = 5V, T_A = 0°C to 70°C, Unless Otherwise Noted. Typical specifications are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC}	UGATE, LGATE, and DRIVEx Open	-	5	-	mA
POWER-ON RESET						
Rising VCC Threshold			4.25	-	4.51	V
Falling VCC Threshold			3.74	-	4.0	V
OSCILLATOR AND SOFT-START						
Free Running Frequency	F_{OSC}	ISL6521CBZ	275	300	325	kHz
		ISL6521IBZ (-40°C to 85°C)	250	300	350	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V_{P-P}
Soft-Start Interval	T_{SS}		6.25	6.83	7.40	ms
REFERENCE VOLTAGE						
Reference Voltage (All Regulators)	V_{REF}		0.780	0.800	0.820	V
All Outputs Voltage Regulation		ISL6521CBZ	-2.0	-	+2.0	%
		ISL6521IBZ (-40°C to 85°C)	-2.5	-	+2.5	%
LINEAR REGULATORS (OUT2, OUT3, AND OUT4)						
Output Drive Current (All Linears)		VCC > 4.5V	100	120	-	mA
Undervoltage Level (V_{FB}/V_{REF})	V_{UV}		-	70	-	%
SYNCHRONOUS PWM CONTROLLER ERROR AMPLIFIER						
DC Gain			-	80	-	dB
Gain-Bandwidth Product	GBWP		15	-	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/µs
PWM CONTROLLER GATE DRIVERS						
UGATE Source	I_{UGATE}	VCC = 5V, V_{UGATE} = 2.5V	-	-1	-	A
UGATE Sink	I_{UGATE}	$V_{UGATE-PHASE}$ = 2.5V	-	1	-	A
LGATE Source	I_{LGATE}	VCC = 5V, V_{LGATE} = 2.5V	-	-1	-	A
LGATE Sink	I_{LGATE}	V_{LGATE} = 2.5V	-	2	-	A
PROTECTION						
OCSET Current Source	I_{OCSET}	ISL6521CBZ	34	40	46	µA
		ISL6521IBZ (-40°C to 85°C)	31.5	40	48	µA

Functional Pin Descriptions

VCC (Pin 11)

Provide a well decoupled 5V bias supply for the IC to this pin. This pin also provides the gate bias charge for the lower MOSFET controlled by the PWM section of the IC, as well as the drive current for the linear regulators. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

GND (Pin 5)

Signal ground for the controller. All voltage levels are measured with respect to this pin.

PGND (Pin 9)

This is the power ground connection. Tie the source of the lower MOSFET of the synchronous PWM converter to this pin.

BOOT (Pin 7)

Floating bootstrap supply pin for the upper gate drive. The bootstrap capacitor provides the necessary charge to turn and hold the upper MOSFET on. Connect a suitable capacitor (0.47µF recommended) from this pin to PHASE.

OCSET (Pin 12)

Connect a resistor from this pin to the drain of the upper PWM MOSFET. This resistor, an internal 40µA current source (typical), and the upper MOSFET's on-resistance set the converter overcurrent trip point. An overcurrent trip cycles the soft-start function.

The voltage at this pin is monitored for power-on reset (POR) purposes and pulling this pin below 1.25V with an open drain/collector device will shut down the switching controller.

PHASE (Pin 6)

Connect this pin to the source of the PWM converter upper MOSFET. This pin is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

UGATE (Pin 8)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

LGATE (Pin 10)

This pin provides the gate drive for the synchronous rectifier lower MOSFET. Connect LGATE to the gate of the lower MOSFET.

COMP and FB (Pins 4, 3)

COMP and FB are the available external pins of the PWM converter error amplifier. The FB pin is the inverting input of the error amplifier. Similarly, the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

DRIVE2, 3, 4 (Pins 1, 15, 13)

Connect these pins to the point of load or to the base terminals of external bipolar NPN transistors. These pins are each capable of providing 120mA of load current or drive current for the pass transistors.

FB2, 3, 4 (Pins 2, 16, 14)

Connect the output of the corresponding linear regulators to these pins through properly sized resistor dividers. The voltage at these pins is regulated to 0.8V. These pins are also monitored for undervoltage events.

Quickly pulling and holding any of these pins above 1.25V (using diode-coupled logic devices) shuts off the respective regulators. Releasing these pins from the pull-up voltage initiates a soft-start sequence on the respective regulator.

Description

Operation

The ISL6521 monitors and precisely controls one synchronous PWM converter and three configurable linear regulators from a +5V bias input. The PWM controller is designed to regulate the core voltage of an embedded processor or simple down conversion for high current applications. The PWM controller drives two MOSFETs (Q1 and Q2) in a synchronous-rectified buck converter configuration and regulates the output voltage to a level programmed by a resistor divider. The linear controllers are designed to regulate three additional system voltages. Typically, these include any I/O, memory, or clock voltages that might be required. All three linear controllers support up to 120mA of load current without external pass devices or higher currents with external NPN bipolar transistors.

Initialization

The ISL6521 automatically initializes upon receipt of input power. The Power-On Reset (POR) function continually monitors the input bias supply voltage. The POR monitors the bias voltage at the VCC pin. The POR function initiates soft-start operation after the bias supply voltage exceeds its POR threshold.

Soft-Start

The POR function initiates the soft-start sequence. The PWM error amplifier reference input is clamped to a level proportional to the soft-start voltage. As the soft-start voltage slews up, the PWM comparator generates PHASE pulses of increasing width that charge the output capacitor(s). Similarly, all linear regulators' reference inputs are clamped to a voltage proportional to the soft-start voltage. The ramp-up of the internal soft-start function provides a controlled output voltage rise.

Figure 1 shows the soft-start sequence for a typical application. At T0 the +5V bias voltage starts to ramp up crossing the 4.5V POR threshold at time T1. On the PWM section, the oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the internal soft-start voltage increases, the pulse-width on the PHASE pin increases to reach its steady-state duty cycle at time T2. Also at time T2, the error amplifier

references of the linear controllers, ramp to their final value bringing all outputs within regulation limits.

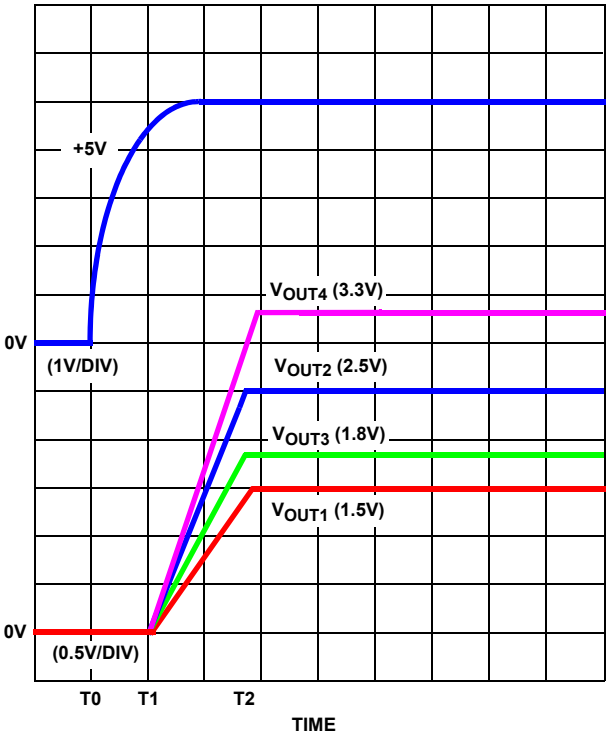


FIGURE 1. SOFT-START INTERVAL

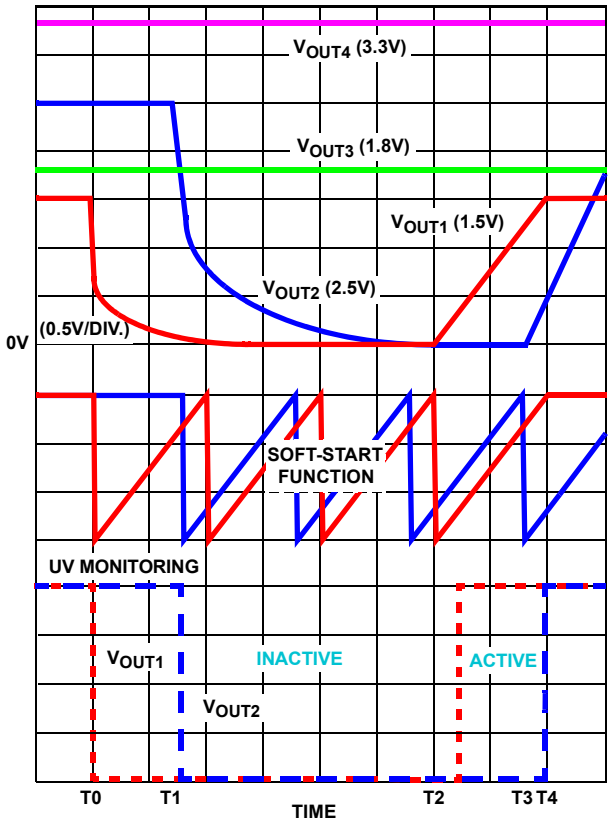


FIGURE 2. OVERCURRENT/UNDERVOLTAGE PROTECTION RESPONSE

Overcurrent Protection

All outputs are protected against excessive overcurrents. The PWM controller uses the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current for protection against a shorted output. All linear controllers monitor their respective FB pins for undervoltage events to protect against excessive currents.

A sustained overload (undervoltage on linears or overcurrent on the PWM) on any output results in an independent shutdown of the respective output, followed by subsequent individual re-start attempts performed at an interval equivalent to 3 soft-start intervals. Figure 2 describes the protection feature. At time T0, an overcurrent event sensed across the switching regulator's upper MOSFET ($r_{DS(ON)}$ sensing) triggers a shutdown of the V_{OUT1} output. As a result, its internal soft-start initiates a number of soft-start cycles. After a three-cycle wait, the fourth soft-start initiates a ramp-up attempt of the failed output, at time T2, bringing the output in regulation at time T4.

To exemplify a UV event on one of the linears, at time T1, the clock regulator (V_{OUT2}) is also subjected to an overcurrent event, resulting in a UV condition. Similarly, after three soft-start periods, the fourth cycle initiates a ramp-up of this linear output at time T3. One soft-start period after T3, the linear output is within regulation limits. UV glitches less than 1µs (typically) in duration are ignored.

Overcurrent protection is performed on the synchronous switching regulator on a cycle-by-cycle basis. OC monitoring is active as long as the regulator is operational. Since the overcurrent protection on the linear regulators is performed through undervoltage monitoring at the feedback pins (FB2, FB3, and FB4), this feature is activated approximately 25% into the soft-start interval (see Figure 2).

A resistor (R_{OCSET}) programs the overcurrent trip level for the PWM converter. As shown in Figure 3, the internal 40µA current sink (I_{OCSET}) develops a voltage across R_{OCSET} (V_{SET}) that is referenced to V_{IN}. The DRIVE signal enables the overcurrent comparator (OCC). When the voltage across the upper MOSFET ($V_{DS(ON)}$) exceeds V_{SET}, the overcurrent comparator trips to set the overcurrent latch. Both V_{SET} and $V_{DS(ON)}$ are referenced to V_{IN} and a small capacitor across R_{OCSET} helps V_{OCSET} track the variations of V_{IN} due to MOSFET switching. The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

The OC trip point varies with MOSFET's $r_{DS(ON)}$ temperature variations. To avoid overcurrent tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

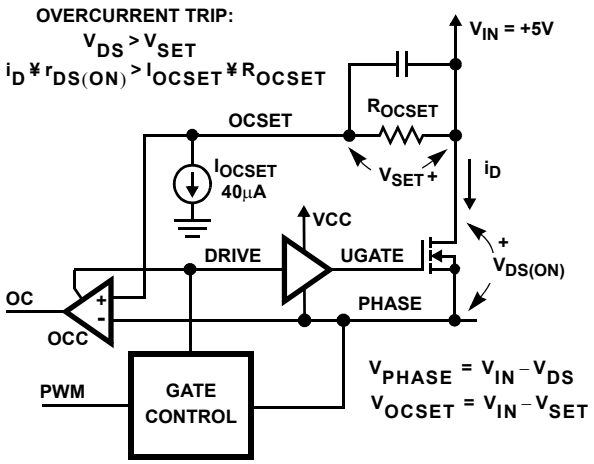


FIGURE 3. OVERCURRENT DETECTION

For an equation for the ripple current see the section under component guidelines titled ‘Output Inductor Selection’.

Output Voltage Selection

The output voltage of the PWM converter can be resistor-programmed to any level between V_{IN} and 0.8V. However, since the value of R_{S1} is affecting the values of the rest of the compensation components, it is advisable its value is kept between 2kΩ and 5kΩ.

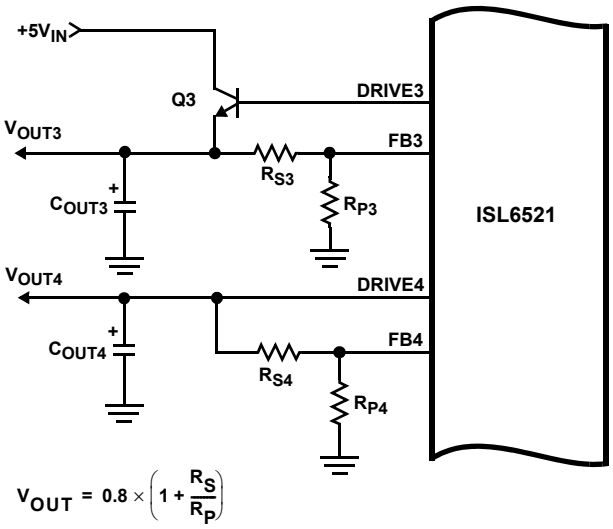


FIGURE 4. ADJUSTING THE OUTPUT VOLTAGE OF ANY OF THE FOUR REGULATORS (OUTPUTS 3 AND 4 PICTURED)

Output voltage selection on the linear regulators is set by means of external resistor dividers as shown in Figure 4. The two resistors used to set the voltage on each of the three linear regulators have to meet the following criteria: their value while in a parallel connection has to be less than 5kΩ, or otherwise said, the following relationship has to be met:

$$\frac{R_S \times R_P}{R_S + R_P} < 5k\Omega$$

To ensure the parallel combination of the feedback resistors equals a certain chosen value, R_{FB}, use the following equations:

$$R_S = \frac{V_{OUT}}{V_{FB}} \times R_{FB}$$

$$R_P = \frac{R_S \times V_{FB}}{V_{OUT} - V_{FB}}, \text{ where}$$

V_{OUT} - the desired output voltage,

V_{FB} - feedback (reference) voltage, 0.8V.

Application Guidelines

Soft-Start Interval

The soft-start function controls the output voltages rate of rise to limit the current surge at start-up. The soft-start function is integrated on the chip and the soft-start interval is fixed.

PWM Controller Feedback Compensation

The PWM controller uses voltage-mode control for output regulation. This section highlights the design consideration for a PWM voltage-mode controller. Apply the methods and considerations only to the PWM controller.

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level, 0.8V. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain, given by V_{IN}/V_{OSC}, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}.

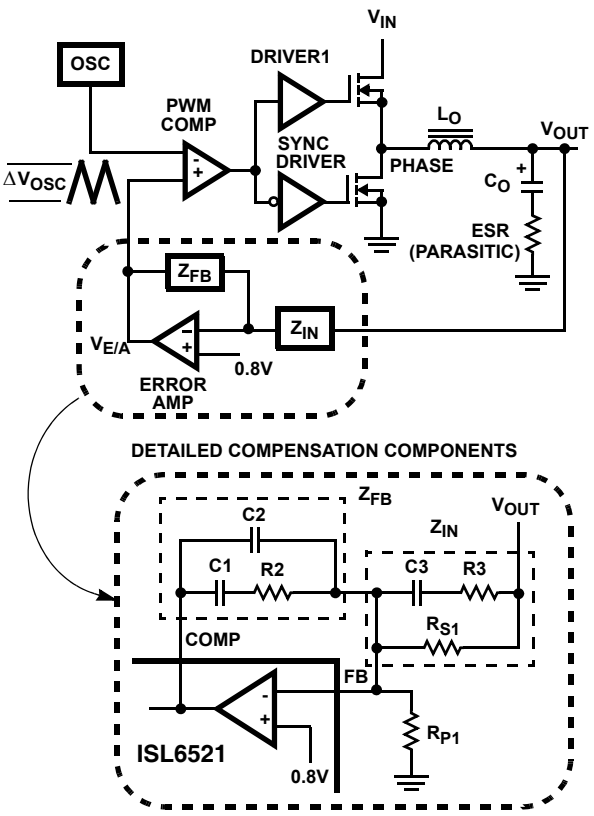


FIGURE 5. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the ISL6521) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 5. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_{S1} + R3) \times C3} \qquad F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

Figure 6 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown in Figure 5. Using the above guidelines should yield a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

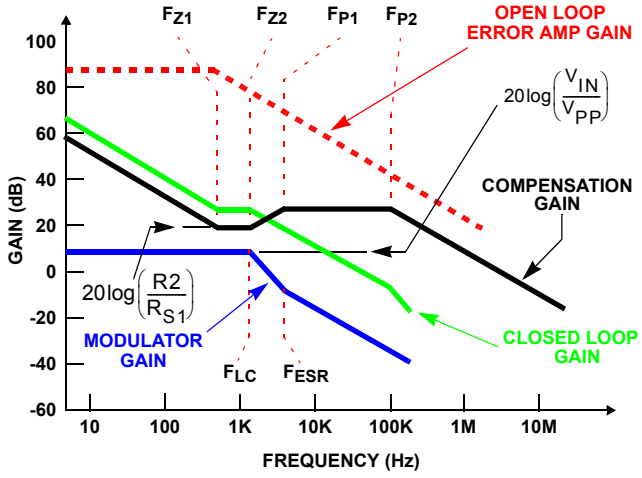


FIGURE 6. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Individual Output Disable

The PWM and linear controllers can independently be shutdown.

To disable the switching regulator, use an open-drain or open-collector device capable of pulling the OCSET pin (with the attached R_{OCSET} pull-up) below 1.25V. To minimize the possibility of OC trips at levels different than predicted, a C_{OCSET} capacitor with a value of an order of magnitude larger than the output capacitance of the pull-down device, has to be

used in parallel with R_{OCSET} (1nF recommended). Upon turn-off of the pull-down device, the switching regulator undergoes a soft-start cycle.

To disable a particular linear controller, pull and hold the respective FB pin above a typical threshold of 1.25V. One way to achieve this task is by using a logic gate coupled through a small-signal diode. The diode should be placed as close to the FB pin as possible to minimize stray capacitance to this pin. Upon turn-off of the pull-up device, the respective output undergoes a soft-start cycle, bringing the output within regulation limits. On regulators implementing this feature, the parallel combination of the feedback resistors has to be sufficiently high to allow ease of driving from the external device. Considering the other restriction applying to the upper range of this resistor combination (see 'Output Voltage Selection' paragraph), it is recommended the values of the feedback resistors on the linear regulator output meet the following constraint:

$$2k\Omega < \frac{R_S \times R_P}{R_S + R_P} < 5k\Omega$$

Important Note When Using External Pass Devices

If the collector voltage to a linear regulator pass transistor (Q3, Q4, or Q5 shown in Figure 7) is lost, the respective regulator has to be shut down by pulling high its FB pin. This measure is necessary in order to avoid possible damage to the ISL6521 as a result of overheating. Overheating can occur in such situations due to sheer power dissipation inside the chip's linear drivers.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of the upper PWM MOSFET. Prior to turn-off, the upper MOSFET was carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using an ISL6521 controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

The critical small signal components include the bypass capacitor for VCC and the feedback resistors. Locate these components close to their connecting pins on the control IC.

A multi-layer printed circuit board is recommended. Figure 7 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each can represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE nodes, but do not unnecessarily oversize these particular islands. Since the PHASE nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.

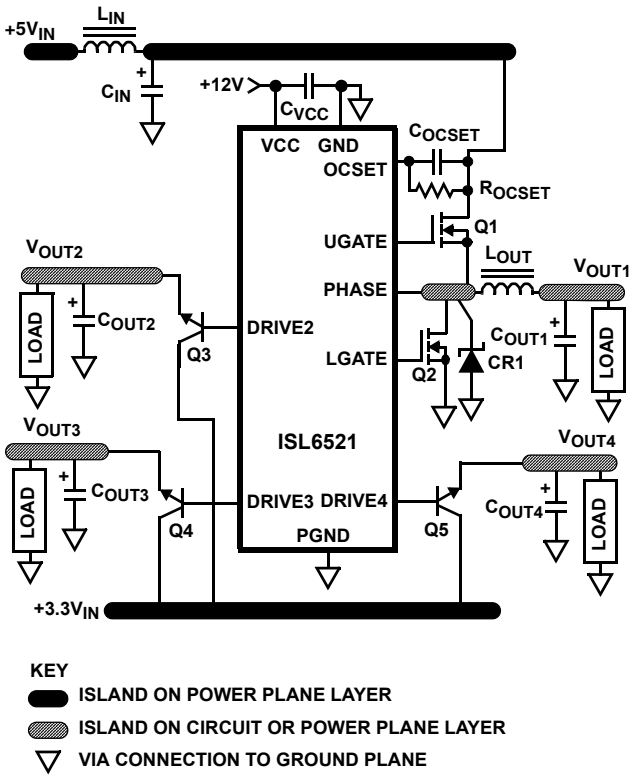


FIGURE 7. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Component Selection Guidelines

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic load regulation requirements. Additionally, the PWM converters require an output capacitor to filter the current ripple. The load transient for some embedded processors requires high quality capacitors to supply the high slew rate (di/dt) current demands.

PWM Output Capacitors

High performance embedded processors can produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Linear Output Capacitors

The output capacitors for the linear regulators provide dynamic load current. The linear controllers use dominant pole compensation integrated into the error amplifier and are insensitive to output capacitor selection. Output capacitors should be selected for transient load regulation.

PWM Output Inductor Selection

The PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter's response time to a load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values increase the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6521 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the post-transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 of the summation of the DC load current.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up.

Transistors Selection/Considerations

The ISL6521 can employ up to 5 external transistors. Two N-channel MOSFETs are used in the synchronous-rectified buck topology of PWM converter. The linear controllers can each drive an NPN bipolar transistor as a pass element. All these transistors should be selected based upon $r_{DS(ON)}$, current gain, saturation voltages, gate/base supply requirements, and thermal management considerations.

PWM MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty factor (see the equations below). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage.

The equations below assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6521 and don't heat the MOSFETs. However, large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

Given the reduced available gate bias voltage (5V) logic-level or sub-logic-level transistors have to be used for both N-MOSFETs. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics, as the low gate threshold could be conducive to some shoot-through (due to the Miller effect), in spite of the counteracting circuitry present aboard the ISL6521.

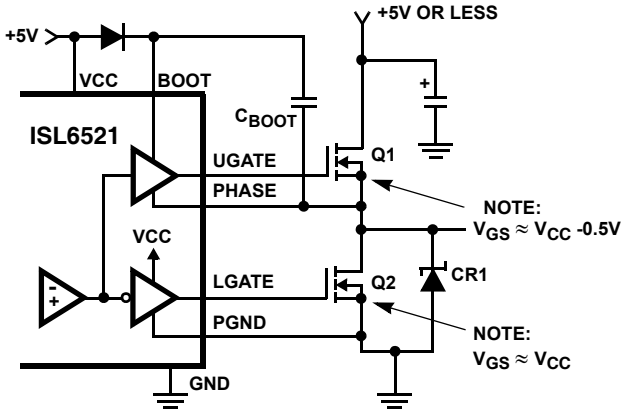


FIGURE 8. MOSFET GATE BIAS

Rectifier CR1 is a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, providing the body diode is fast enough to avoid excessive negative voltage swings at the PHASE pin. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

Linear Controller Transistor Selection

The main criteria for selection of transistors for the linear regulators is package selection for efficient removal of heat. The power dissipated in a linear regulator is:

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the rating with a the maximum expected ambient temperature.

If bipolar NPN transistors have to be used with the linear controllers, insure the current gain at the given operating V_{CE} is sufficiently large to provide the desired maximum output load current when the base is fed with the minimum driver output current.

ISL6521 DC-DC Converter Application Circuit

Figure 9 shows a power management application circuit for powering an embedded processor. The circuit provides the processor core voltage (V_{CORE}), the I/O voltage ($V_{I/O}$), the clock voltage (V_{CLOCK}), and memory voltage (V_{MEMORY}) from a single +5V supply. A component selection table provides the recommended component values at various load current steps.

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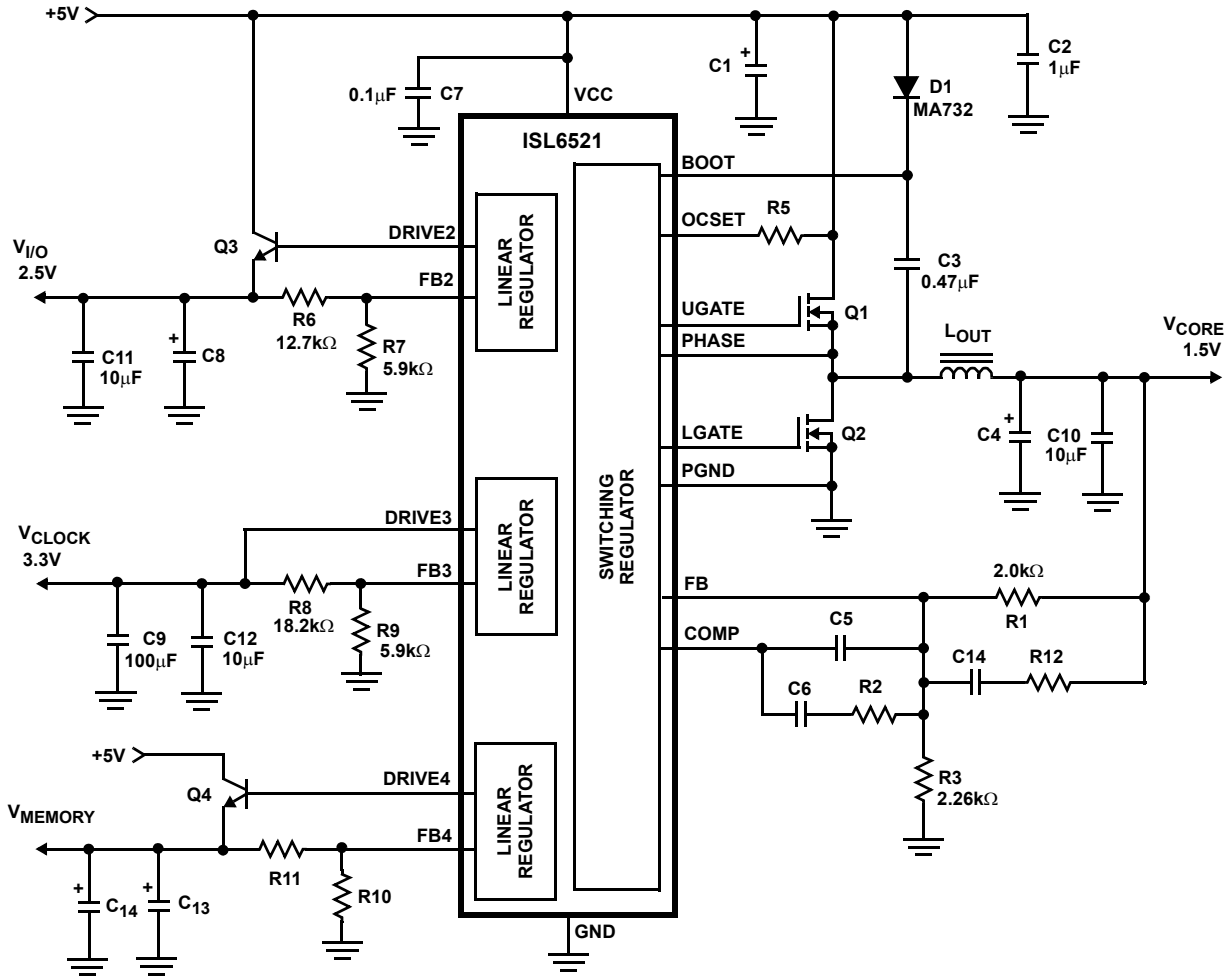
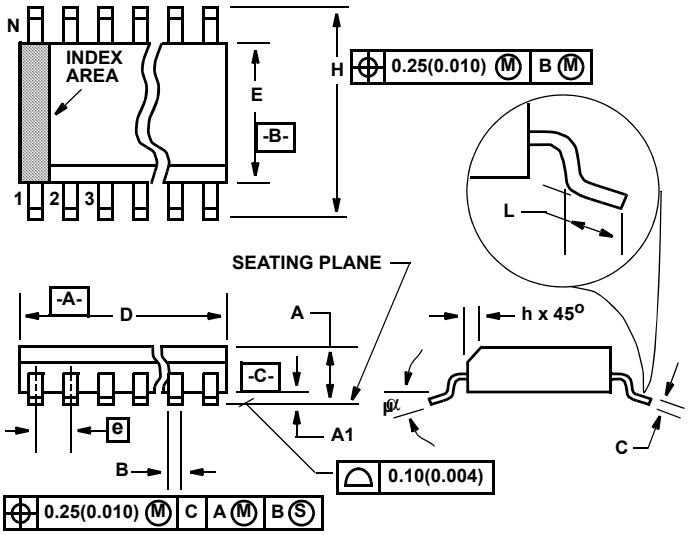


FIGURE 9. POWER SUPPLY APPLICATION CIRCUIT FOR AN EMBEDDED PROCESSOR

Component Selection Table

I_{CC_INT}	L_{OUT}	Q1	Q2	Q3	C1	C4
5A	7.5µH Pulse P1172.103	IRF7910	IRF7910	FZT649 (1A or less)	1 x 1000µF 10MBZ1000M 10x12.5	1 x 1200µF 6.3MBZ1200M 8x16
10A	4.8µH Sumida CDEP134	IRF7460	IRF7476	2SD1802 (3A or less)	2 x 1000µF 10MBZ1000M 10x12.5	2 x 1800µF 6.3MBZ1800M 10x16
15A	1.6µH Sumida CDEP134	IRF7821	IRF7832	2SD1802 (3A or less)	2 x 1800µF 10MBZ1800M 10x20	2 x 3300µF 6.3MBZ3300M 10x23
20A	0.5µH Pulse PG0006.601	2 x IRF7821	2 x IRF7832	2SD1802 (3A or less)	3 x 1500µF 10MBZ1500M 10x16	3 x 3300µF 6.3MBZ3300M10x23

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)

16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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