DC-Coupled, UCSP 3.125Gbps Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}, V_{TI}, and V_{TO} .....-0.5V to +6V
Continuous Output Current.....-25mA to +25mA
IN±, OUT±, EN.....-0.5V to (V_{CC} + 0.5V)

Operating Ambient Temperature Range .....0°C to +85°C
Storage Ambient Temperature Range.....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Input Termination Voltage	V_{TI}		1.1		V_{CC}	V
Output Termination Voltage	V_{TO}		1.1		V_{CC}	V
Supply Noise Tolerance		10Hz ≤ f < 100Hz		100		mV_{P-P}
		100Hz ≤ f < 1MHz		40		
		1MHz ≤ f ≤ 2.5GHz		10		
Operating Ambient Temperature			0	25	85	°C
Bit Rate		NRZ data	2.488		3.125	Gbps
CID		Consecutive identical digits			100	bits

ELECTRICAL CHARACTERISTICS

(Typical values are at +3.3V and at T_A = +25°C, unless otherwise noted. Specifications guaranteed over specified operating conditions.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 1)		EN = high		45	67	mA
		EN = low		14	32	
Output Driver Supply Current		(Note 2)		9	14	mA
Input Swing (Note 1)		Measured differentially at point A (Figure 1)	400		1000	mV_{P-P}
Input Common-Mode Voltage Range		(Note 1)	V_{TI} - 0.25V		V_{TI} - 0.10V	V
Input Return Loss		100MHz to 2.5GHz		10		dB
Input Resistance		Single ended (Note 1)	42.5	50	57.5	Ω
Output Swing (Notes 1, 3)		EN = high	440	525	680	mV_{P-P}
		EN = low		30		
Output Common-Mode Voltage				V_{TO} - 0.112V		V
Output Resistance		Single ended (Note 1)	42.5	50	57.5	Ω
Output Return Loss		100MHz to 2.5GHz		10		dB
Output Transition Time	t_r, t_f	20% to 80% (Notes 2, 4)	40	70	100	ps
Differential Skew		Difference in 50% crossing between OUT+ and OUT-		10		ps

ELECTRICAL CHARACTERISTICS (continued)

(Typical values are at +3.3V and at T_A = +25°C, unless otherwise noted. Specifications guaranteed over specified operating conditions.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Residual Deterministic Jitter Output (2.5Gbps, CJTPAT) (Notes 2, 5)		0in, 6-mil FR4		0.01	0.10	UI
		10in, 6-mil FR4		0.04	0.10	
		20in, 6-mil FR4		0.05	0.10	
		30in, 6-mil FR4		0.05	0.15	
		40in, 6-mil FR4		0.07	0.15	
		3m Tensolite cable		0.03	0.10	
		5m Tensolite cable		0.1	0.20	
		10m Tensolite cable		0.14	0.25	
Residual Deterministic Jitter Output (2.5Gbps, 2^7 PRBS + 100 CID) (Notes 2, 6)		0in, 6-mil FR4		0.01	0.10	UI
		10in, 6-mil FR4		0.06	0.10	
		20in, 6-mil FR4		0.11	0.15	
		30in, 6-mil FR4		0.15	0.20	
		3m Tensolite cable		0.09	0.15	
Residual Deterministic Jitter Output (3.125Gbps, CJTPAT) (Notes 2, 7)		0in, 6-mil FR4		0.01	0.10	UI
		10in, 6-mil FR4		0.02	0.10	
		20in, 6-mil FR4		0.03	0.15	
		30in, 6-mil FR4		0.06	0.15	
		40in, 6-mil FR4		0.11	0.25	
		3m Tensolite cable		0.05	0.10	
		5m Tensolite cable		0.16	0.25	
Random Jitter Output		(Notes 2, 4)		2	3	ps_{RMS}
Latency		From IN to OUT		0.3		ns
Low-Frequency Cutoff				15		kHz
LVTTL Input High Voltage	V_{IH}	(Note 1)	1.5			V
LVTTL Input Low Voltage	V_{IL}	(Note 1)			0.5	V
LVTTL Input High Current	I_{IH}	(Note 1)			10	µA
LVTTL Input Low Current	I_{IL}	(Note 1)			10	µA

Note 1: Production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Specifications are guaranteed by design and characterization.

Note 3: Measured differentially at point C with 50Ω ±1% at each side (Figure 1).

Note 4: Using a 0000011111 or equivalent pattern at selected bit rate. Measured at 600mV_{P-P} input voltage, 10m cable or 40in FR4, at 2.5Gbps and within 2in of output pins.

Note 5: Difference in peak-to-peak deterministic jitter between reference points A and C in Figure 1. Evaluated at 2.5Gbps with CJTPAT.

Note 6: Difference in peak-to-peak deterministic jitter between reference points A and C in Figure 1. Evaluated at 2.5Gbps with a PRBS 2^7 with 100 CIDs input pattern.

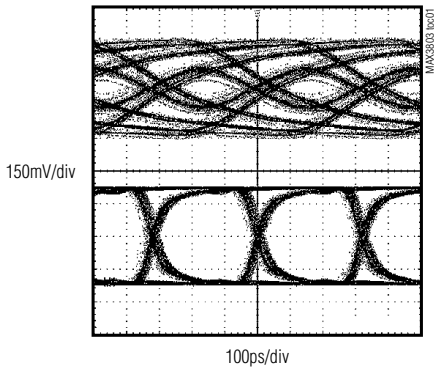
Note 7: Difference in peak-to-peak deterministic jitter between reference points A and C in Figure 1. Evaluated at 3.125Gbps with CJTPAT.

DC-Coupled, UCSP 3.125Gbps Equalizer

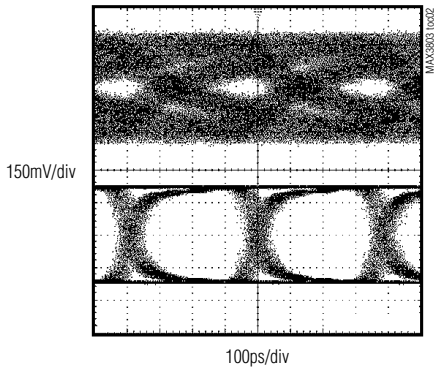
Typical Operating Characteristics

(V_{CC} = +3.3V, V_{TI} = +1.1V, V_{TO} = +1.1V, and T_A = +25°C, unless otherwise noted.)

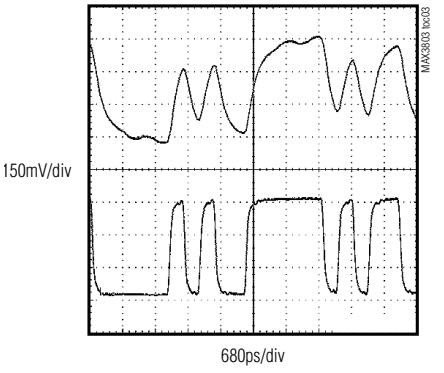
40in, 6-mil FR4 AT 3.125Gbps WITH CJTPAT (BEFORE EQUALIZATION, AFTER EQUALIZATION)



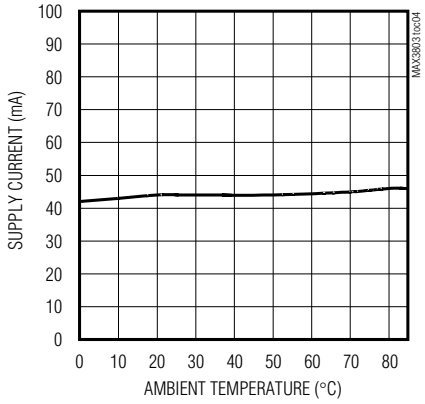
20ft TENSOLITE CABLE AT 2.48832Gbps WITH PRBS 2^{23} - 1 (BEFORE EQUALIZATION, AFTER EQUALIZATION)



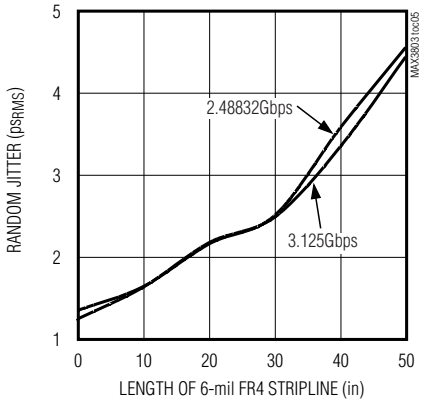
30in, 6-mil FR4 AT 3.125Gbps WITH K28.5 (BEFORE EQUALIZATION, AFTER EQUALIZATION)



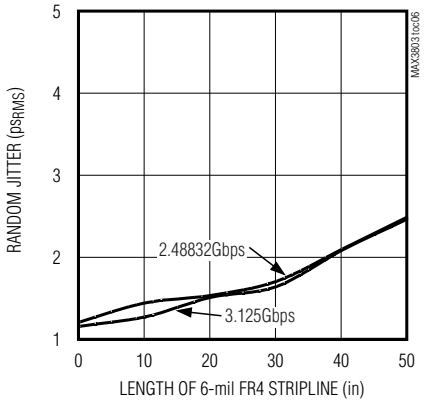
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



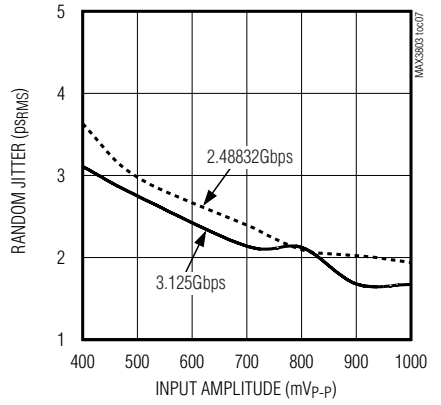
RANDOM JITTER vs. LENGTH (IN± = 400mVP-P, PATTERN = K28.7)



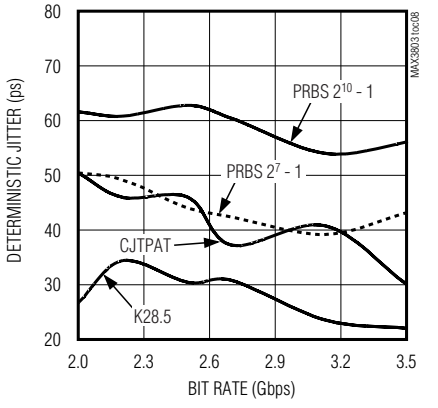
RANDOM JITTER vs. LENGTH (IN± = 800mVP-P, PATTERN = K28.7)



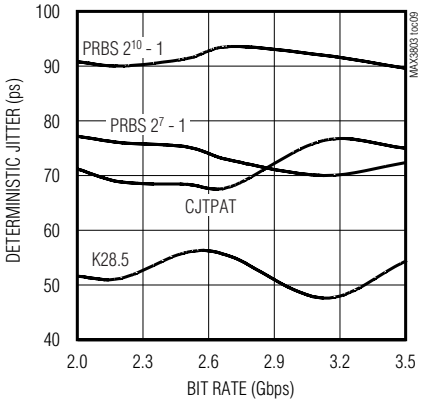
RANDOM JITTER vs. INPUT AMPLITUDE (40in, 6-mil FR4 STRIPLINE, PATTERN = K28.7)



DETERMINISTIC JITTER vs. BIT RATE (30in, 6-mil FR4 STRIPLINE, IN± = 1000mVP-P)



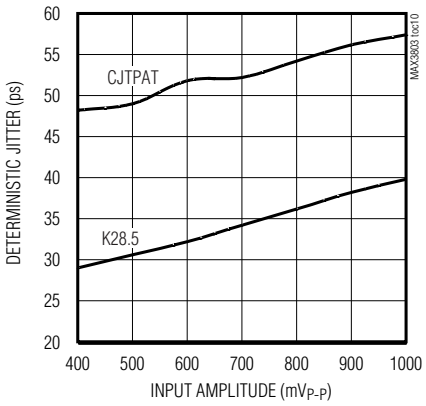
DETERMINISTIC JITTER vs. BIT RATE (33ft, 28AWG TENSOLITE CABLE, IN± = 400mVP-P)



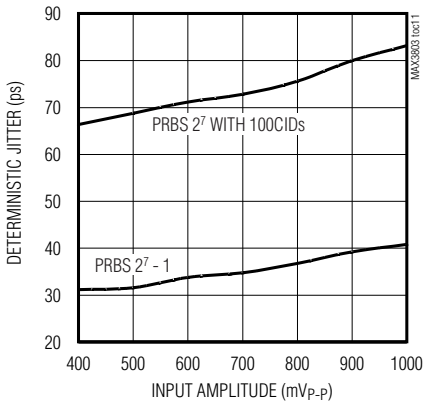
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{TI} = +1.1V, V_{TO} = +1.1V, and T_A = +25°C, unless otherwise noted.)

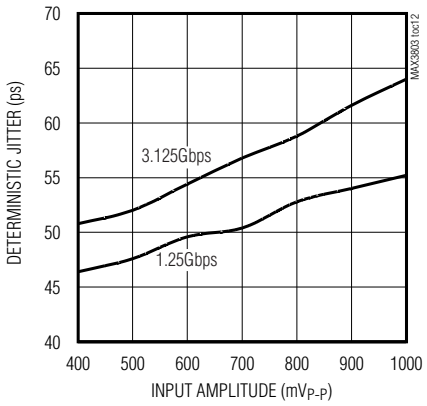
DETERMINISTIC JITTER vs. INPUT AMPLITUDE (40in, 6-mil FR4 STRIPLINE, 3.125Gbps)



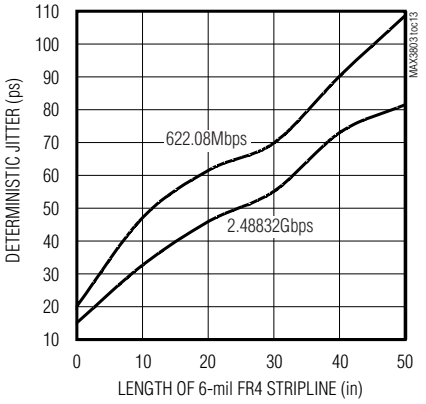
DETERMINISTIC JITTER vs. INPUT AMPLITUDE (30in, 6-mil FR4 STRIPLINE, 2.488Gbps)



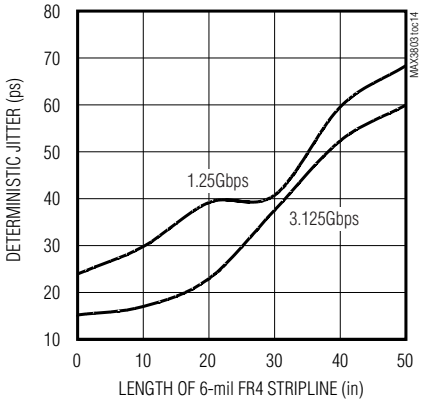
DETERMINISTIC JITTER vs. INPUT AMPLITUDE (33ft, 28AWG TENSOLITE CABLE, PATTERN = K28.5)



DETERMINISTIC JITTER vs. LENGTH (IN± = 800mVP-P, PATTERN = PRBS 2^{10} - 1)



DETERMINISTIC JITTER vs. LENGTH (IN± = 600mVP-P, PATTERN = CJTPAT)



Pin Description

PIN	NAME	FUNCTION
A1	V_{TO}	Output Termination Voltage
A2	EN	Enable. Connect to V_{CC} to enable the equalizer core. Connect to GND to disable the equalizer core, TTL. Do not leave unconnected.
A3, A4	N.C.	No Connection
A5	V_{TI}	Input Termination Voltage
B1	OUT+	Positive Data Output, CML
B5	IN+	Positive Data Input, CML
C1	OUT-	Negative Data Output, CML
C5	IN-	Negative Data Input, CML
D1, D5	GND	Supply Ground
D2, D3, D4	V_{CC}	Core Supply Voltage

DC-Coupled, UCSP 3.125Gbps Equalizer

Detailed Description and Applications Information

The MAX3803 is an adaptive equalizer designed to extend the reach of transmission lines in high-frequency backplane and rack-to-rack interconnect applications. The MAX3803 automatically adjusts to attenuation caused by skin-effect and dielectric losses. Although optimized for coded and scrambled data between 2.488Gbps and 3.125Gbps, the MAX3803 provides effective compensation for rates between 1Gbps and 3.2Gbps.

The MAX3803 consists of low common-mode input and output buffers, an equalizer core, a DC-offset-correction loop, and a limiting amplifier (Figure 2).

Low Common-Mode Input and Output

The MAX3803 permits DC-coupling to CML transmitters and receivers that require termination voltages as low as 1.1V and as high as V_{CC}. Use the V_{TI} and V_{TO} pins to maintain compatible common-mode levels between the data source and load. V_{TI} and V_{TO} are independent and can be used to bridge two common-mode requirements without the use of DC-blocking capacitors. See Figure 3 and Figure 4 for the equivalent input and output structures.

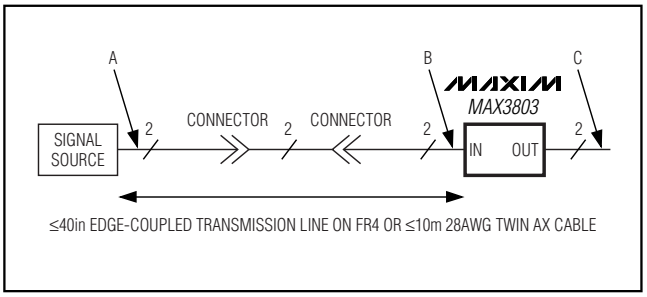


Figure 1. Backplane Interconnect

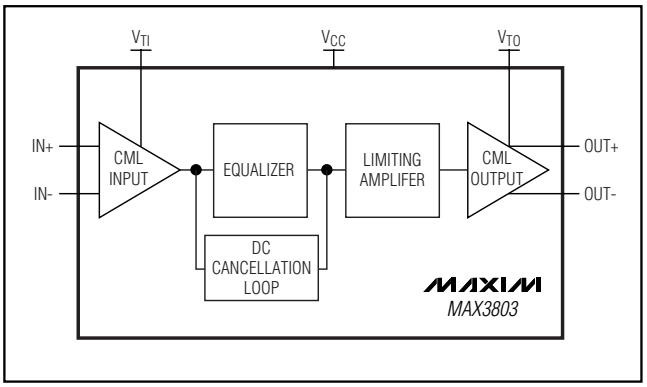


Figure 2. Functional Diagram

Media Equalization

Equalization at the input compensates for high-frequency loss encountered with FR4 stripline (edge-coupled) or 28AWG twin ax. The equalizer core is an amplifier with a self-adjusting frequency response.

DC Cancellation Loop

The DC cancellation loop removes the pulse-width distortion caused by internal offsets. The closed-loop response creates a low-frequency cutoff of approximately 15kHz, below which the offset control tracks the AC signal. This also sets the limit on the maximum time

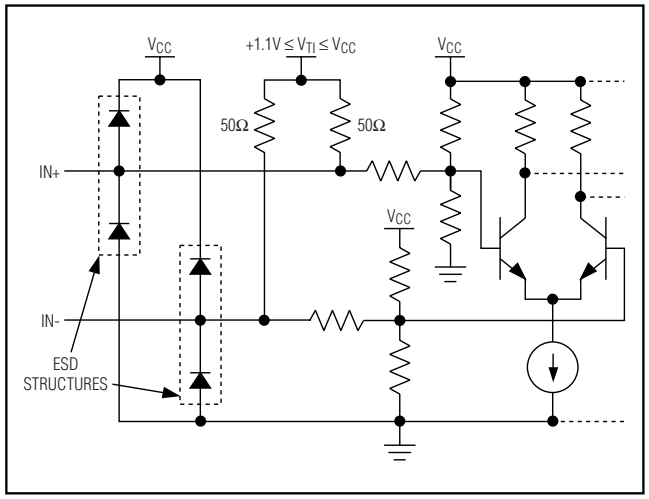


Figure 3. CML Input Structure

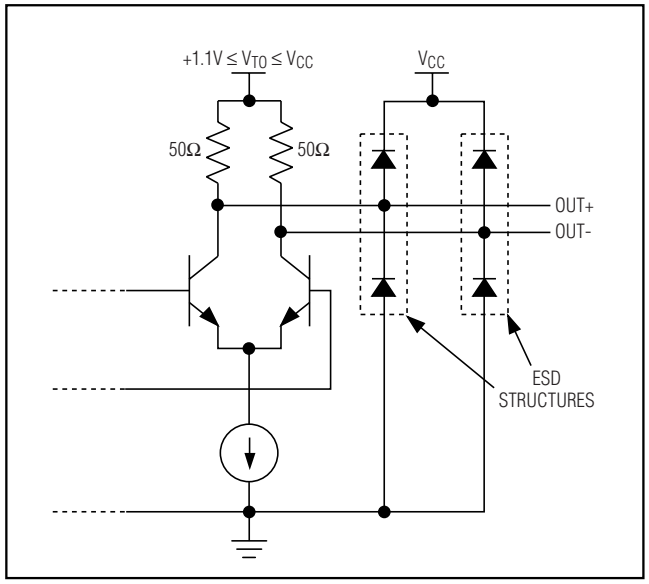


Figure 4. CML Output Structure

required to reach a balanced mark/space ratio (i.e., 50%). This permits the use of scrambled data as found in SONET and SDH transmissions.

Limiting Amplifier

The limiting amplifier limits the outputs of the equalizer so all frequencies are at the same output voltage level.

Enable Function

Connect the EN pin to V_{CC} to enable the equalizer core. Connect the EN pin to GND to disable the equalizer core when valid data is not present to save power. When EN is low, the outputs are static with approximately 30mV_{P-P} differential. This pin must be connected to V_{CC} or GND.

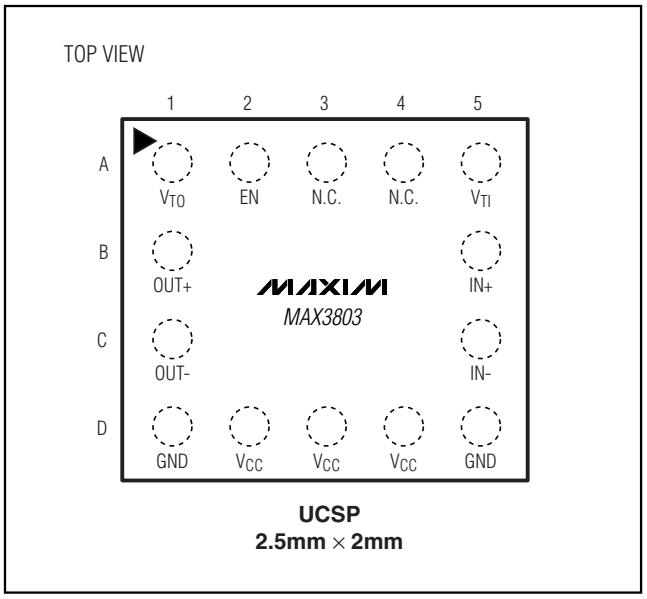
Packaging

The MAX3803 is packaged in a 2.5mm × 2mm, 5 × 4 chip-scale package (USCP). The six center ball positions (B2, B3, B4, C2, C3, C4) are not populated, leaving fourteen perimeter balls. This package does not require underfill over an ambient temperature range of 0°C to +85°C. Thermal dissipation is provided through the GND connection. Go to Maxim's website, www.maxim-ic.com, for the latest packaging information and details about UCSP layout and handling.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3803 high-speed inputs and outputs. Power-supply decoupling should be placed as close to the V_{CC} as possible. To reduce feedthrough, isolate input signals from output signals.

Pin Configuration

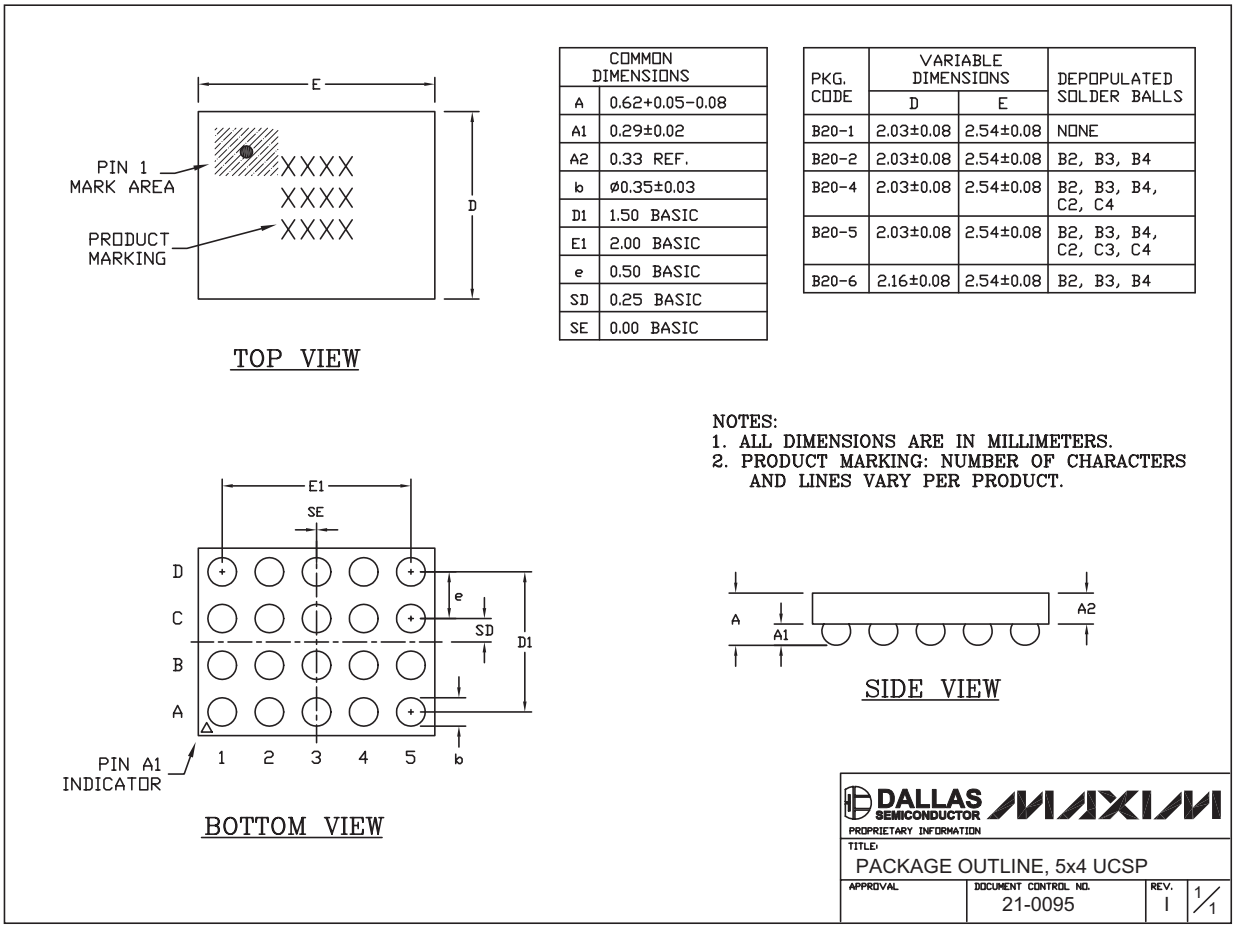


UCSP
2.5mm × 2mm

DC-Coupled, UCSP 3.125Gbps Equalizer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B20-1	2.03±0.08	2.54±0.08	NONE
B20-2	2.03±0.08	2.54±0.08	B2, B3, B4
B20-4	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C4
B20-5	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C3, C4
B20-6	2.16±0.08	2.54±0.08	B2, B3, B4