Low-Cost, Low-Power, 8-Bit DACs with 2-Wire Serial Interface in SOT23

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUT, SCL, SDA to GND .....-0.3V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW

Operating Temperature Ranges
MAX538_ _EUK-T .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX5380), V_{DD} = +4.5V to +5.5V (MAX5381), V_{DD} = +2.7V to +5.5V (MAX5382); R_L = 10kΩ; C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Integral Linearity Error	INL	(Note 1)				±1	LSB
Differential Linearity Error	DNL	Guaranteed monotonic				±1	LSB
Offset Error		(Note 2)			±1	±25	mV
Offset Error Supply Rejection		MAX5382 (Notes 2, 3)		60			dB
Offset Error Temperature Coefficient		(Note 2)	MAX5380/MAX5381		3		ppm/°C
			MAX5382		1		
Full-Scale Error		Code = 255	MAX5380/MAX5381			10	% of ideal FS
			MAX5382			5	
Full-Scale Error Supply Rejection		Code = 255, MAX5380/MAX5281 (Note 4)				50	dB
Full-Scale Error Temperature Coefficient		Code = 255	MAX5380/MAX5381		±40		ppm/°C
			MAX5382		±10		
DAC OUTPUT							
Internal Reference (Note 5)	REF	MAX5380		1.8	2	2.2	V
		MAX5381		3.6	4	4.4	
		MAX5382		0.85 x V_{DD}	0.9 x V_{DD}	0.95 x V_{DD}	
Output Load Regulation		Code = 255, 0 to 100µA			0.5		LSB
		Code = 0, 0 to 100µA			0.5		
Output Resistance		V_{OUT} = 0 to V_{DD}, power-down mode			10		kΩ
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative			0.4		V/µs
Output Settling Time		To 1/2 LSB, 50kΩ and 50pF load (Note 6)			20		µs
Digital Feedthrough		Code = 0, all digital inputs from 0 to V_{DD}			2		nVs
Digital-Analog Glitch Impulse		Code 127 to 128			40		nVs
Wake-Up Time		From software shutdown			50		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX5380), V_{DD} = +4.5V to +5.5V (MAX5381), V_{DD} = +2.7V to +5.5V (MAX5382); R_L = 10kΩ; C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX5380		2.7		3.6	V
		MAX5381		4.5		5.5	
		MAX5382		2.7		5.5	
Supply Current	I_{DD}	No load, all digital inputs at 0 or V_{DD}, code = 255			150	230	µA
		Shutdown mode				1	
DIGITAL INPUTS (SCL, SDA)							
Input Low Voltage	V_{IL}					0.3 x V_{DD}	V
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Hysteresis	V_{HYS}				0.05 x V_{DD}		V
Input Capacitance	C_{IN}	(Note 7)			10		pF
Input Leakage Current	I_{IN}					±10	µA
Pulse Width of Spike Suppressed	t_{SP}			0		50	ns
DIGITAL OUTPUT (SDA, open drain)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
		I_{SINK} = 6mA				0.6	
Output Fall Time	t_{OF}	$V_{IH(MIN)}$ to $V_{IL(MAX)}$, bus capacitance = 10pF to 400pF	I_{SINK} = 3mA			250	ns
			I_{SINK} = 6mA			250	

TIMING CHARACTERISTICS

(Figure 3; V_{DD} = +2.7V to +3.6V (MAX5380), V_{DD} = +4.5V to +5.5V (MAX5381), V_{DD} = +2.7V to +5.5V (MAX5382); R_L = 10kΩ; C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time Repeated for a START Condition	$t_{HD:STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns

Low-Cost, Low-Power, 8-Bit DACs with 2-Wire Serial Interface in SOT23

TIMING CHARACTERISTICS (continued)

(Figure 3; V_{DD} = +2.7V to +3.6V (MAX5380), V_{DD} = +4.5V to +5.5V (MAX5381), V_{DD} = +2.7V to +5.5V (MAX5382); R_L = 10kΩ; C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 7)

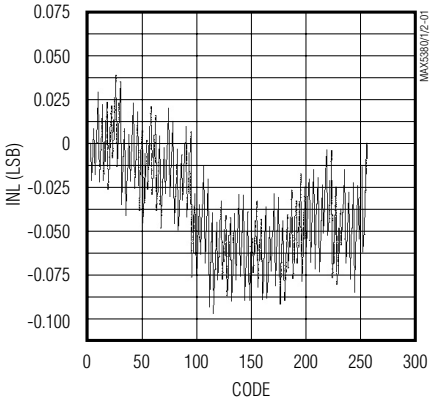
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time of Both SDA and SCL Signals	t_r				300	ns
Fall Time of Both SDA and SCL Signals	t_f				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF

Note 1: Guaranteed from code 5 to code 255.
Note 2: The offset value extrapolated from the range over which the INL is guaranteed.
Note 3: MAX5382 tested at V_{DD} = +5V ±10%.
Note 4: MAX5380 tested at V_{DD} = +3V ±10%, MAX5381 tested at V_{DD} = 5V ±10%.
Note 5: Actual output voltages at full scale are 255/256 x V_{REF}.
Note 6: Output settling time is measured by taking the code from code 5 to 255, and from code 255 to 5.
Note 7: Guaranteed by design.

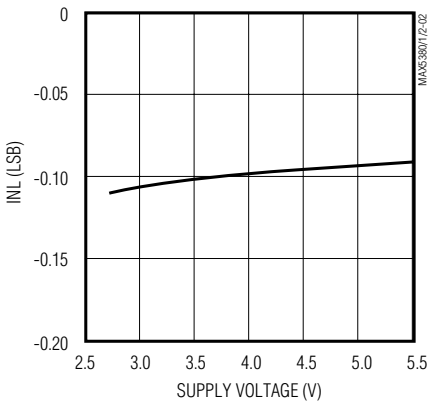
Typical Operating Characteristics

(V_{DD} = +3.0V (MAX5380), V_{DD} = +5.0V (MAX5381/MAX5382); R_L = 10kΩ, T_A = +25°C, unless otherwise noted.)

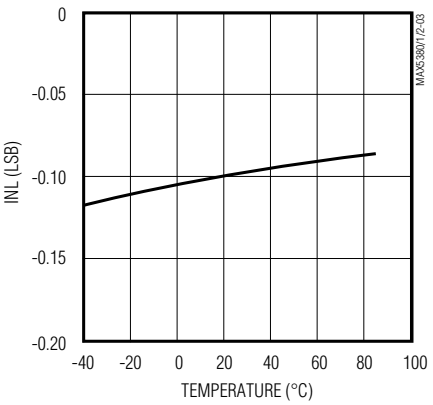
INTEGRAL NONLINEARITY vs. CODE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



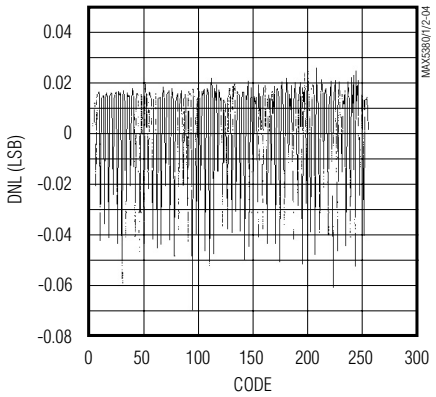
INTEGRAL NONLINEARITY vs. TEMPERATURE



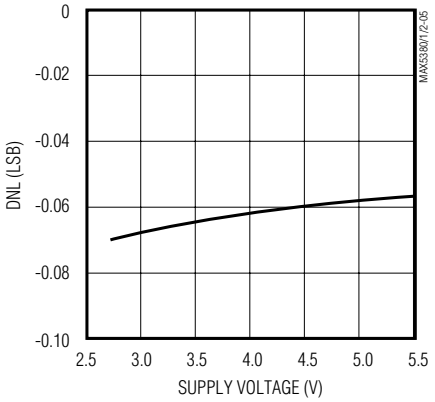
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5380), V_{DD} = +5.0V (MAX5381/MAX5382); R_L = 10kΩ, T_A = +25°C, unless otherwise noted.)

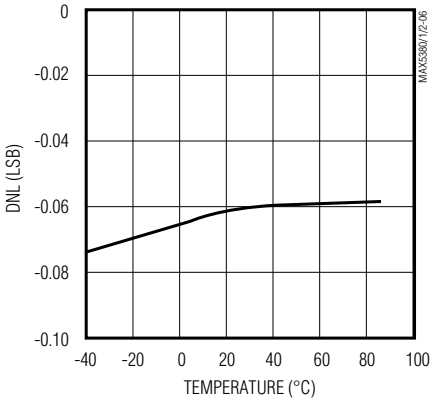
DIFFERENTIAL NONLINEARITY vs. CODE



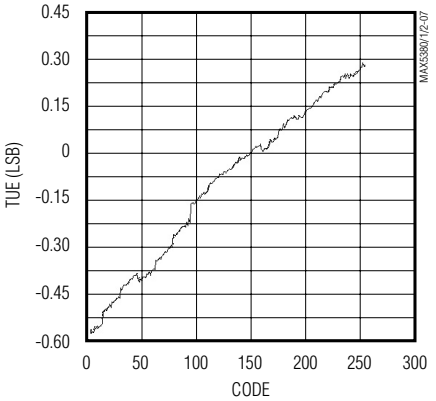
DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



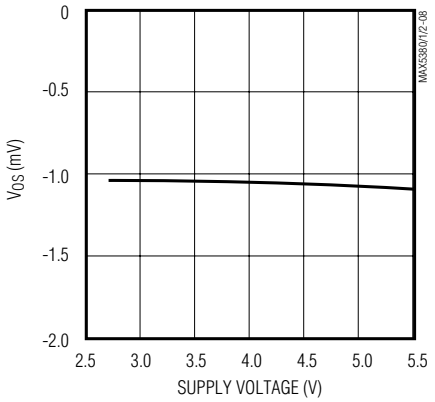
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



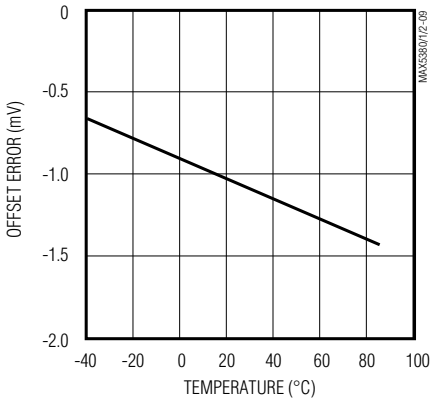
TOTAL UNADJUSTED ERROR vs. CODE



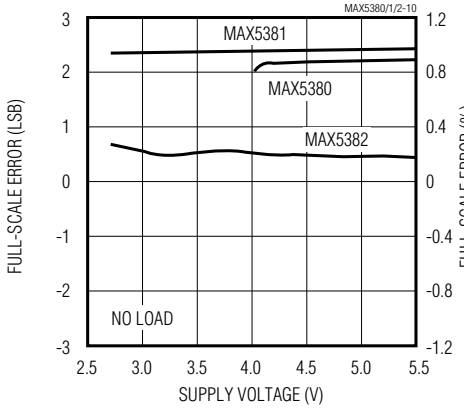
OFFSET ERROR vs. SUPPLY VOLTAGE



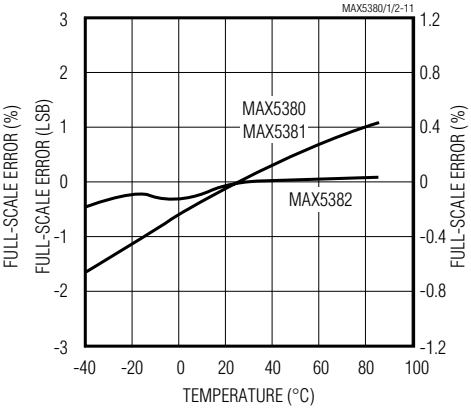
OFFSET ERROR vs. TEMPERATURE



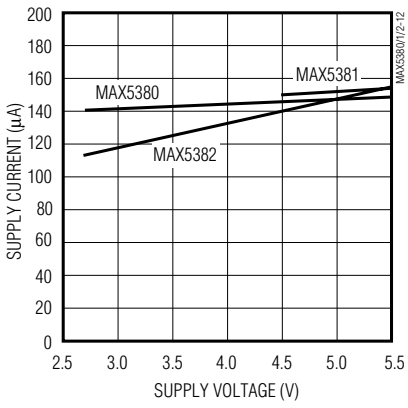
FULL-SCALE ERROR vs. SUPPLY VOLTAGE



FULL-SCALE ERROR vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

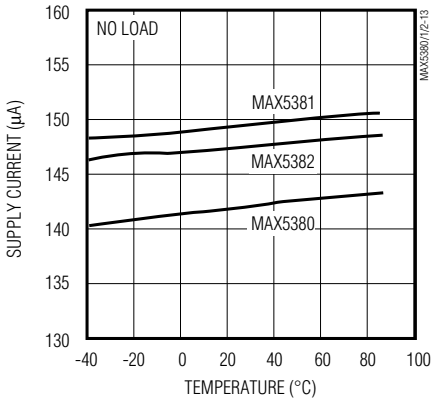


Low-Cost, Low-Power, 8-Bit DACs with 2-Wire Serial Interface in SOT23

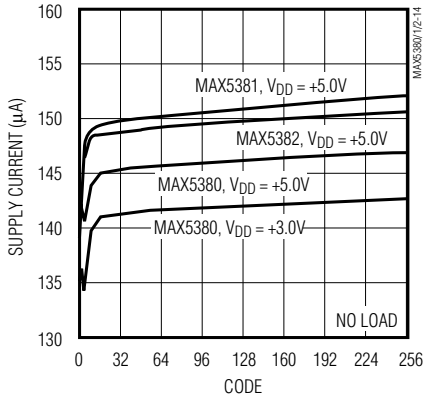
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5380), V_{DD} = +5.0V (MAX5381/MAX5382); R_L = 10kΩ, T_A = +25°C, unless otherwise noted.)

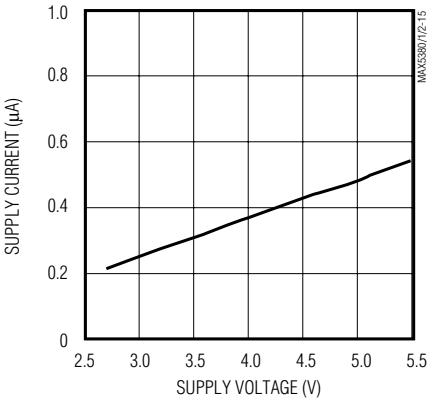
SUPPLY CURRENT vs. TEMPERATURE



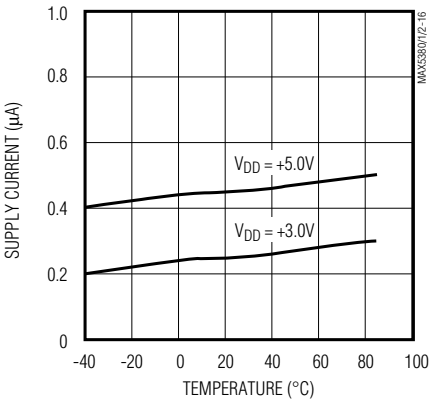
SUPPLY CURRENT vs. CODE



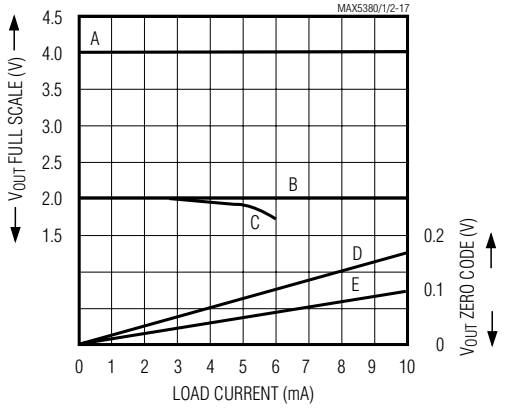
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

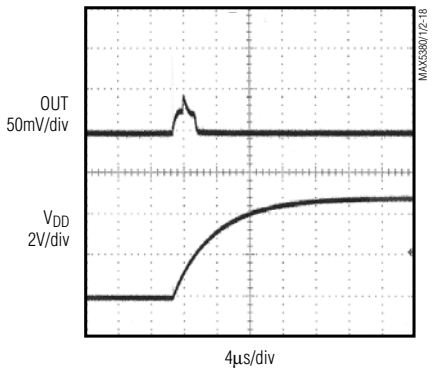


OUTPUT LOAD REGULATION



A: MAX5361/MAX5362, V_{DD} = 4.5V FULL-SCALE OR SOURCING
B: MAX5360, FULL-SCALE, V_{DD} = 2.7V SINKING, V_{DD} = 5.0V SOURCING
C: MAX5360, FULL-SCALE, V_{DD} = 2.7V SOURCING
D: ZERO CODE, V_{DD} = 2.7V SINKING
E: ZERO CODE, V_{DD} = 5.5V SINKING

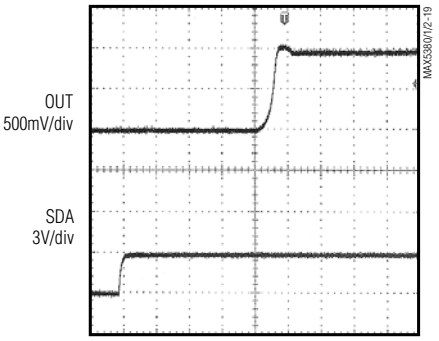
OUTPUT VOLTAGE ON POWER-UP



Typical Operating Characteristics (continued)

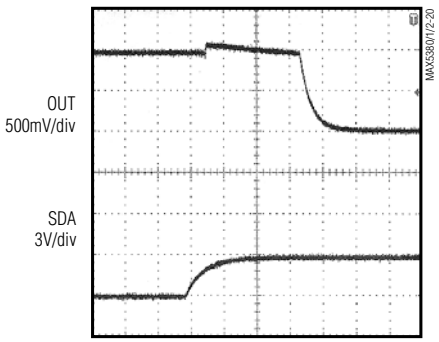
(V_{DD} = +3.0V (MAX5380), V_{DD} = +5.0V (MAX5381/MAX5382); R_L = 10kΩ, T_A = +25°C, unless otherwise noted.)

OUTPUT VOLTAGE EXITING SHUTDOWN



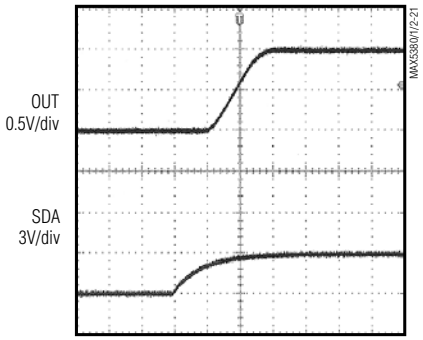
MAX5380, SHDN TO 0x80

OUTPUT VOLTAGE ENTERING SHUTDOWN



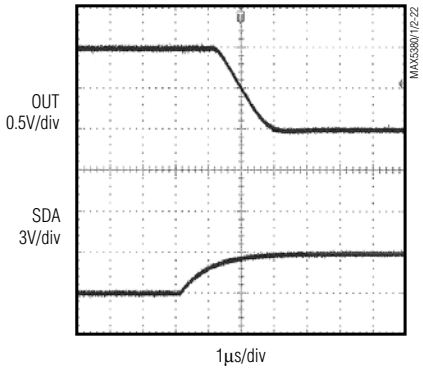
MAX5380, 0x80 TO SHDN

OUTPUT SETTLING FROM 1/4 FS TO 3/4 FS



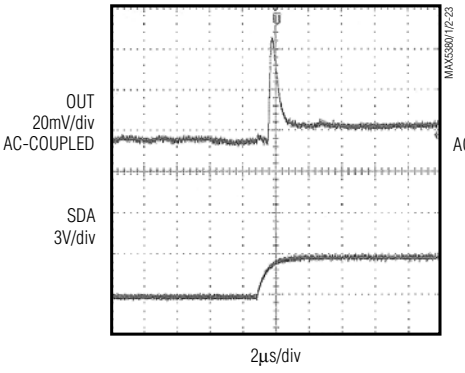
MAX5380

OUTPUT SETTLING FROM 3/4 FS TO 1/4 FS



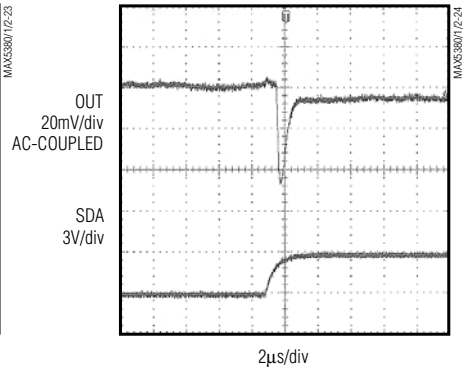
MAX5380

OUTPUT SETTLING 1LSB STEP UP



MAX5380, 0x7F TO 0x80

OUTPUT SETTLING 1LSB STEP DOWN



MAX5380, 0x80 TO 0x7F

Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Voltage Output
2	GND	Ground
3	V_{DD}	Power-Supply Input
4	SDA	Serial Data Input
5	SCL	Serial Clock Input

Low-Cost, Low-Power, 8-Bit DACs with 2-Wire Serial Interface in SOT23

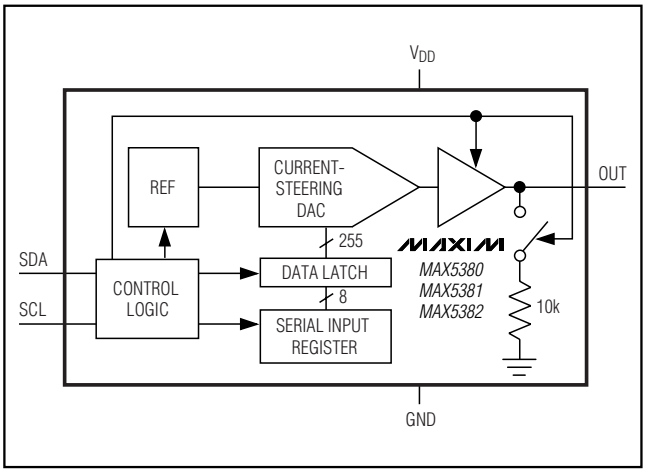


Figure 1. Functional Diagram

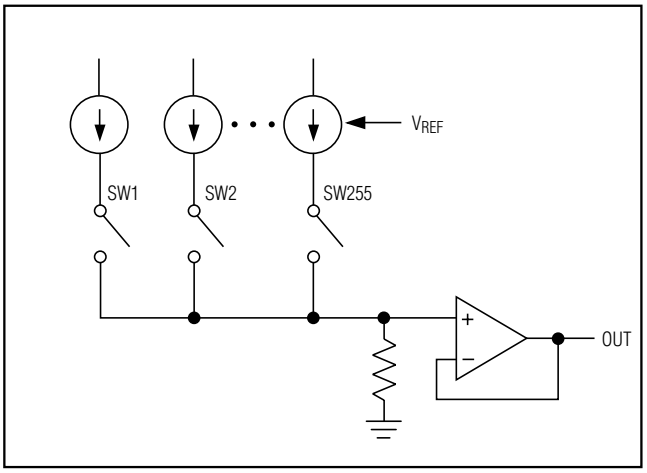


Figure 2. Current-Steering Topology

Table 1. Unipolar Code Output Voltage

DAC CODE	OUTPUT VOLTAGE		
	MAX5380	MAX5381	MAX5382
1111 1111	2V x (255 / 256)	4V x (255 / 256)	0.9 x V_{DD} x (255 / 256)
1000 0000	+1V	+2V	0.9 x V_{DD} / 2
0000 0001	7.8mV	15.6mV	0.9 x V_{DD} / 256
0000 0000	0	0	0

Detailed Description

The MAX5380/MAX5381/MAX5382 voltage-output, 8-bit digital-to-analog converters (DACs) offer full 8-bit performance with less than 1LSB integral nonlinearity error and less than 1LSB differential nonlinearity error, ensuring monotonic performance. The devices use a simple 2-wire, fast-mode I^2C-compatible serial interface that operates at up to 400kHz. The MAX5380/MAX5381/MAX5382 include an internal reference, an output buffer, and a low-current shutdown mode, which make these devices ideal for low-power, highly integrated applications (See Figure 1. *Functional Diagram).*

Analog Section

The MAX5380/MAX5381/MAX5382 employ a current-steering DAC topology as shown in Figure 2. At the core of the DAC is a reference voltage-to-current converter (V/I) that generates a reference current. This current is mirrored to 255 equally weighted current sources. DAC switches control the outputs of these current mirrors so that only the desired fraction of the total current-mirror currents is steered to the DAC output. The current is then converted to a voltage across a resistor, and this voltage is buffered by the output buffer amplifier.

Output Voltage

Table 1 shows the relationship between the DAC code and the analog output voltage. The 8-bit DAC code is binary unipolar with 1LSB = V_{REF} / 256. The MAX5380/MAX5381 have a full-scale output voltage of (+2V - 1LSB) and (+4V - 1LSB), respectively, set by the internal references. The MAX5382 has a full-scale output voltage of (0.9 x V_{DD} - 1LSB).

Output Buffer

The DAC voltage output is an internally buffered unity-gain follower that typically slews at ±0.4V/µs. The output can swing from 0 to full scale. With a 1/4 FS to 3/4 FS output transition, the amplifier outputs typically settle to 1/2LSB in less than 5µs when loaded with 10kΩ in parallel with 50pF. The buffer amplifiers are stable with any combination of resistive loads >10kΩ and capacitive loads <50pF.

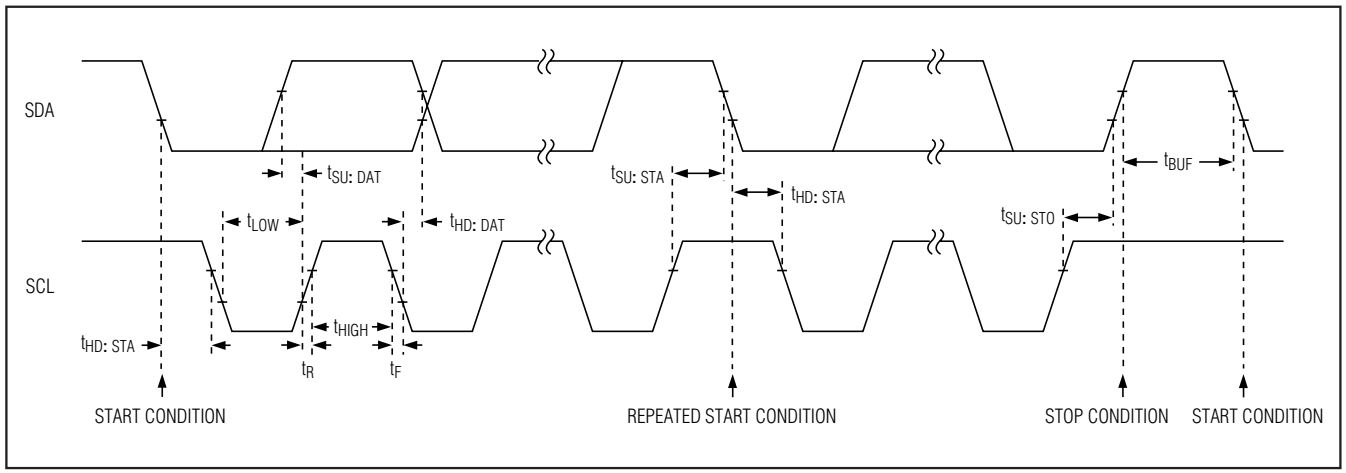


Figure 3. 2-Wire Serial Interface Timing Diagram

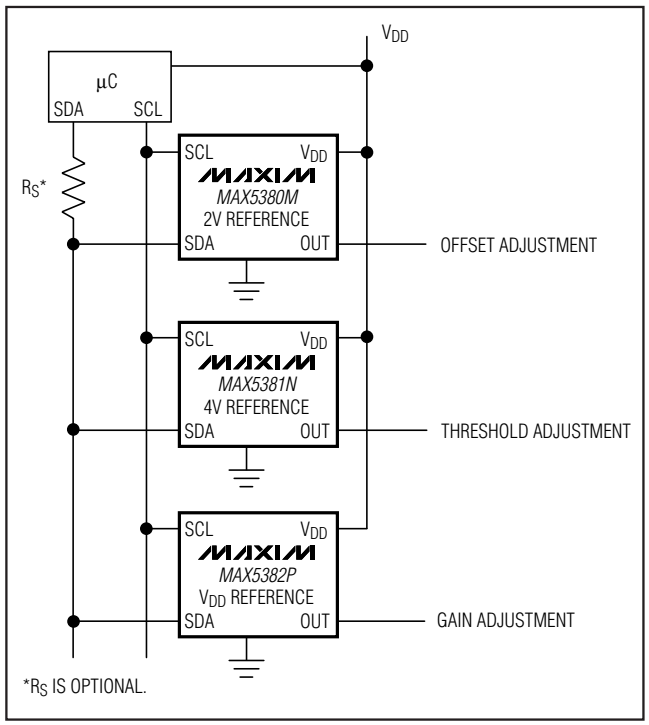


Figure 4. Typical Application Circuit

Power-On Reset

The MAX5380/MAX5381/MAX5382 have a power-on reset circuit to set the DAC's output to 0 when V_{DD} is first applied or when V_{DD} dips below 1.7V (typ). This ensures that unwanted DAC output voltages will not occur immediately following a system startup, such as after a loss of power. The output glitch at startup is typically less than 50mV.

Shutdown Mode

The MAX5380/MAX5381/MAX5382 include a software-controlled shutdown mode that reduces the supply current to <1µA. All internal circuitry is disabled, and an internal 10kΩ resistor is placed from OUT to GND to ensure 0V at OUT while in shutdown. The device enters shutdown in less than 5µs and exits shutdown in less than 50µs.

Digital Section

Serial Interface

The MAX5380/MAX5381/MAX5382 use a simple 2-wire serial interface requiring only two I/O lines (2-wire bus) of a standard microprocessor (µP) port. Figure 3 shows the timing diagram for signals on the 2-wire bus.

The two bus lines (SDA and SCL) must be high when the bus is not in use. The MAX5380/MAX5381/MAX5382 are receive-only devices (slaves) and must be controlled by a bus master device. Figure 4 shows a typical application where up to four devices can be connected to the bus, provided they have different address settings. External pull-up resistors are not necessary on these lines (when driven by push-pull drivers), though these DACs can be used in applications where pull-up resistors are required (such as in I^2C systems) to maintain compatibility with existing circuitry. The serial interface operates at SCL rates up to 400kHz. The SDA state is allowed to change only while SCL is low, with the exception of START and STOP conditions as shown in Figure 5. Each transmission consists of a START condition sent by the bus master

Low-Cost, Low-Power, 8-Bit DACs with 2-Wire Serial Interface in SOT23

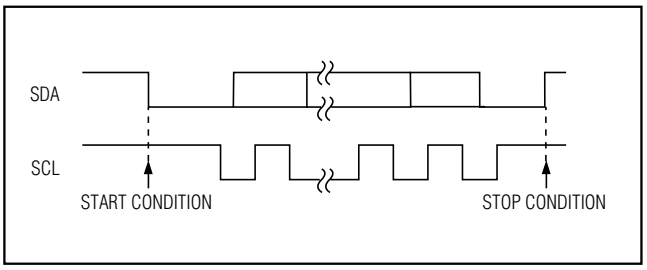


Figure 5. START and STOP Conditions

device, followed by the MAX5380/MAX5381/MAX5382s' preset slave address, a power-mode bit, the DAC data, and finally, a STOP condition (Figure 6). The bus is then free for another transmission.

SDA's state is sampled and therefore must remain stable while SCL is high. Data is transmitted in 8-bit bytes. Nine clock cycles are required to transfer each byte to the MAX5380/MAX5381/MAX5382. Release SDA during the 9th clock cycle since the selected device acknowledges receipt of the byte by pulling SDA low during this time. A series resistor on the SDA line may be needed if the master's output is forced high while the selected device acknowledges (Figure 4).

Slave Address

The MAX5380/MAX5381/MAX5382 are available with one of four preset slave addresses. Each address option is identified by the suffix L, M, N, or P added to the part number. The address is defined as the 7MSBs sent by the master after a START condition. The address options are 0x60, 0x62, 0x64, 0x66 (left justified with LSB set to 0). The 8th bit, typically used to define a write or read protocol, sets the device's power mode (SHDN). The device is powered-down when SHDN is set to one. During a device search routine, the MAX5380/MAX5381/MAX5382 acknowledge both options (SHDN = 0 or SHDN = 1), but do not change their power state if a stop condition (or restart) is issued immediately. The second byte (DAC data) must be sent/received for the device to update both power mode and DAC output.

DAC Data

The 8-bit DAC data is decoded as straight binary MSB first with 1LSB = V_{REF} / 256 and converted into the corresponding analog voltage as shown in Table 1. After receiving the data byte, the devices acknowledge its receipt and expect a STOP condition, at which point the DAC output is updated.

The MAX5380/MAX5381/MAX5382 update the output and the power mode only if the second byte is clocked in (SHDN = 0) or out (SHDN = 1) of the device. When SHDN = 1, the master will read all ones when clocking out a data byte. The MAX5380/MAX5381/MAX5382 do not drive SDA except for the acknowledge bit.

I^2C Compatibility

The MAX5380/MAX5381/MAX5382 are compatible with existing I^2C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the 9th clock pulse. Figure 7 shows a typical I^2C application. The communication protocol supports standard I^2C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The devices' address is compatible with the 7-bit I^2C addressing protocol only. No 10-bit formats

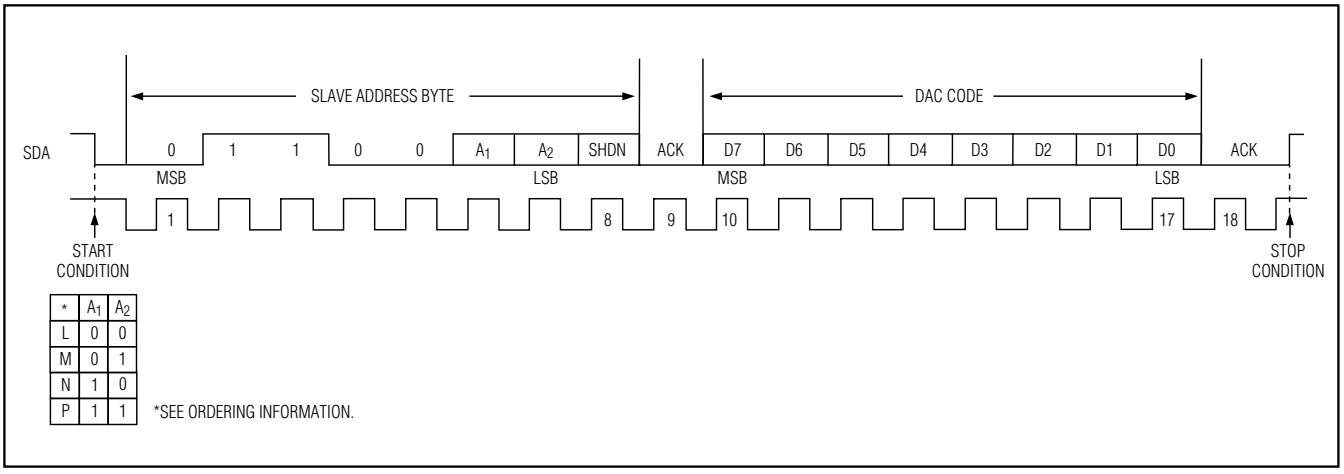


Figure 6. A Complete Serial Transmission

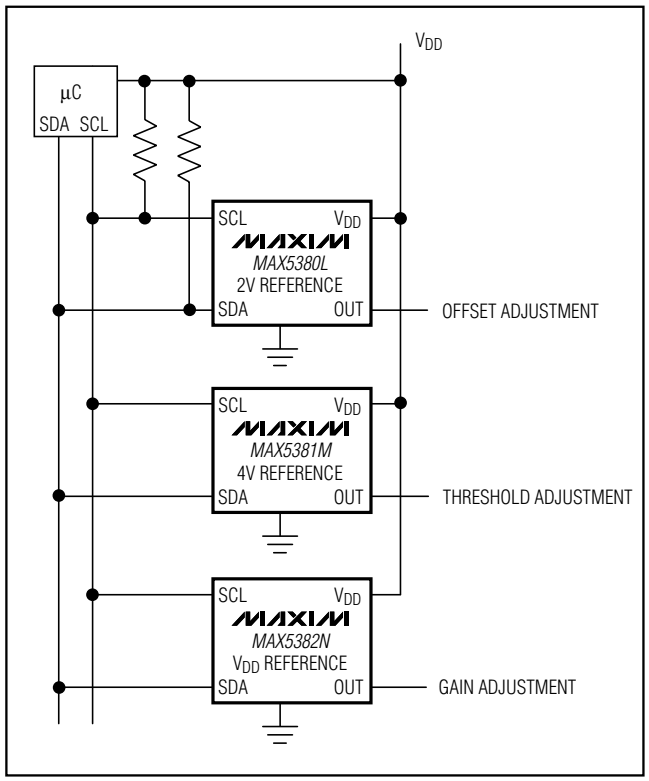


Figure 7. Typical I²C Application

are supported. RESTART protocol is supported, but an immediate STOP condition is necessary to update the DAC. The 8th bit of the address byte, typically used to indicate a read or write protocol, is used in the MAX5380/MAX5381/MAX5382 to enter or exit shutdown mode. When MAX5380/MAX5381/MAX5382 are addressed in I²C read mode, they enter shutdown mode.

Applications Information

Digital Inputs and Interface Logic

The serial 2-wire interface has logic levels defined as V_{IL} = 0.3 x V_{DD} and V_{IH} = 0.7 x V_{DD}. All inputs include Schmitt trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5380/MAX5381/MAX5382 without additional external logic. The digital inputs are compatible with CMOS logic levels and must not be driven with voltages higher than V_{DD}.

Power-Supply Bypassing and Layout

Careful printed circuit board layout is important for best system performance. To reduce crosstalk and noise injection, keep analog and digital signals separate. Ensure that the ground return from GND to the supply ground is short and low impedance; a ground plane is recommended. Bypass V_{DD} with a 0.1µF capacitor to ground as close as possible to the device. If the supply is excessively noisy, connect a 10Ω resistor in series with the supply and V_{DD} and add additional capacitance.

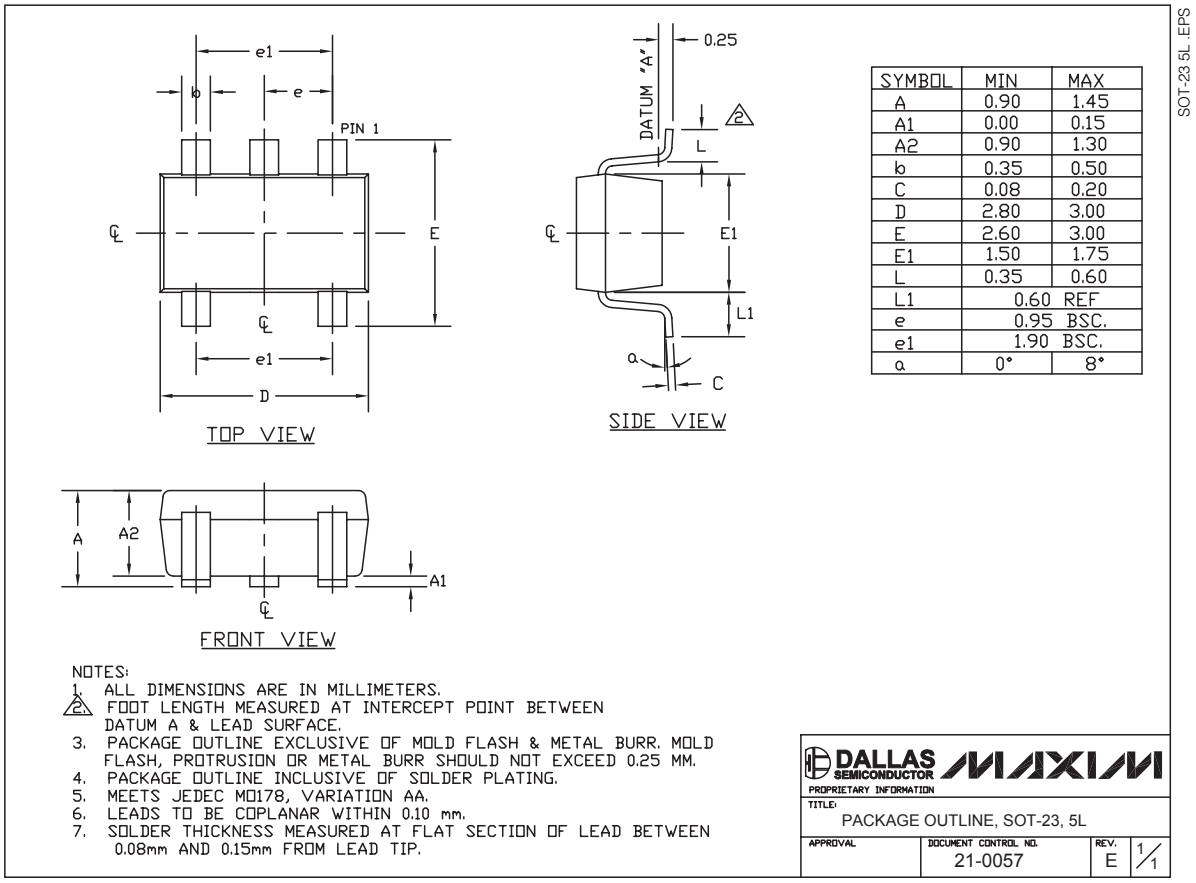
Chip Information

TRANSISTOR COUNT: 2910

Low-Cost, Low-Power, 8-Bit DACs with 2-Wire Serial Interface in SOT23

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF	
e	0.95 BSC.	
e1	1.90 BSC.	
α	0°	8°

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