Temperature Sensor and System Monitor in a 10-Pin µMAX

ABSOLUTE MAXIMUM RATINGS

All Voltages Are Referenced to GND

V_{CC} .....-0.3V to +6.0V
Voltage on $12V_{IN}$ .....-0.3V to +16V
All Other Pins .....-0.3V to +6.0V
Output Current (SDA, $\overline{ALERT}$) .....-1mA to +50mA
Junction Temperature .....+150°C

Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{CC}			2.7		5.5	V
Supply Current	I_{CC}	Active			200	500	µA
	I_{SD}	Shutdown mode, all digital inputs are grounded			<1	10	µA
Power-On Reset Voltage		$V_{CC\_}$ rising or falling edge			2		V
TEMPERATURE							
Accuracy (Note 5)		V_{CC} = +5V	T_A = +25°C			±2	°C
			-20°C ≤ T_A ≤ +80°C			±3	
			-40°C ≤ T_A ≤ +125°C			±5	
PSRR		V_{CC} = +2.7V to +5.5V			0.7	1.3	°C/V
Resolution					±1		°C
ADC CHARACTERISTICS							
Total Unadjusted Error	TUE	V_{IN} > 10LSB			±1	±1.5	%
Differential Nonlinearity	DNL	V_{IN} > 10LSB				±1	LSB
Supply Sensitivity	PSS	V_{CC} = +2.7V to +5.5V			±1		V
Input Resistance	R_{IN}	$12V_{IN}$, $2.5V_{IN}$, $3.3V_{IN}$		100	150	200	kΩ
Total Monitoring Cycle Time	tc	(Note 1)			200	300	ms
SCL, SDA, ADD							
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input High Voltage	V_{IH}	V_{CC} ≤ 3.6V		2.0			V
		V_{CC} > 3.6V		2.6			V
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA				400	mV
Input Leakage Current	I_{LEAK}	V_{IN} = 0 or 5V				±1	µA
$\overline{ALERT}$							
Output Low Voltage	V_{OLA}	I_{SINK} = 1.2mA, V_{CC} > 2.7V				0.3	V
		I_{SINK} = 3.2mA, V_{CC} > 4.5V				0.4	V
TIMING							
Serial Clock Frequency	f_{SCL}			0		400	kHz
Bus Free Time Between STOP and START	t_{BUF}			1.3			µs

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Hold Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SP:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	(Note 2)	0		0.9	µs
Receive SCL/SDA Minimum Rise Time	t_R	(Note 3)		20 + 0.1C_B		ns
Receive SCL/SDA Maximum Rise Time	t_R	(Note 3)		300		ns
Receive SCL/SDA Minimum Fall Time	t_F	(Note 3)		20 + 0.1C_B		ns
Receive SCL/SDA Maximum Fall Time	t_F	(Note 3)		300		ns
Transmit SDA Fall Time	t_F	400pF, I_{SINK} = 3mA	20 + 0.1C_B		300	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 4)		50		ns

Note 1: Total monitoring time includes temperature conversion and four analog input voltage conversions.

Note 2: A master device must provide at least a 300ns hold time for the SDA signal, referred to V_{IL} of the SCL signal, to bridge the undefined region of SCL's falling edge.

Note 3: C_B = total capacitance of one bus line in pF. Rise and fall times are measured between 0.3 x V_{CC} to 0.7 x V_{CC}.

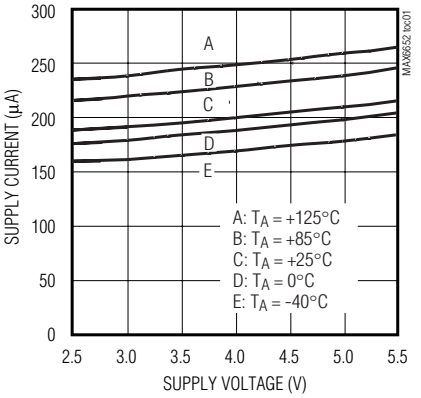
Note 4: Input filters on SDA, SCL, and ADD suppress noise spikes <50ns.

Note 5: Guaranteed but not tested over the entire temperature range.

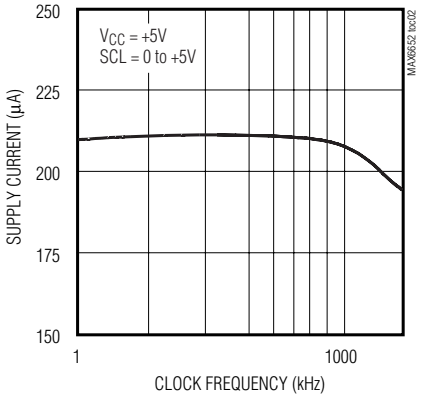
Typical Operating Characteristics

(V_{CC} = +5V, ADD = GND, $\overline{ALERT}$ = 10kΩ to V_{CC}, T_A = +25°C, unless otherwise noted.)

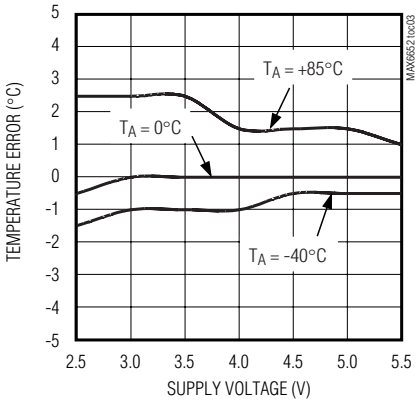
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SCL CLOCK FREQUENCY



TEMPERATURE ERROR vs. SUPPLY VOLTAGE



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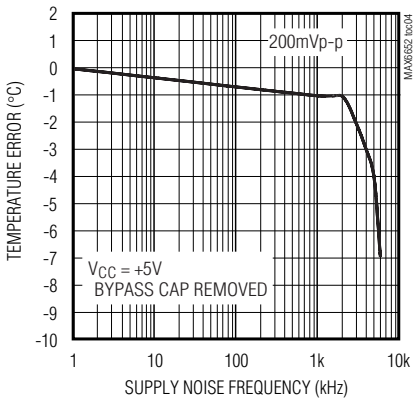
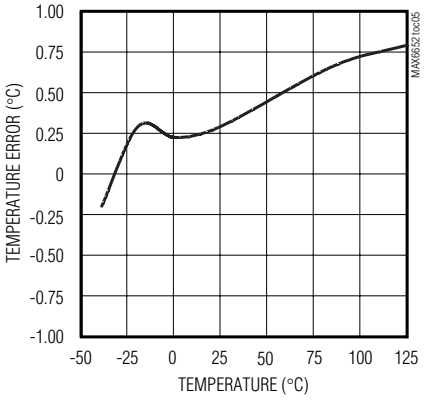
Typical Operating Characteristics (continued)

(V_{CC} = +5V, ADD = GND, $\overline{ALERT}$ = 10kΩ to V_{CC}, T_A = +25°C, unless otherwise noted.)

TEMPERATURE ERROR vs. SUPPLY NOISE FREQUENCY



TEMPERATURE ERROR vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	$12V_{IN}$	Analog Input. Monitors 12V supply.
2	$2.5V_{IN}$	Analog Input. Monitors 2.5V supply.
3	$3.3V_{IN}$	Analog Input. Monitors 3.3V supply.
4	N.C.	No Connection. Can be connected to GND to improve thermal conductivity.
5	GND	Ground
6	$\overline{ALERT}$	SMBus Alert (Interrupt) Output, Open Drain. Alerts the master that a temperature or voltage limit has been violated.
7	ADD	SMBus Address Select Input. ADD is sampled at the beginning of each I^2C-compatible/SMBus transaction, and the 2 LSBs of the slave address register are detemined by ADD's connection to GND, SDA, SCL, or V_{CC}.
8	SDA	I^2C-Compatible/SMBus Serial Data Interface
9	SCL	I^2C-Compatible/SMBus Serial Clock Input
10	V_{CC}	Supply Voltage Input, +2.7V to +5.5V. Also serves as a voltage monitor input. Bypass V_{CC} to GND with a 0.1µF capacitor.

Detailed Description

The MAX6652 is a voltage and temperature monitor designed to communicate through an I^2C-compatible/SMBus interface with an external microcontroller (µC). A µC with no built-in I^2C-compatible or SMBus capabilities can generate SMBus serial commands by "bit-banging" general-purpose input-output (GPIO) pins.

The MAX6652 can monitor external supply voltages of typically 2.5V, 3.3V, and 12V, as well as its own supply voltage and temperature. This makes it ideal for supervisor and thermal management applications in telecommunications, desktop and notebook computers, workstations, and networking equipment. All inputs are converted to an 8-bit code using an ADC with an oversampling ratio of 8 to improve noise rejection. The oversampling ratio can be reduced by a factor of 4, with a corresponding reduction in the monitoring cycle time, by setting bit 5 of the configuration register to 1. Each input voltage is scaled down by an on-chip resistive divider so that its output, at the nominal input voltage, is 3/4 of the ADC's full-scale range, or a decimal count of 192 (Table 3). Table 1 is the register map and Table 2 is the temperature data format.

Table 1. Register Map

ADDRESS	READ/WRITE	POWER-ON DEFAULT	DESCRIPTION
20h	R	—	Data register for 2.5 V_{IN} measurement
21h	R	—	Data register for $12V_{IN}$ measurement
22h	R	—	Data register for $3.3V_{IN}$ measurement
23h	R	—	Data register for V_{CC} measurement
27h	R	—	Data register for temperature measurement
2Bh	R/W	1101 0011 (1.1 × 2.5V)	High limit for $2.5V_{IN}$
2Ch	R/W	1010 1101 (0.9 × 2.5V)	Low limit for $2.5V_{IN}$
2Dh	R/W	1101 0011 (1.1 × 12V)	High limit for $12V_{IN}$
2Eh	R/W	1010 1101 (0.9 × 12V)	Low limit for $12V_{IN}$
2Fh	R/W	1101 0011 (1.1 × 3.3V)	High limit for $3.3V_{IN}$
30h	R/W	1010 1101 (0.9 × 3.3V)	Low limit for $3.3V_{IN}$
31h	R/W	1101 0011 (1.1 × 5V)	High limit for V_{CC}
32h	R/W	1010 1101 × (0.9 × 5V)	Low limit for V_{CC}
39h	R/W	0101 0000 × (+80°C)	Hot temperature limit
3Ah	R/W	0100 0001 × (+65°C)	Hot temperature hysteresis
40h	R/W	0000 1000	Configuration register
41h	R	0000 0000	Interrupt status register
43h	R/W	0000 0000	Interrupt mask register
48h	R/W	0010 1XXY	Device address register. The values of XX are dependent on the status of the ADD pin. **Power-On Default** — **ADD Connection** 0010 100Y — To GND 0010 101Y — To V_{CC} 0010 110Y — To SDA 0010 111Y — To SCL Y (bit 0) is the SMBus read/write bit. When the 7-bit chip address is read back from the serial address register, an 8-bit word will be presented with a 0 in bit 0 (Y).
4Bh	R/W	0000 0000	Temperature configuration register

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Table 2. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0111 1101	7D
+25	0001 1001	19
+1	0000 0001	01
0	0000 0000	00
-1	1111 1111	FF
-25	1110 0111	E7
-40	1101 1000	D8

Writing a 1 to bit 0 of the configuration register starts the monitoring function. The device will perform a sequential sampling of all the inputs, starting with the internal temperature sensor and continuing with $2.5V_{IN}$, $12V_{IN}$, $3.3V_{IN}$, and V_{CC}. If the master terminates the conversion, the sequential sampling will not stop until the sampling cycle is completed and the results are stored. When it starts again, it will always start with the temperature measurement.

An interrupt signal is generated when a temperature measurement goes above the hot limit or when a voltage measurement is either above the high limit or below the low limit. This will cause the open-drain output ($\overline{ALERT}$) to go to the active-low state and set each corresponding interrupt status bit (bits 0 through 4) to 1 (Table 5). The interrupt will be cleared by reading the interrupt status register, except for temperature interrupts generated in comparator mode. Reading the interrupt status register also clears the register itself, except for temperature interrupt bits set in comparator mode.

Unless the fault is removed, the $\overline{ALERT}$ output will only remain cleared until the end of the next conversion cycle where it will again be asserted. The $\overline{ALERT}$ output can also be masked by writing to the appropriate bits in the interrupt mask register (Table 6) or by setting bit 1 of the configuration register (Table 4) to 0.

ADC and Multiplexer

The ADC integrates over a 66ms period, an integral multiple of the line period with excellent noise rejection. The internal oscillator is trimmed to produce a 66ms conversion time for temperature and 33ms for each voltage. This is equivalent to 4 and 2 cycles of 60Hz, respectively, and provides protection against noise pickup from the main supply. The internal oscillation frequency can be changed to provide the same protection against 50Hz by setting bit 7 in the configuration register to 1 (Table 4). The multiplexer automatically sequences through the inputs, measuring voltages, and temperature.

Table 3. Voltage Data Format

ADC OUTPUT CODE	INPUT VOLTAGE AT $12V_{IN}$	INPUT VOLTAGE AT $2.5V_{IN}$	INPUT VOLTAGE AT $3.3V_{IN}$	V_{CC}
LSB weight	62mV (12V/192)	13mV (2.5V/192)	17.2mV (3.3V/192)	26mV (5.0V/192)
0	< 62mV	< 13mV	< 17.2mV	—
1	62mV - 125mV	13mV - 26mV	17.2mV - 34.4mV	—
2	125mV - 187mV	26mV - 39mV	34.4mV - 51.6mV	—
—	—	—	—	—
64 (1/4 scale)	4.000V - 4.063V	833mV - 846mV	1.100V - 1.117V	—
—	—	—	—	—
128 (1/2 scale)	8.000V - 8.063V	1.667V - 1.680V	2.200V - 2.217V	3.330V - 3.560V
—	—	—	—	—
192 (3/4 scale)	12.000V - 12.063V	2.500V - 2.513V	3.300V - 3.317V	5.000V - 5.026V
—	—	—	—	—
253	15.813V - 15.875V	3.294V - 3.307V	4.348V - 4.366V	6.566V - 6.615V
254	15.875V - 15.938V	3.572V - 3.586V	4.366V - 4.383V	6.615V - 6.640V
255	> 15.938	> 3.586	> 4.383	> 6.640

Table 4. Configuration Register (Address 41h, Power-Up Default = 00h)

BIT	NAME	READ/WRITE	DESCRIPTION
0	Start/Stop	R/W	This bit controls the monitoring loop. Setting the bit to 0 stops the monitoring loop and puts the device into shutdown mode. The I^2C/SMBus interface is still active during the shutdown mode. Setting the bit to 1 starts the monitoring cycle. All high/low limits should be set before setting this bit to 1.
1	Interrupt Enable	R/W	This bit is used to enable or disable the interrupt output. Setting the bit to 1 enabes the interrupt output; setting the bit to 0 disables the interrupt output.
2	Reserved	—	—
3	Interrupt Clear	R/W	This bit is used to clear the interrupt output when it is set to high. It will not affect the interrupt status register. The monitoring loop will not start until the bit is set to 0.
4	Line Frequency Select	R/W	This bit controls the internal clock frequency. Setting the bit to 1 changes the clock frequency to 51.2kHz from 61.4kHz. This can improve the measurement accuracy when the power-line frequency is at 50Hz.
5	Short Cycle	R/W	This bit reduces the conversion rate by a factor of four when it is set to 1.
6	Reserved	—	—
7	Reset	R/W	This bit is used as a reset signal for the register initialization. The 1 of this bit will reset all the register values into the power-up default mode, including bit 7 itself.

Table 5. Interrupt Status Register (Address 41h, Power-Up Default = 00h)

BIT	NAME	READ/WRITE	DESCRIPTION
0	$2.5V_{IN}$ Error	R	A 1 indicates either a high or low limit has been exceeded at the $2.5V_{IN}$ input.
1	$12V_{IN}$ Error	R	A 1 indicates either a high or low limit has been exceeded at the $12V_{IN}$ input.
2	$3.3V_{IN}$ Error	R	A 1 indicates either a high or low limit has been exceeded at the $3.3V_{IN}$ input.
3	V_{CC} Error	R	A 1 indicates either a high or low limit has been exceeded at the V_{CC} input.
4	Temperature Error	R	A 1 indicates either a high or low limit has been exceeded at the internal temperature sensor. The conditions that will generate and clear this bit depend on the temperature interrupt mode selected by bits 0 and 1 in the temperature configuration register.
5, 6, 7	Reserved	—	—

Table 6. Interrupt Mask Register (Address 43h, Power-Up Default = 00h)

BIT	NAME	READ/WRITE	DESCRIPTION
0	2.5V	R/W	Setting the bit to 1 disables the interrupt status register bit (bit 0) and the $\overline{ALERT}$ output for the $2.5V_{IN}$ input.
1	12V	R/W	Setting the bit to 1 disables the interrupt status register bit (bit 1) and the $\overline{ALERT}$ output for the $12V_{IN}$ input.
2	3.3V	R/W	Setting the bit to 1 disables the interrupt status register bit (bit 2) and the $\overline{ALERT}$ output for the $3.3V_{IN}$ input.
3	5.0V	R/W	Setting the bit to 1 disables the interrupt status register bit (bit 3) and the $\overline{ALERT}$ output for the V_{CC} input.
4	Temperature	R/W	Setting the bit to 1 disables the interrupt status register bit (bit 4) and the $\overline{ALERT}$ output for temperature.
5, 6, 7	Reserved	—	—

Low-Power Shutdown Mode

Setting bit 0 in the configuration register to 0 stops the monitoring loop and puts the MAX6652 into low-power shutdown mode. In this mode, the I^2C-compatible/SMBus interface remains active, and the supply current drops to 10µA or less.

Power-On Reset (POR)

The MAX6652 power-on reset supply (POR) voltage is typically 2V. Below this supply voltage, all registers are reset, the device is put into shutdown mode, and the I^2C-compatible/SMBus interface is inactive.

Alarm Threshold Registers

Two registers, a hot temperature limit (T_{HOT}) at 39h and a hot temperature hysteresis (T_{HYST}) at 3Ah, store alarm threshold data (Table 1). If a measured temperature exceeds the value of T_{HOT}, an $\overline{ALERT}$ is asserted. Alerts are cleared and reasserted depending on the interrupt mode selected in the temperature configuration register (see *$\overline{ALERT}$ Interrupts*).

The POR state of the T_{HOT} register is 0101 0000 or +80°C. The POR state of the T_{HYST} register is 0100 0001 or +65°C.

High and low limits for the voltage inputs are stored in registers 2Bh through 32h. If a measured voltage is less than V_{LOW} or greater than V_{HIGH}, an $\overline{ALERT}$ is asserted.

The POR states of the high- and low-voltage limits are 1.1 and 0.9 times the nominal voltage for each input, respectively.

Interrupt Status Byte Functions

The interrupt status register records temperature or voltage fault conditions whenever a limit is exceeded (Table 5). Bits 0 through 3 correspond to the 2.5V, 12V, 3.3V, and 5V internal V_{CC} voltage inputs, and bit 4 corresponds to the temperature. If a threshold has been crossed, the appropriate bit will contain a 1. In the default and one-time interrupt modes, reading the status register clears the register until a new out-of-range condition is detected.

$\overline{ALERT}$ Interrupts

An out-of-range voltage or temperature causes the $\overline{ALERT}$ output signal to be asserted. However, if the assertion is caused by an out-of-range temperature, the $\overline{ALERT}$ output can operate in one of three different modes: default, one-time interrupt, and comparator modes. The $\overline{ALERT}$ signal can be cleared only by reading the interrupt status register (Table 5), except when the $\overline{ALERT}$ has been activated by an out-of-range temperature in comparator mode. In this case, $\overline{ALERT}$ is only cleared when the fault is removed. Reading the interrupt status register also clears this register, except for bit 4 in comparator mode. Unless the fault is removed, $\overline{ALERT}$ will be reasserted after the next conversion cycle. The $\overline{ALERT}$ output can also be masked by writing to the appropriate bits in the interrupt mask register (Table 6) or by setting bit 1 of the configuration register (Table 4) to 0.

The interrupt does not halt conversions. New temperature and voltage data continue to be available over the I^2C-compatible/SMBus interface after $\overline{ALERT}$ is asserted. The three temperature $\overline{ALERT}$ modes are illustrated in Figure 1 and are selected through the temperature configuration register (Table 7). The $\overline{ALERT}$ output pin is open drain, so the device can share a common interrupt line.

Default Mode

An interrupt is initiated when temperature exceeds T_{HOT} (address 39Ah). The interrupt is cleared only by reading the interrupt status register. An interrupt will continue to be generated on subsequent measurements until temperature goes below T_{HYST} (address 3Ah).

One-Time Interrupt Mode

An interrupt is initiated when temperature exceeds T_{HOT} (address 39Ah). The interrupt is cleared only by reading the interrupt status register. The next interrupt is then initiated when temperature falls below the T_{HYST} (address 3Ah).

Comparator Mode

An interrupt is initiated when temperature exceeds T_{HOT} (address 39Ah). The $\overline{ALERT}$ output will remain asserted low until the temperature goes below T_{HOT}. Reading the interrupt status register will not clear the $\overline{ALERT}$ output or interrupt status bit in the register. The interrupt will continue to be generated on subsequent measurements until temperature falls below T_{HOT}.

Figure 1 shows successive interrupts and clears using a temperature fault as an example.

I²C-Compatible/SMBus Digital Interface

From a software perspective, the MAX6652 appears as a set of byte-wide registers that contain voltage and temperature data, alarm threshold values, or control bits.

The device employs four standard I²C-compatible/SMBus protocols: write byte, read byte, send byte, and receive byte (Figures 2, 3, 4).

Slave Address

The device address can be set to one of four different values by pin strapping ADD to GND, SDA, SCL, or V_{CC}, so more than one MAX6652 can reside on the same bus without address conflicts (Table 1). The address pin state is checked at the beginning of each I²C-compatible/SMBus transaction and so is insensitive to glitches on V_{CC}. Any address code can also be written to the serial address register and will overwrite the code set by connecting the ADD pin until the MAX6652 is taken through a POR cycle.

The MAX6652 also responds to the SMBus alert response address (see *Alert Response Address*).

Alert Response Address

The SMBus alert response interrupt pointer provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. Usually the $\overline{ALERT}$ outputs of several slave devices are wired-ORed to the same interrupt input of the host master. Upon receiving an interrupt signal, the host master can broadcast a receive byte transmission (Figure 2) with the alert response address (0001 1000). Then, any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus.

The alert response can activate several different slave devices simultaneously, similar to the I²C general call. If more than one slave attempts to respond, bus arbitration rules apply, and the device with the lower address code wins. The losing device does not generate an acknowledge signal and continues to hold the interrupt line low until serviced. The MAX6652 does not automatically clear its $\overline{ALERT}$ when it responds to an alert response address. The host master must then clear or mask the $\overline{ALERT}$ by reading the interrupt status register, writing to the interrupt mask register, or setting bit 1 of the configuration register to 0 before it can identify other slaves generating an interrupt.

Command Byte Functions

The 8-bit command byte register (Table 1) is the master index that points to the other data, configuration, limits, and address registers within the MAX6652. The functions of those other registers are described below.

Configuration Byte Functions

The configuration register (Table 4) is a read-write register with several functions:

Bit 0 puts the MAX6652 into software standby mode (STOP) or autoconvert (START) mode. The 2-wire interface is still active in the standby mode. All voltage and temperature limits should be set before setting this bit to 1.

Bit 1 enables and disables the $\overline{ALERT}$ output. Setting this bit to 1 enables the $\overline{ALERT}$ output.

Bit 2 is reserved.

Bit 3 clears the $\overline{ALERT}$ output and stops the monitoring loop when set to 1. Clearing the output will not affect the contents of the interrupt status registers.

Bit 4 sets the analog-to-digital conversion speed to minimize interference from power-line frequencies. Setting this bit to 1 can improve accuracy when the power-line frequency is 50Hz. When the power-line frequency is 60Hz, bit 4 should be 0.

Bit 5 reduces the oversampling ratio in the ADC from 8 to 2. This reduces the monitoring cycle time by a factor of 4 to typically 50ms at the cost of reduced noise rejection.

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Table 7. Temperature Configuration Register

BIT	NAME	R/W	DESCRIPTION
0-1	Hot Temperature Interrupt Mode Select	R/W	Bit 1, Bit 0 → 00: Default Mode Bit 1, Bit 0 → 01: One-Time Interrupt Mode Bit 1, Bit 0 → 10: Comparator Mode Bit 1, Bit 0 → 11: Default Mode
2-7	Reserved	R/W	—

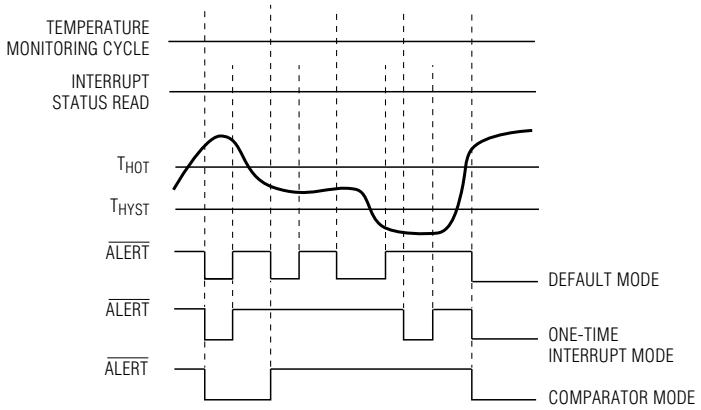


Figure 1. Alert Response to Temperature Interrupts

Bit 6 is reserved.**Bit 7** resets all register values to their power-up default values. To reset all registers, set bit 7 to 1. This will also reset bit 7 to its power-up value of 0.

Applications Information

Sensing Circuit Board and Component Temperatures

Temperature sensor ICs like the MAX6652 that sense their own die temperatures must be mounted on or close to the object whose temperature they are intended to measure. Because there is a good thermal path between the 10-pin µMAX package's metal leads and the IC die, the MAX6652 can accurately measure the temperature of the circuit board to which it is soldered. If the sensor is intended to measure the temperature of a heat-generating component on the circuit board, it should be mounted as close as possible to that component and should share supply and ground traces (if they are not noisy) with that component where possible. This will maximize the heat transfer from the component to the sensor.

The thermal path between the plastic package and the die is not as good as the path through the leads, so the MAX6652, like all temperature sensors in plastic packages, will be less sensitive to the temperature of the surrounding air than to the temperature of the leads.

As with any IC, the wiring and circuits must be kept insulated and dry to avoid leakage and corrosion, especially if the part will be operated at cold temperatures where condensation can occur.

Chip Information

TRANSISTOR COUNT: 13,446

PROCESS: BiCMOS

Write Byte Format

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	P
	7 bits			8 bits		8 bits		

Slave Address: equivalent to chip-select line of a 3-wire interface

Command Byte: selects which register you are writing to

Data Byte: data goes into the register set by the command byte (to set thresholds, configuration masks, and sampling rate)

Read Byte Format

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	$\overline{A}$	P
	7 bits			8 bits			7 bits			8 bits		

Slave Address: equivalent to chip-select line

Command Byte: selects which register you are reading from

Slave Address: repeated due to change in data-flow direction

Data Byte: reads from the register set by the command byte

Send Byte Format

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	P
	7 bits			8 bits		

Data Byte: writes data to the register commanded by the last read byte or write byte transmission

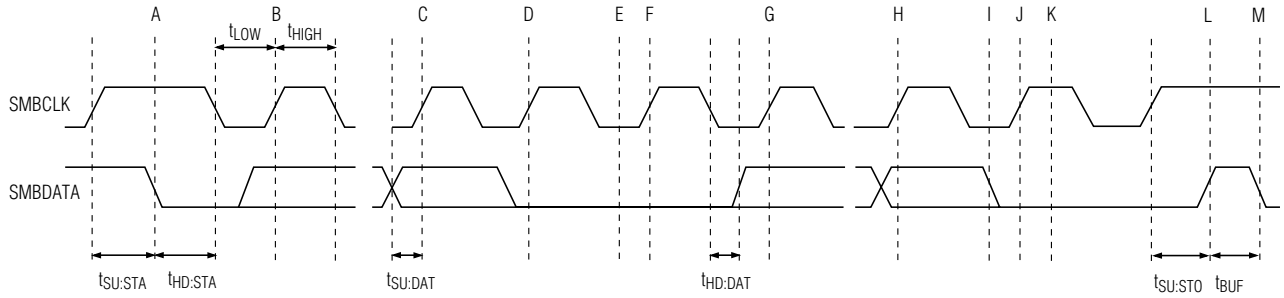
Receive Byte Format

S	ADDRESS	RD	ACK	DATA	$\overline{A}$	P
	7 bits			8 bits		

Data Byte: reads data from the register commanded by the last read byte or write byte transmission; also used for SMBus alert response return address

S = Start condition *Shaded = Slave transmission*
P = Stop condition *$\overline{A}$ = Not acknowledged*

Figure 2. I²C/SMBus Protocols



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/$\overline{W}$ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE
H = LSB OF DATA CLOCKED INTO SLAVE
I = MASTER PULLS DATA LINE LOW
J = ACKNOWLEDGE CLOCKED INTO SLAVE
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION
M = NEW START CONDITION

Figure 3. I²C/SMBus Write Timing Diagram

Temperature Sensor and System Monitor in a 10-Pin µMAX

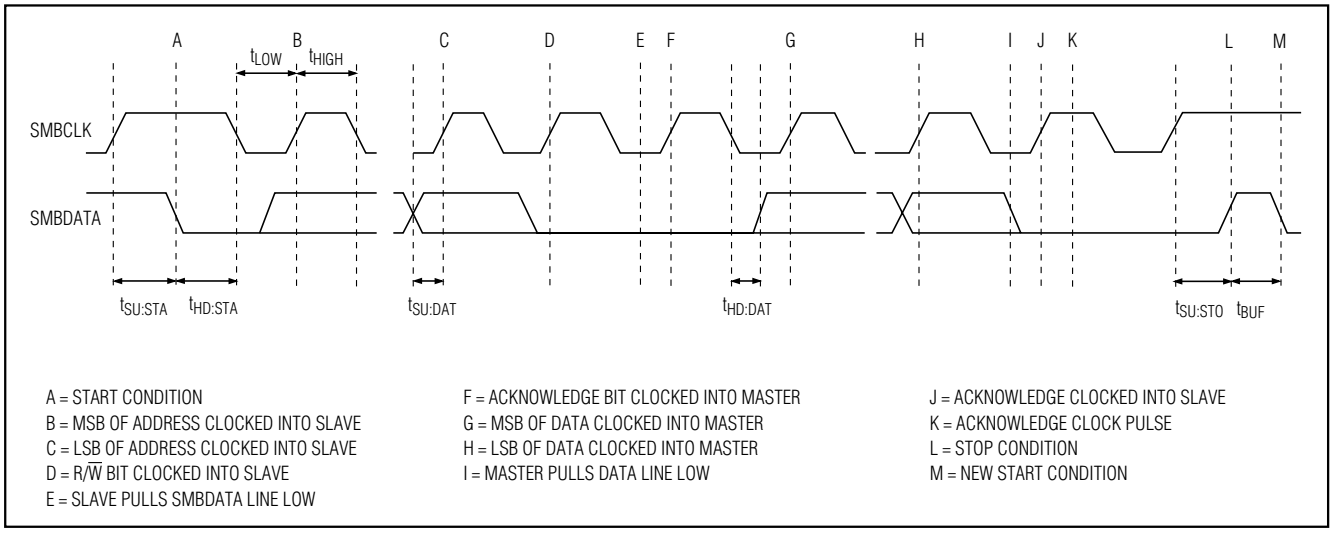
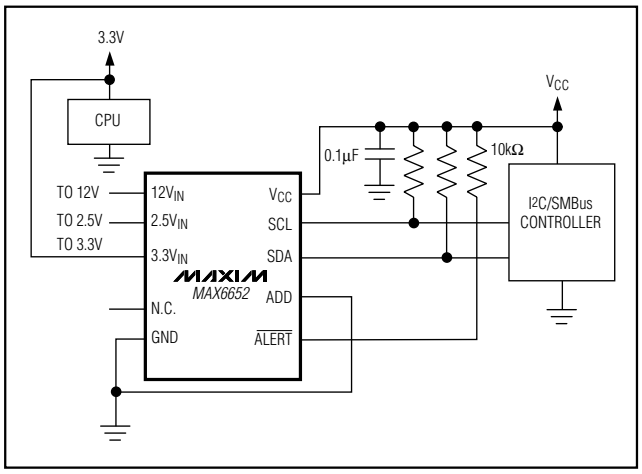
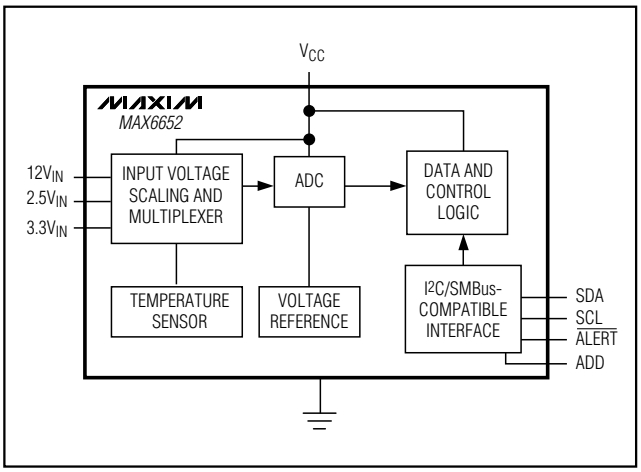


Figure 4. I²C/SMBus Read Timing Diagram

Typical Application Circuit



Functional Diagram



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