Standard Definition Video Reconstruction Filters and Buffers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....+6V
All Other Pins to GND.....-0.3V to (V_{CC} + 0.3V)
Maximum Current Into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 9.71mW/°C above +70°C).....777mW
10-Pin µMAX (derate 6.94mW/°C above +70°C) 555.5mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, R_{REXT} = 300kΩ ±1%, C_{IN} = 0.1µF, C_{REXT} = (1nF to 1µF) ±1%, C_{LOAD} = 0 to 20pF; BOOST0_, BOOST1_ = 0, 0; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Passband Response		f = 100kHz to 4.2MHz relative to 100kHz	-0.5		+0.5	dB
		f = 100kHz to 5MHz relative to 100kHz	-1.0		+1.0	
Stopband Attenuation	A_{sb}	f ≥ 27MHz	48			dB
HF Boost Relative Step Size, 4 Levels		f = 4.2MHz to 5MHz	0.2	0.4	0.6	dB
Differential Gain	dG	5-step modulated staircase		0.2		%
Differential Phase	dθ	5-step modulated staircase		0.2		degrees
Harmonic Distortion	THD	f = 100kHz to 5MHz		0.1	0.5	%
Signal-to-Noise Ratio	SNR	Peak signal (2Vp-p) to RMS noise, f = 100Hz to 50MHz	72			dB
Group Delay Deviation	Δt_g	Deviation from 100kHz to 3.58 (4.43)MHz			20	ns
Line-Time Distortion	H_{dist}	18µs, 100 IRE bar			0.3	%
Field-Time Distortion	V_{dist}	130 lines, 18µs, 100 IRE bar			0.5	%
Clamp Settling Time	t_{clamp}	to ±1% (Note 1)			100	Lines
Output DC Clamp Level		CLEVEL = 0	0.8		1.3	V
		CLEVEL = 1	1.35		1.85	
Low-Frequency Gain	A_V	Gain at 100kHz	1.9	1.975	2.05	V/V
Group Delay Matching	$t_{g(MATCH)}$	Low frequency channel-to-channel matching f = 100kHz		2		ns
Low-Frequency Gain Matching	$A_{V(MATCH)}$	Channel-to-channel gain matching, f = 100kHz			5	%
Channel-to-Channel Crosstalk	X_{TALK}	Channel-to-channel crosstalk, f = 100kHz to 5.5MHz		-60		dB
Output Short-Circuit Current	I_{SC}	OUT_ shorted to ground or V_{CC}		50		mA
Input Leakage Current	I_{IN}				10	µA
Input Dynamic Swing	Y_{INp-p}	CLEVEL = 0		1.4		Vp-p
	C_{INp-p}	CLEVEL = 1		0.9		
V_{CC} Supply Range	V_{CC}		4.5		5.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, R_{REXT} = 300kΩ ±1%, C_{IN} = 0.1µF, C_{REXT} = (1nF to 1µF) ±1%, C_{LOAD} = 0 to 20pF; BOOST0_, BOOST1_ = 0, 0; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	No load	MAX7428		24	32	mA
			MAX7430		45	62	
			MAX7432A		68	86	
Power-Supply Rejection Ratio	PSRR	V_{IN} = 100mVp-p, f = 0 to 5.5MHz			40		dB
IN_A/IN_B Crosstalk		V_{IN} = 100mVp-p, f = 100kHz to 5.5MHz			-60		dB
LOGIC CHARACTERISTICS							
Logic Input High Voltage	V_{IH}			2			V
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input Current	I_{IH}/I_{IL}	V_{IL} = 0 (source), V_{IH} = V_{CC} (sink)				10	µA
Logic Output High Voltage	V_{OH}	$I_{(SOURCE)}$ = 500µA		V_{CC} - 0.5			V
Logic Output Low Voltage	V_{OL}	$I_{(SINK)}$ = 500µA				0.4	V

MSPB INTERFACE TIMING SPECIFICATIONS

(V_{CC} = +5V ±10%, R_{REXT} = 300kΩ ±1%, C_{REXT} = (1nF to 1µF) ±1%, C_{LOAD} = 0 to 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figures 4 through 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MSPB TIMING						
Logic-Zero/Prompt Pulse Width	t_0, t_P		1	5	8	µs
Logic-One Pulse Width	t_1		24	30	36	µs
Transaction Pulse Width	t_T		80	100	120	µs
Separation Between Pulses	t_{WAIT}		0.5			µs
Bus Release Time by Host After Prompt Pulse	$t_{RELEASE}$				1	µs
Bus Reclaim Time by Host After Prompt Pulse	$t_{RECLAIM}$		13			µs
Read Back Data Valid Window After the Prompt Pulse	t_{READ}		2.3		4.7	µs

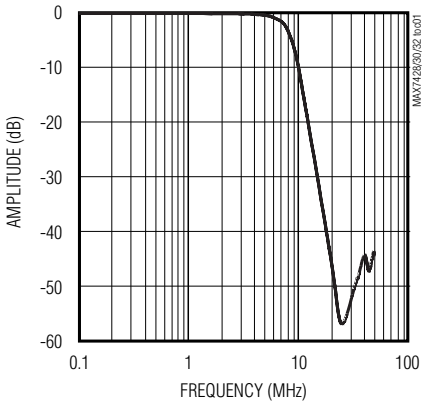
Note 1: One horizontal line = 63.5µs.
Note 2: MAX7428 devices are 100% production tested at T_A = +25°C and are guaranteed by design from T_A = T_{MIN} to T_{MAX}.

Standard Definition Video Reconstruction Filters and Buffers

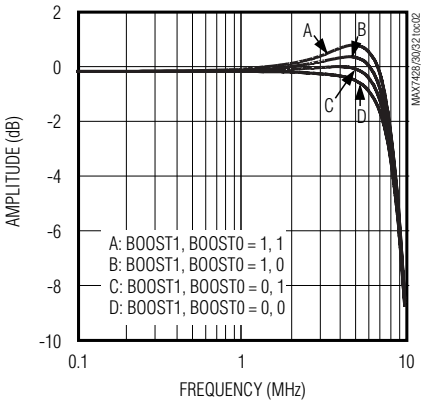
Typical Operating Characteristics

(V_{CC} = +5V, R_{REXT} = 300kΩ; BOOST0_, BOOST1_ = 0, 0; $V_{IN\_}$ = 1Vp-p, T_A = +25°C, unless otherwise noted.)

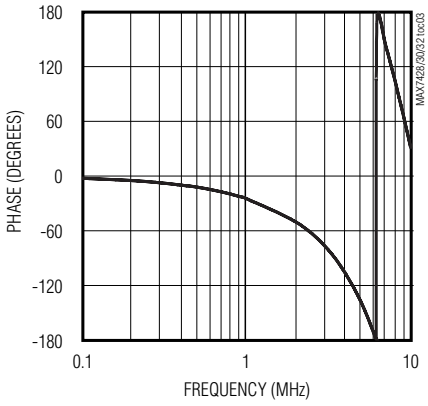
AMPLITUDE vs. FREQUENCY



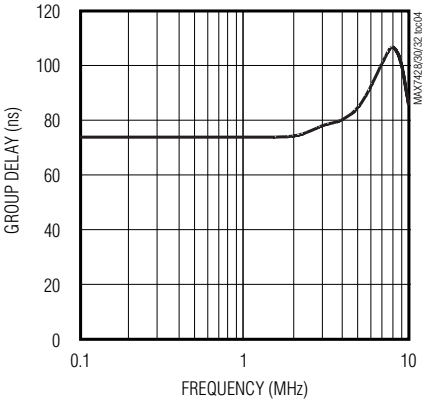
PASSBAND AMPLITUDE vs. FREQUENCY



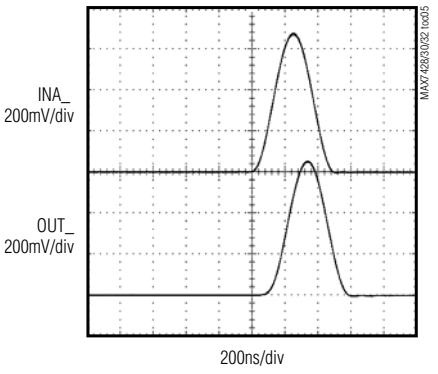
PHASE RESPONSE vs. FREQUENCY



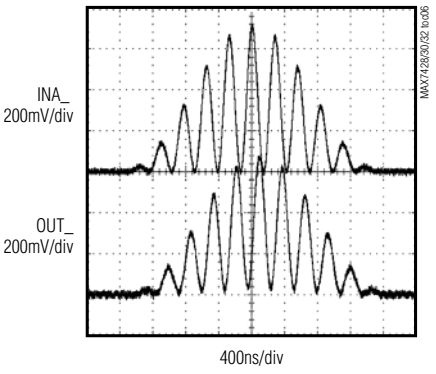
GROUP DELAY vs. FREQUENCY



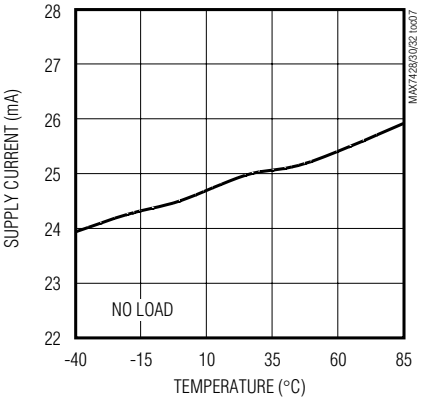
2T RESPONSE (1IRE = 7.14mV)



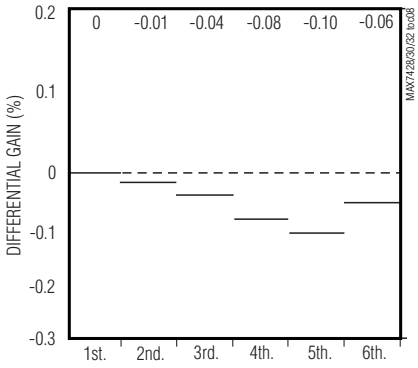
MODULATED 12.5T RESPONSE (1IRE = 7.14mV)



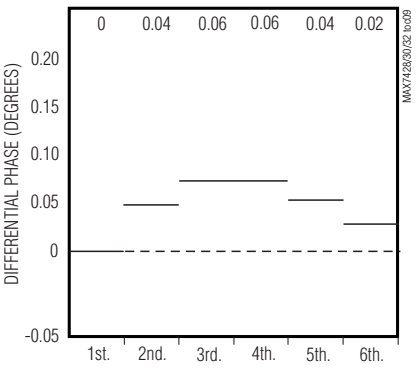
SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL GAIN



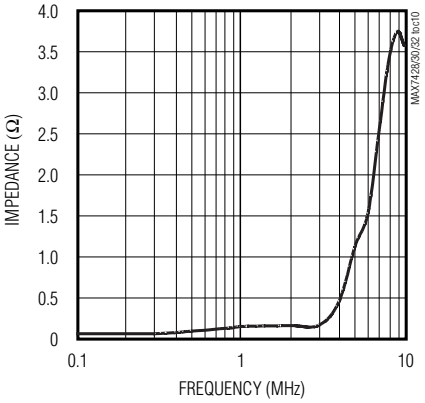
DIFFERENTIAL PHASE



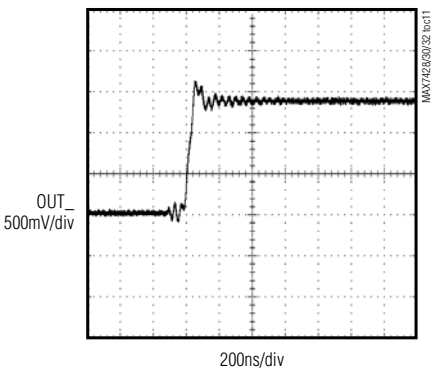
Typical Operating Characteristics (continued)

(V_{CC} = +5V, R_{REXT} = 300kΩ; BOOST0_, BOOST1_ = 0, 0; V_{IN} = 1Vp-p, T_A = +25°C, unless otherwise noted.)

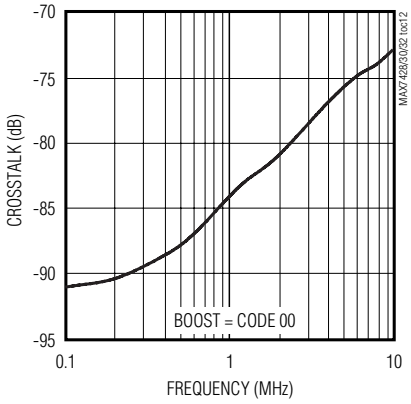
OUTPUT IMPEDANCE vs. FREQUENCY



OUTPUT TRANSIENT DUE TO INPUT MUX SWITCHING



PASSBAND CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



Pin Description

PIN			NAME	FUNCTION
MAX7432A	MAX7430	MAX7428		
1	1	—	IN1A	Video Input 1A. Master channel, sync signal required. Use a 0.1µF series input capacitor for proper operation.
2	2	—	IN2A	Video Input 2A. Slave channel, clamping controlled by master channel sync. Use a 0.1µF series input capacitor for proper operation.
3	—	—	IN3A	Video Input 3A. Slave channel, clamping controlled by master channel sync. Use a 0.1µF series input capacitor for proper operation.
4, 10	8	4	GND	Ground
5	4	—	IN1B	Video Input 1B. Master channel, sync signal required. Use a 0.1µF series input capacitor for proper operation.
6	5	—	IN2B	Video Input 2B. Slave channel, clamping controlled by master channel sync. Use a 0.1µF series input capacitor for proper operation.
7	—	—	IN3B	Video Input 3B. Slave channel, clamping controlled by master channel sync. Use a 0.1µF series input capacitor for proper operation.
8	6	6	DATA	Serial Data Interface
9	—	—	OUT3	Buffer Output 3
11	7	—	OUT2	Buffer Output 2
12	3	7	REXT	External Resistor. Connect a 300kΩ resistor from REXT to GND for internal biasing. Connect a 1nF to 1µF capacitor from REXT to GND for chip-address programming (see Table 3).

Standard Definition Video Reconstruction Filters and Buffers

Pin Description (continued)

PIN			NAME	FUNCTION
MAX7432A	MAX7430	MAX7428		
13	9	—	OUT1	Buffer Output 1
14	10	2	V_{CC}	+5V Supply Voltage
—	—	1	INA	Video Input A. Use a 0.1µF series input capacitor for proper operation.
—	—	3	INB	Video Input B. Use a 0.1µF series input capacitor for proper operation.
—	—	5	SYNCIO	Sync Pulse Input or Output
—	—	8	OUT	Buffer Output

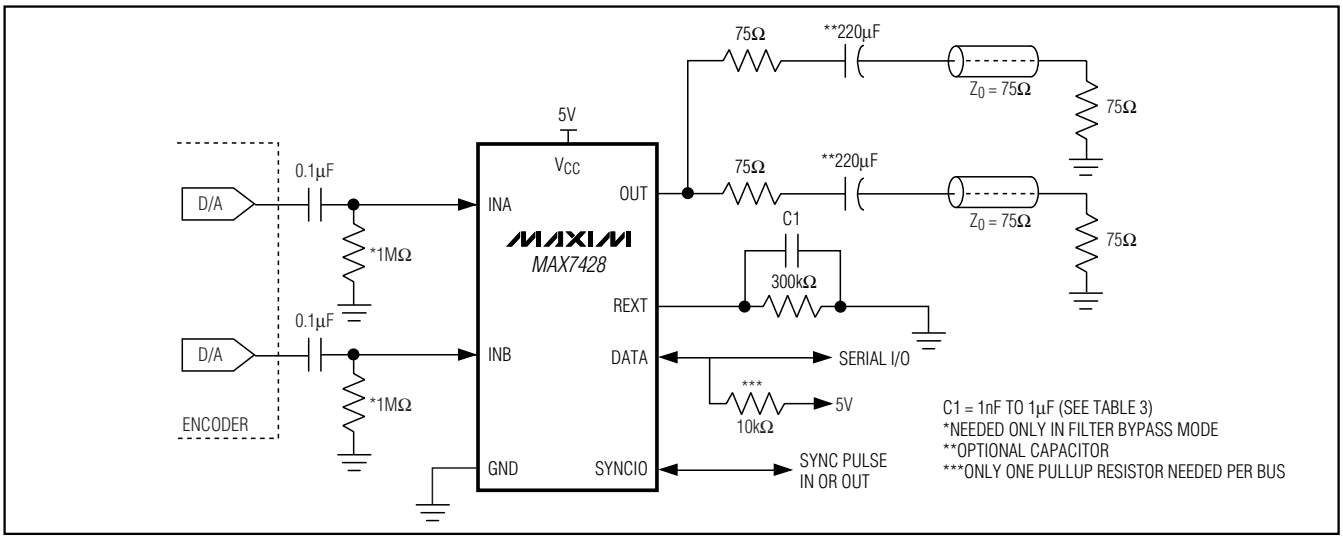


Figure 1. MAX7428 Typical Application Circuit

Detailed Description

The MAX7428/MAX7430/MAX7432A filter and buffer the outputs of DAC encoder chipsets that process digital video information in applications such as set-top boxes, hard-disk recorders, DVD players, recorders, and digital VCRs. These devices also filter and "clean-up" analog video signals. Each channel in the MAX7428/MAX7430/MAX7432A includes an input mux to select the input channel, a 6th-order Sallen-Key filter with four adjustable high-frequency boost levels, an output buffer with a 6dB gain, a sync detector and clamp, and an external resistor to set internal bias levels. Output disable adds additional multiplexing in a wired-OR configuration. Filter bypass, in conjunction with the two inputs, can be used to provide filtered and unfiltered video signal processing. Maxim's Single Pin Bus (MSPB) interface controls all of the above features. An external capacitor is used to assign each device a unique address that allows control of up to 16 devices on the same bus. Typical application circuits for the MAX7428/MAX7430/MAX7432A are shown in Figures 1, 2, and 3.

Input Considerations

Use a 0.1µF ceramic capacitor to AC-couple the input to the MAX7428/MAX7430/MAX7432A. This input capacitor stores a DC level to level-shift the input signal to an optimal point between V_{CC} and GND. The ABSEL bit on the Control Register sets which channel (IN_A or IN_B) is selected (*Control Register* section). The IN_A and IN_B inputs have a typical input resistance of 50kΩ.

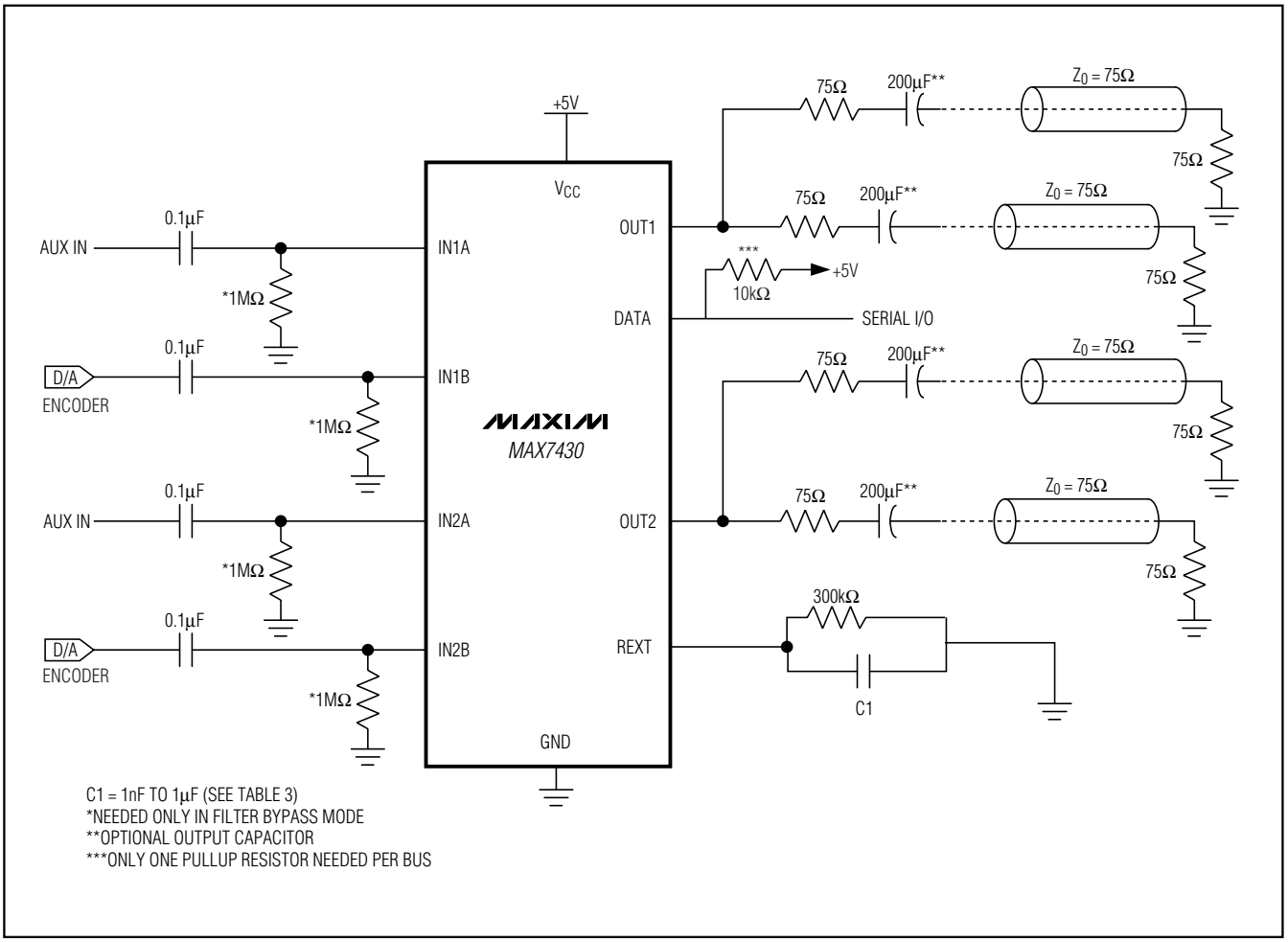


Figure 2. MAX7430 Typical Application Circuit

Standard Definition Video Reconstruction Filters and Buffers

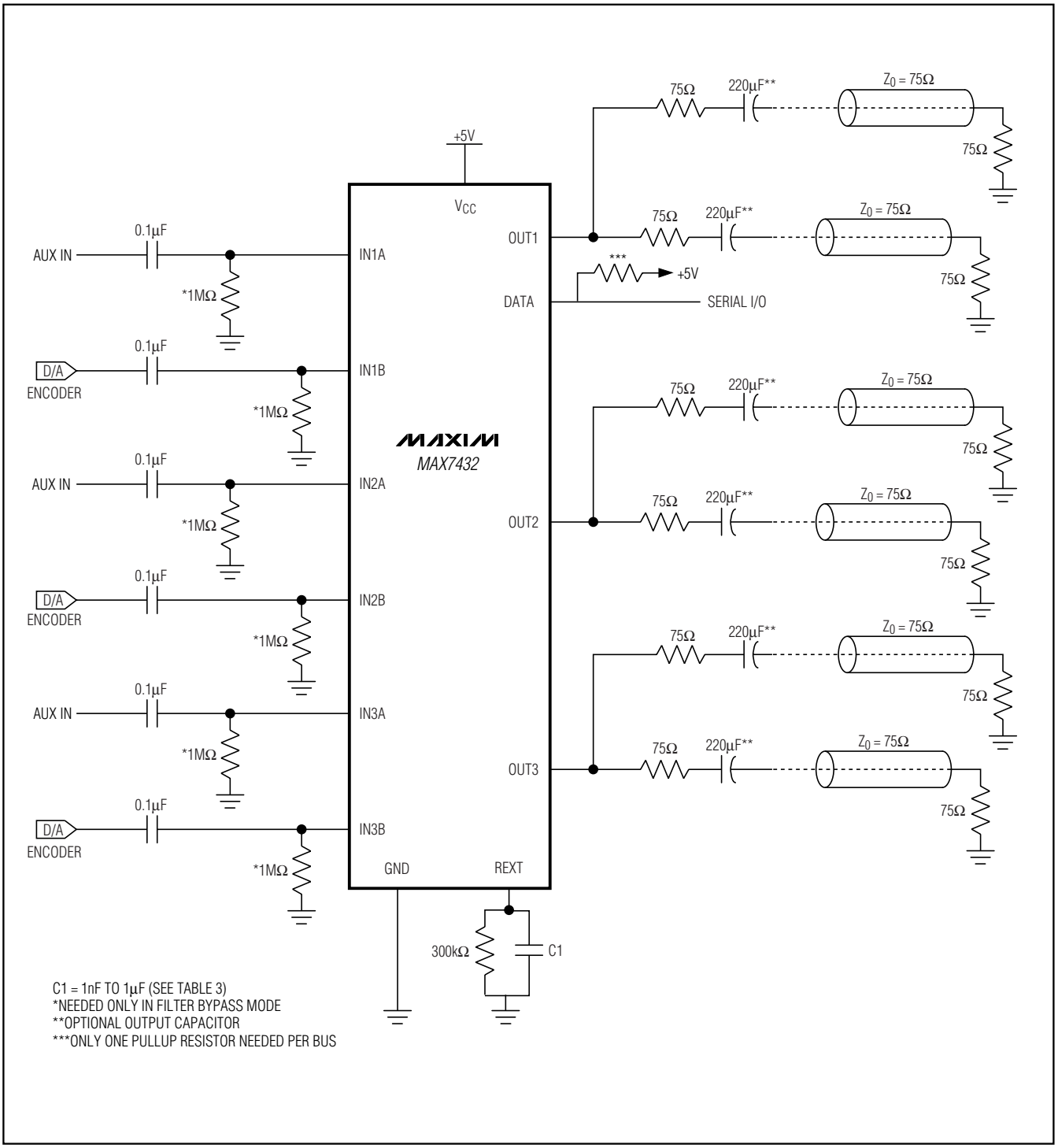


Figure 3. MAX7432A Typical Application Circuit

Table 1. MAX7428 Control Register

	(MSB)							FIRST BIT (LSB)
NAME	SYNCIO	ABSEL	BYPASS	CLEVEL	BOOST1	BOOST0	OUTDISABLE	—
DEFAULT	0	1	1	0	0	0	0	0

Filter

Filter Response

The reconstruction filter consists of a 6th-order Butterworth filter in three second-order stages. The Butterworth filter features a maximally flat passband for NTSC and PAL bandwidths. The stopband offers typically 50dB of attenuation at sampling frequencies of 25MHz and above (see *Typical Operating Characteristics*).

The corner frequency is not critical since the response of the filter meets both the stopband and passband specifications. The MAX7428/MAX7430/MAX7432A incorporate an autotrimming feature that reduces the corner frequency variation digitally. It is possible, although not likely, that a discrete shift in the corner frequency may occur due to an external environmental change. The autotrimming operates continuously so that the corner frequency remains centered over the full operating temperature range.

High-Frequency Boost

The high-frequency boost compensates for signal degradation and roll-off in the signal path prior to the MAX7428/MAX7430/MAX7432A. High-frequency boost is programmable in four steps to increase image sharpness.

Output Buffer

The output buffer is able to drive two 150Ω video loads with a 2Vp-p signal. The +6dB gain of the output buffer is independent of the filter bypass or input selection. The output buffer drives the 75Ω backmatch resistors and series capacitor (typically 220µF). The MAX7428/MAX7430/MAX7432A are able to drive the video load directly without using the 220µF capacitor. This feature is common in SCART applications. The OUTDISABLE bit of the control register disables the output (mute) (see *Control Register* section).

Filter Bypass

The MAX7428/MAX7430/MAX7432A offer selectable filter bypassing that allows either of the video inputs to be filtered or unfiltered. The 1MΩ optional input resistors are needed only in filter bypass mode to provide a discharge path for the input coupling capacitors.

Serial Interface

Maxim's Single Pin Bus (MSPB) interface uses DATA to transfer data to and from the microprocessor (µP) and the MAX7428/MAX7430/MAX7432A. This negative logic protocol uses three different pulse widths to represent a logic "1", logic "0", and control commands. MSPB allows up to 16 devices to be connected on the same bus by assigning a unique 4-bit identification address to each device. The µP can communicate to each device individually or by sending a "broadcast" message to all the devices. The unique address for each device is set by means of the time constant set by the external capacitor connected in parallel with the external 300kΩ resistor (see *Initializing the MAX7428/MAX7430/MAX7432A* section).

MAX7428 Control Register

Table 1 defines the structure of the MAX7428 8-bit control register programmed by MSPB. This register controls the selection of INA or INB, SYNCIO functionality, filter bypassing, clamp-level selection, high-frequency boost control, and output disable. See *Maxim's Single Pin Bus Interface (MSPB)* section for detailed programming instructions.

SYNCIO: SYNCIO Select bit. A logic 0 sets the SYNCIO pin to function as an output while a logic 1 sets SYNCIO to function as an input.

ABSEL: Channel Select bit. A logic 0 selects the input at INB to be processed while a logic 1 selects the input at INA to be processed.

BYPASS: Filter Bypass Select bit. A logic 1 selects the filter while a logic 0 bypasses the filter.

Table 2. Boost Level Programming

BOOST1	BOOST0	RELATIVE HIGH FREQUENCY BOOST
0	0	0
0	1	0.3db to 0.5db
1	0	0.6db to 1.0db
1	1	0.9db to 1.5db

Standard Definition Video Reconstruction Filters and Buffers

Table 3. MAX7430 Control Register

(MSB)

NAME	—	ABSEL2	BYPASS2	CLEVEL2	BOOST1(2)	BOOST0(2)	OUT DISABLE2	—
DEFAULT	0	1	1	0	0	0	0	0

NAME	—	ABSEL1	BYPASS1	CLEVEL1	BOOST1(1)	BOOST0(1)	OUT DISABLE1	—
DEFAULT	0	1	1	0	0	0	0	0

FIRST BIT (LSB)

CLEVEL: Clamp Level bit. A logic 0 selects a clamp level of 1V while a logic 0 selects a clamp level of 1.5V at the output.

[BOOST1, BOOST0]: High-Frequency Boost Control bits. The adjust bits select the amount of high-frequency boost for the filter. Table 2 defines four levels of adjustment.

OUTDISABLE: Output Disable bit. A logic 0 selects normal operation while a logic 1 places the output in a high-impedance state.

MAX7430 Control Register

Table 3 defines the structure of the MAX7430 16-bit control register programmed by MSPB. This register controls the selection of IN_A or IN_B, selection of filter 1 or 2, filter bypassing, clamp-level selection, high-frequency boost control, and output disable. See *Maxim's Single Pin Bus Interface (MSPB)* section for detailed programming instructions.

ABSEL_: Channel Select bit. A logic zero selects the input at IN_B to be processed while a logic 1 selects the input at IN_A to be processed.

BYPASS_: Filter Bypass Select bit. A logic 1 selects the channel filter while a logic 0 bypasses the channel filter.

CLEVEL_: Clamp Level bit. A logic 0 selects a channel clamp level of 1V while a logic 0 selects a channel clamp level of 1.5V at the output.

[BOOST1_, BOOST0_]: High-Frequency Boost Control bits. The adjust bits select the amount of high-frequency boost for the channel filter. Table 4 defines four levels of adjustment.

OUTDISABLE_: Output Disable bit. A logic 0 selects normal channel output operation while a logic 1 puts the channel output in a high-impedance state.

Table 4. Boost Level Programming

BOOST1_	BOOST0_	RELATIVE HIGH FREQUENCY BOOST
0	0	0
0	1	0.3dB to 0.5dB
1	0	0.6dB to 1.0dB
1	1	0.9dB to 1.5dB

MAX7432A Control Register

Table 5 defines the structure of the MAX7432A 24-bit control register programmed by MSPB. This register controls the selection of IN_A or IN_B, selection of filter 1, 2, or 3, filter bypassing, clamp-level selection, high-frequency boost control, and output disable. See *Maxim's Single-Pin Bus Interface (MSPB)* section for detailed programming instructions.

ABSEL_: Channel Select bit. A logic zero selects the input at IN_B to be processed while a logic 1 selects the input at IN_A to be processed.

BYPASS_: Filter Bypass Select bit. A logic 1 selects the channel filter while a logic 0 bypasses the channel filter.

CLEVEL_: Clamp Level bit. A logic 0 selects a channel clamp level of 1V while a logic 0 selects a channel clamp level of 1.5V at the output.

[BOOST1_, BOOST0_]: High-Frequency Boost Control bits. The adjust bits select the amount of high-frequency boost for the channel filter. Table 6 defines four levels of adjustment.

OUTDISABLE_: Output Disable Bit. A logic 0 selects normal channel output operation while a logic 1 puts the channel output in high-impedance state.

Table 5. MAX7432A Control Register

(MSB)

NAME	—	ABSEL3	BYPASS3	CLEVEL3	BOOST1(3)	BOOST0(3)	OUT DISABLE3	—
DEFAULT	0	1	1	0	0	0	0	0

NAME	—	ABSEL2	BYPASS2	CLEVEL2	BOOST1(2)	BOOST0(2)	OUT DISABLE2	—
DEFAULT	0	1	1	0	0	0	0	0

NAME	—	ABSEL1	BYPASS1	CLEVEL1	BOOST1(1)	BOOST0(1)	OUT DISABLE1	—
DEFAULT	0	1	1	0	0	0	0	0

FIRST BIT (LSB)

Applications Information

Maxim's Single Pin Bus (MSPB) Serial Interface

The MSPB interface uses three pulses of different widths to represent commands and data bits. Figure 4 shows the set of pulses that the single pin interface uses to communicate with the device. A combination of the one pulse (t_1), zero pulse (t_0), transaction pulse (t_T), and prompt pulse (t_P), writes to, reads back from, and sends broadcast data to the devices on the bus.

Note: The zero pulse and prompt pulse are the same. Initialization pulses are significantly longer and are used only on power-up or software reset.

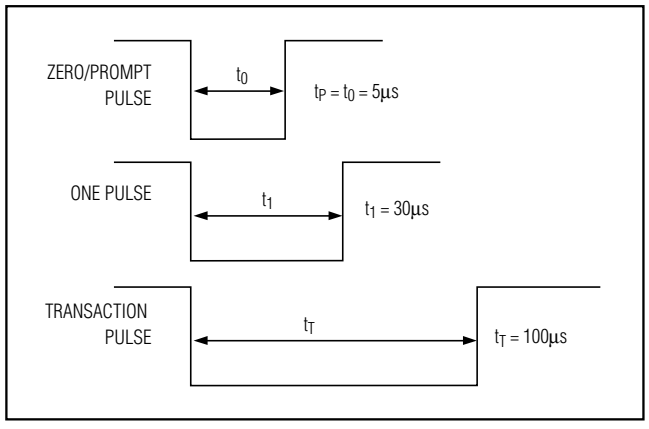


Figure 4. MSPB Interface Pulses

Table 6. Boost Level Programming

BOOST1_	BOOST0_	RELATIVE HIGH FREQUENCY BOOST
0	0	0
0	1	0.3dB to 0.5dB
1	0	0.6dB to 1.0dB
1	1	0.9dB to 1.5dB

Initializing the MAX7428/MAX7430/MAX7432A

Initialization is performed only after power-up or software reset. It assigns a unique address to each device on the bus. The time constant of the capacitor connected to R_{EXT} in parallel with the 300kΩ resistor determines the order in which the devices are initialized (address assigned). The device with the largest time constant is initialized first and so on, in descending order. Table 7 shows the "Initialize Wait" and "Initialize Time" pulse widths needed for a specific capacitor value and tolerance. Program each device on the bus with this command sequence starting with the device with the biggest capacitor. To reinitialize a device, cycle the power or use a software reset. The following is the command sequence and timing diagram (Figure 5) for initialization as shown below. Chip ID is entered LSB first.

Note: If there is only one device on the bus, no initialization is needed. Communicate to the device using the broadcast command described on page 13.

Standard Definition Video Reconstruction Filters and Buffers

Table 7. Initialization Capacitor Values and Pulse Widths (C_{EXT} = ±10% Tolerance, R_{EXT} = ±1% Tolerance)

CAPACITOR VALUE (nF)	INITIALIZING WAIT PERIOD (ms) ($t_{INTWAIT}$)	INITIALIZING TIME PERIOD (ms) WITH R_{REXT} = 300kΩ (t_{INT})		
		MIN	TYP	MAX
1000	20.000	162 (136.8)	171 (144)	179 (151.2)
680	13.600	112	118	123
470	9.400	52.6 (44.1)	55.4 (46.4)	58.2 (48.72)
220	4.400	35.90	37.80	39.70
150	3.000	23.90 (13.7)	25.20 (14.4)	26.50 (15.1)
100	2.000	16.25	17.10	17.95
68	1.360	11.21 (4.4)	11.80 (4.64)	12.39 (4.9)
47	0.940	5.26	5.54	5.82
22	0.440	3.59	3.78	3.97
15	0.300	2.39	2.52	2.65
10	0.200	1.625 (1.37)	1.710 (1.44)	1.795 (1.51)
6.8	0.136	1.121	1.180	1.239
4.7	0.094	0.526 (0.441)	0.554 (0.464)	0.582 (0.487)
2.2	0.044	0.359	0.378	0.397
1.5	0.030	0.239	0.252	0.265
1	0.020	0.162 (0.137)	0.171 (0.144)	0.179 (0.151)

Note: *( ) Indicates the time periods associated with 20% capacitors. This limits the maximum number of devices on the bus to seven.*

Initialization Command Sequence:				
Initialize wait	T011	Initialize Time	Address ID = 4-bits	T111

Programming the MAX7428/MAX7430/MAX7432A

An address sequence precedes a write or read operation to determine with which device to communicate. If the address transmitted in this mode matches with a device's address, the device and µP can initiate data transfer. When entering the four address bits, ensure that the LSB is entered first. The following is the command sequence and timing diagram (Figure 6) for an address sequence.

Address Command Sequence:		
T010	Address = 4-bits	T111

Use a write sequence to load data into the data register of the device. It must follow an address sequence. Transmit a minimum of eight data bits for the MAX7428, 16 data bits for the MAX7430, or 24 data bits for the MAX7432A to make this transaction valid starting with the LSB first. The last 8/16/24 data bits are used if more than 8/16/24 bits are loaded into the register. The following is the command sequence and timing diagram (Figure 7) for a write sequence.

Write Command Sequence:		
T001	Data ≥ 8-bits (MAX7428, See Table 1) Data ≥ 16-bits (MAX7430, See Table 3) Data ≥ 24-bits (MAX7432A, See Table 5)	T111

During the read sequence, the µP sends a prompt pulse causing the device to output the data word LSB first. Similar to the write transaction, the read transaction must be preceded by an address sequence. If more than 8 prompts (MAX7428), 16 prompts (MAX7430), or 24 prompts (MAX7432A) are available, the device outputs the same data starting with the LSB again. The following is the command sequence and timing diagram (Figure 8) for a read sequence.

Read Command Sequence:		
T101	Prompts ≥ 8 (MAX7428) Prompts ≥ 16 (MAX7430) Prompts ≥ 24 (MAX7432A)	T111

The broadcast sequence writes data to the control registers of all the devices on the bus at the same time. Write data with the LSB first. The following is the command sequence and timing diagram (Figure 9) for the broadcast transaction. No address sequence is required. Use the broadcast command when there is only one device on the bus.

Broadcast Command Sequence:		
T000	Data ≥ 8-bits (MAX7428) Data ≥ 16-bits (MAX7430) Data ≥ 24-bits (MAX7432A)	T111

Executing a software reset serves the same function as a power-on reset and is achieved by transmitting all data bits (eight or more) for the MAX7428, sixteen or more ones for the MAX7430, or 24 or more ones for the MAX7432A to that device register.

Software Reset Command Sequence:		
T000	8 or more 1s (MAX7428) 16 or more 1s (MAX7430) 24 or more 1s (MAX7432A)	T111
OR		
T010	Address = 4-bits	T111
T001	8 or more 1s (MAX7428) 16 or more 1s (MAX7430) 24 or more 1s (MAX7432A)	T111

Composite Video Filtering

The MAX7428 is ideally suited for filtering composite video signals. Program the SYNCIO as an output when processing composite video signals. In the rare occasion that an external sync pulse is needed to process the composite video, program the SYNCIO as an input.

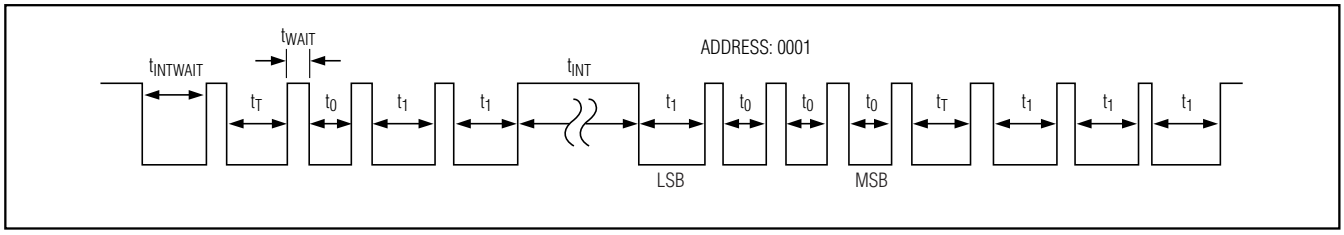


Figure 5. Initialization Timing Diagram

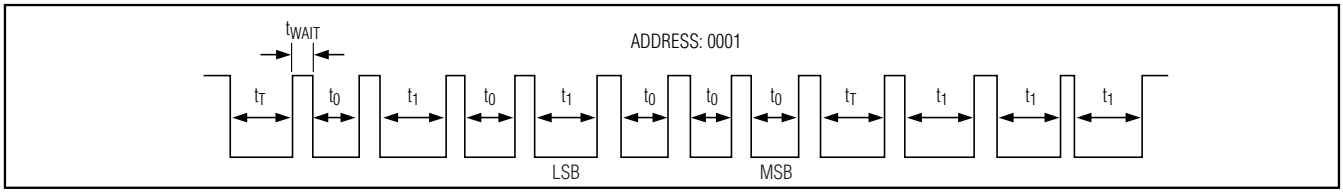


Figure 6. Address Timing Diagram

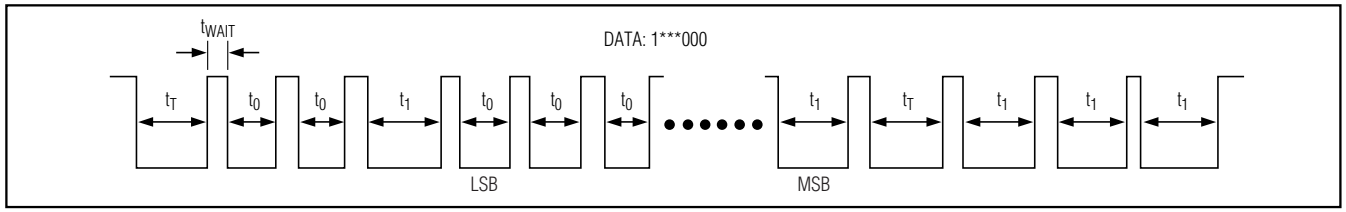


Figure 7. Write Timing Diagram

Standard Definition Video Reconstruction Filters and Buffers

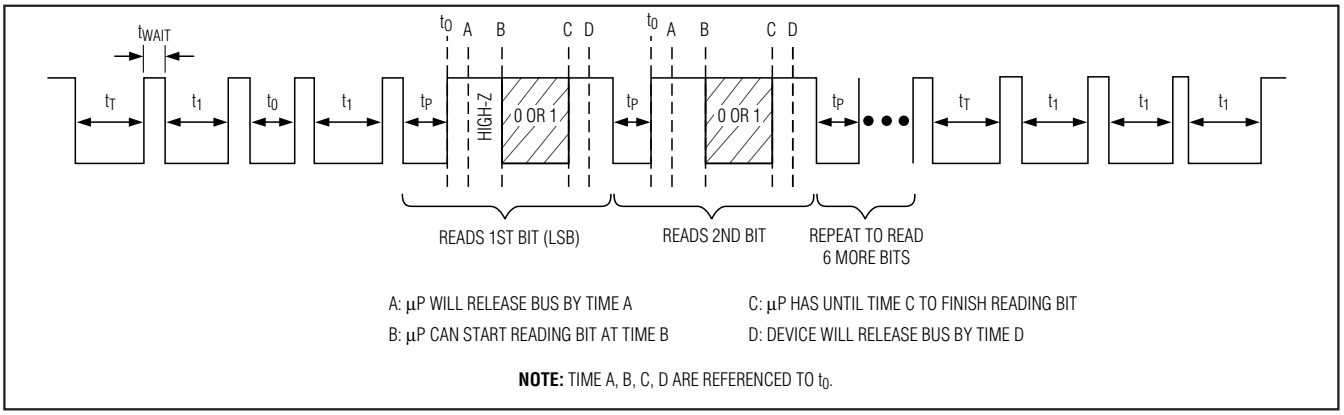


Figure 8. Read Timing Diagram

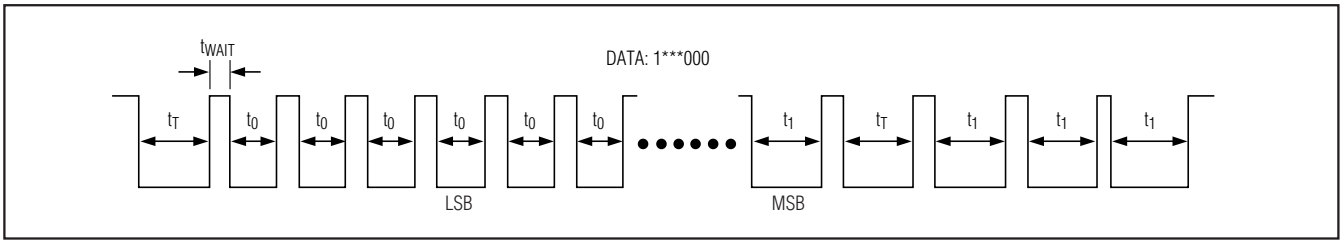


Figure 9. Broadcast Timing Diagram

When processing composite video set the clamp level to +1V (CLEVEL = 0). Use the MAX7430 to process two synchronous composite signals simultaneously. Use the MAX7432A to process three synchronous composite signals simultaneously.

Y/C Video Filtering

The MAX7430 is ideally suited for processing S-Video (Y/C) signals (Figure 10). Ensure that IN1_ filters the signal that contains the sync information (Y) since the clamping on IN2_ is internally controlled by the master channel (IN1_) sync. Set the clamp level for IN1_ to +1V (CLEVEL1 = 0) and set the clamp level for IN2_ to +1.5V (CLEVEL2 = 1).

Use two MAX7428s for Y/C video filtering. Since only the Y signal contains the sync, a typical Y/C video-filtering application requires a master-slave configuration of the SYNCIO. The MAX7428 processing the Y signal should have SYNCIO configured as an output, which in turn drives the SYNCIO of the second MAX7428, processing the C signal that has its SYNCIO configured as an input (Figure 11). Clamping level for the Y signal should be set for +1V (CLEVEL = 0), and clamping level for the C signal should be set for +1.5V (CLEVEL = 1). Use the MAX7432A to filter one Y/C and one composite video signal that are synchronous.

Component Video (RGB or Y P_b P_r) Filtering

Component video consists of three separate signals. Typically the three signals are separate red, green, and blue (RGB) signals or Y (luma) and two color difference signals: B-Y (P_b) which is blue minus luma and R-Y (P_r), which is red minus luma. Sync information is included with the Y signal of Y P_b P_r component video, or in the case of RGB, sync is usually carried on the G or on a separate H sync line. The MAX7432A is ideally suited for filtering component video signals. Ensure that the sync signal (Y for Y P_b P_r signals and usually G for RGB signals) is filtered by IN1_ since IN2_ and IN3_ are internally synced to IN1_. Set the clamp level for IN1_ to +1V (CLEVEL1 = 0) and set the clamp levels for IN2_ and IN3_ to +1.5V (CLEVEL2, 3 = 1) for Y P_b P_r filtering (Figure 12) and set all clamp levels to 1V (CLEVEL_ = 0) for RGB filtering (Figure 13). A Y P_b P_r component video-filter application requires three MAX7428s with SYNCIO master-slave configuration. The MAX7428 processing the Y signal has its SYNCIO configured as an output, which in turn drives the SYNCIO inputs of the other MAX7428s (Figure 14). For RGB video signal filtering with a separate horizontal sync signal, configure all MAX7428s for SYNCIO as an input (Figure 15).

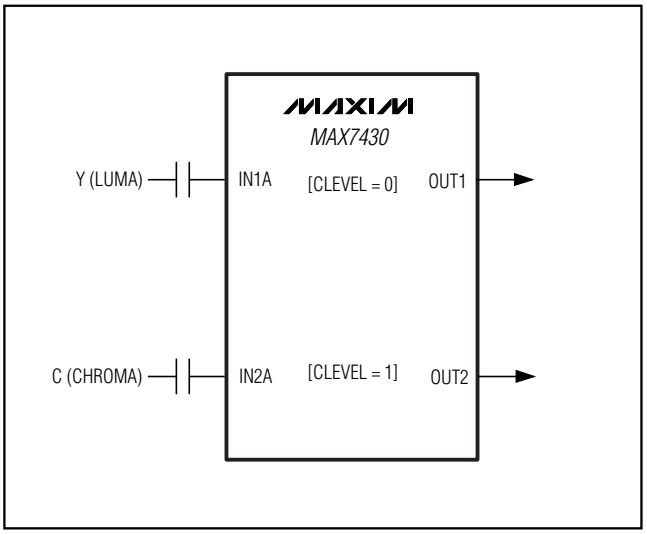


Figure 10. MAX7430 Y/C Video Filter Application

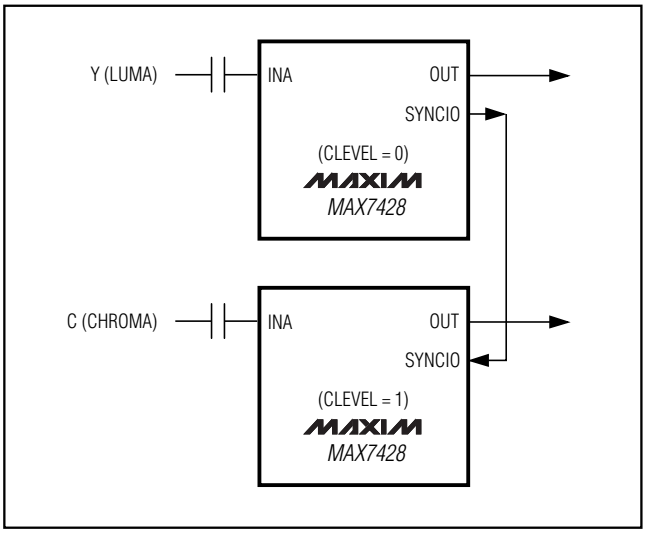


Figure 11. Y/C Video Filter Application

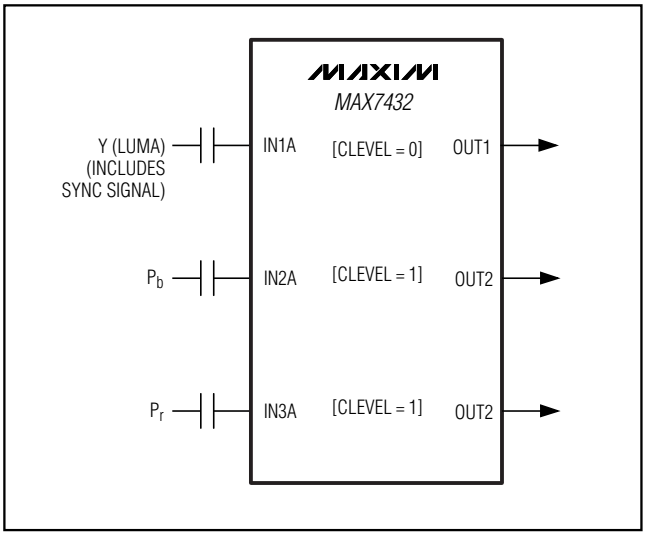


Figure 12. MAX7432A Y P_b P_r Video Filter Application

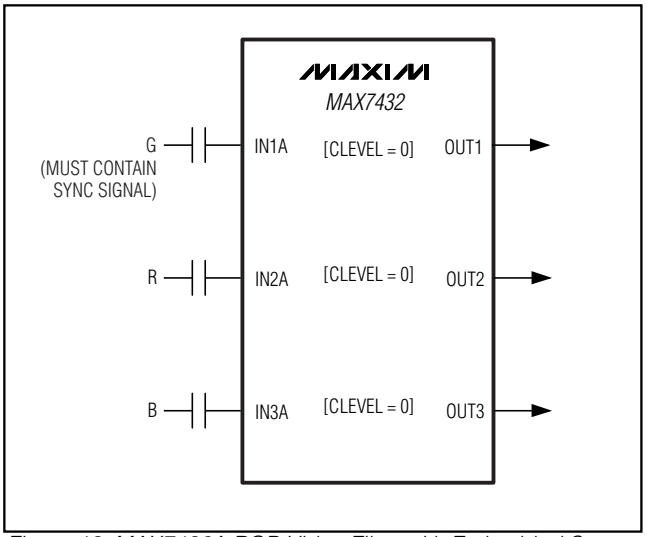


Figure 13. MAX7432A RGB Video Filter with Embedded Sync Application

Set the clamping levels for component video so the MAX7428 processing Y clamps at +1V (CLEVEL = 0). The remaining two MAX7428s should have clamp levels set to +1.5V (CLEVEL = 1). For RGB video with external sync (H), all three MAX7428s should have clamp levels set to +1V (CLEVEL = 0).

Power-Supply Bypassing and Layout

The MAX7428/MAX7430/MAX7432A operate from a single +5V supply. Bypass V_{CC} to GND with a 0.1µF capacitor. Place all external components as close to the devices as possible. Refer to the MAX7428EVKIT for a proven PC board layout example.

Standard Definition Video Reconstruction Filters and Buffers

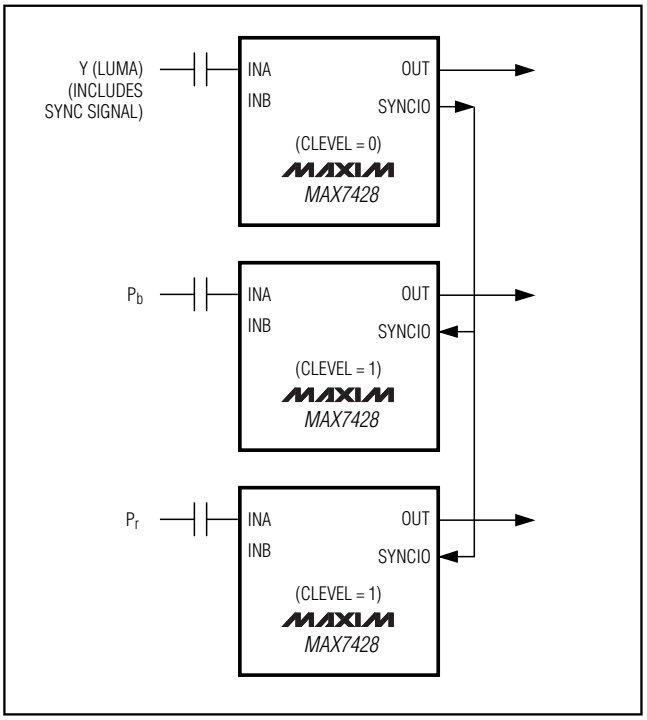


Figure 14. Y P_b P_r Video Filter Application

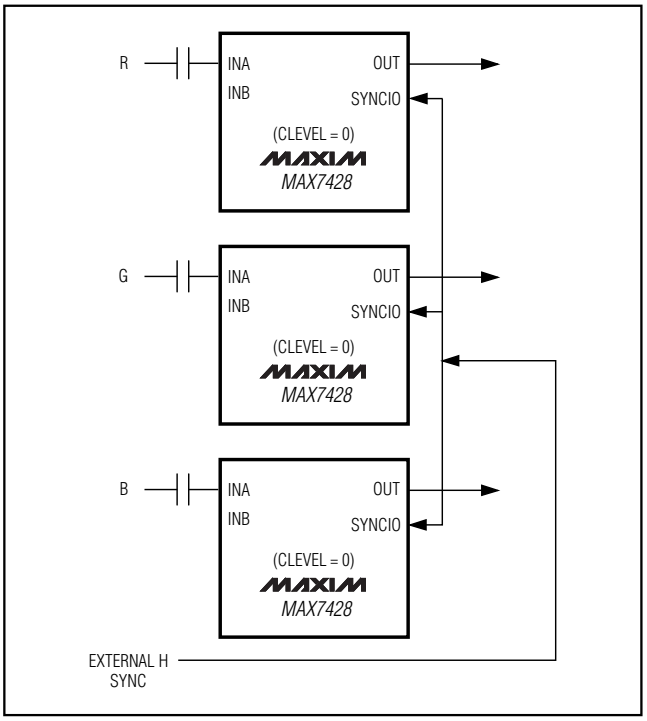


Figure 15. RGB Video Filter with External Sync Application

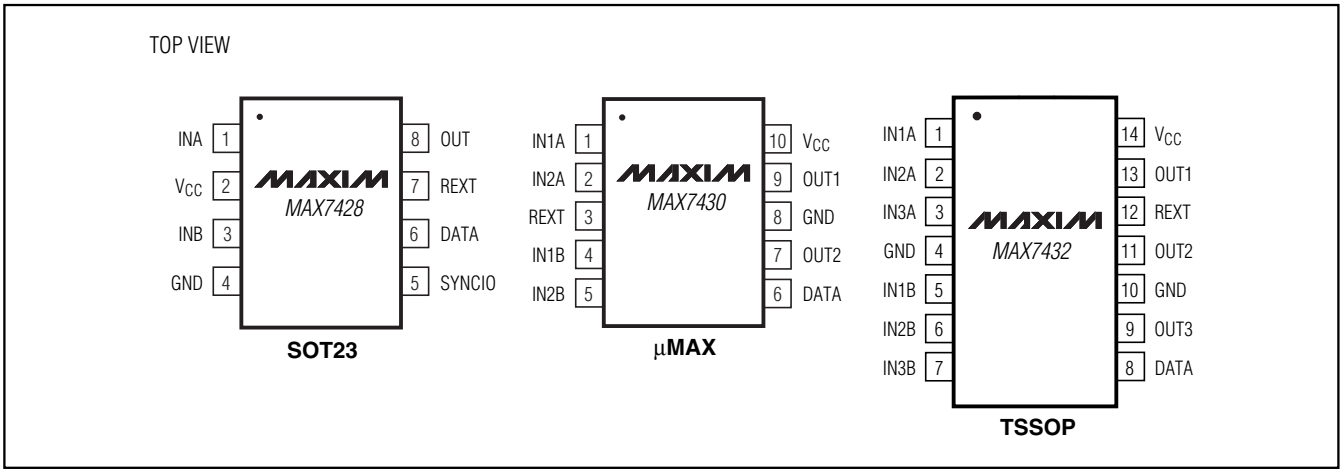
Chip Information

TRANSISTOR COUNT: MAX7428 = 4955
MAX7430 = 7413
MAX7432A = 9873

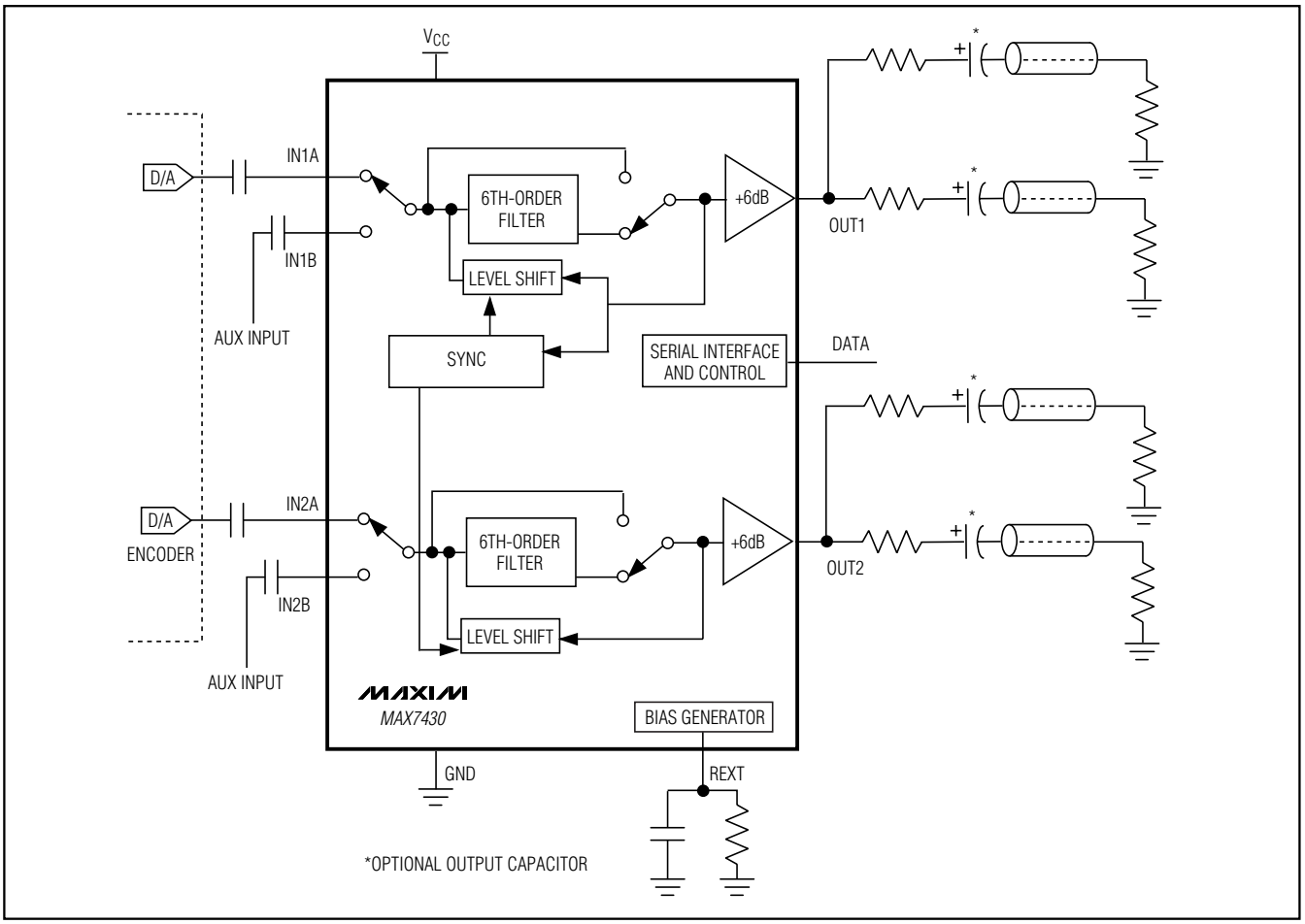
PROCESS: BiCMOS

Standard Definition Video Reconstruction Filters and Buffers

Pin Configurations

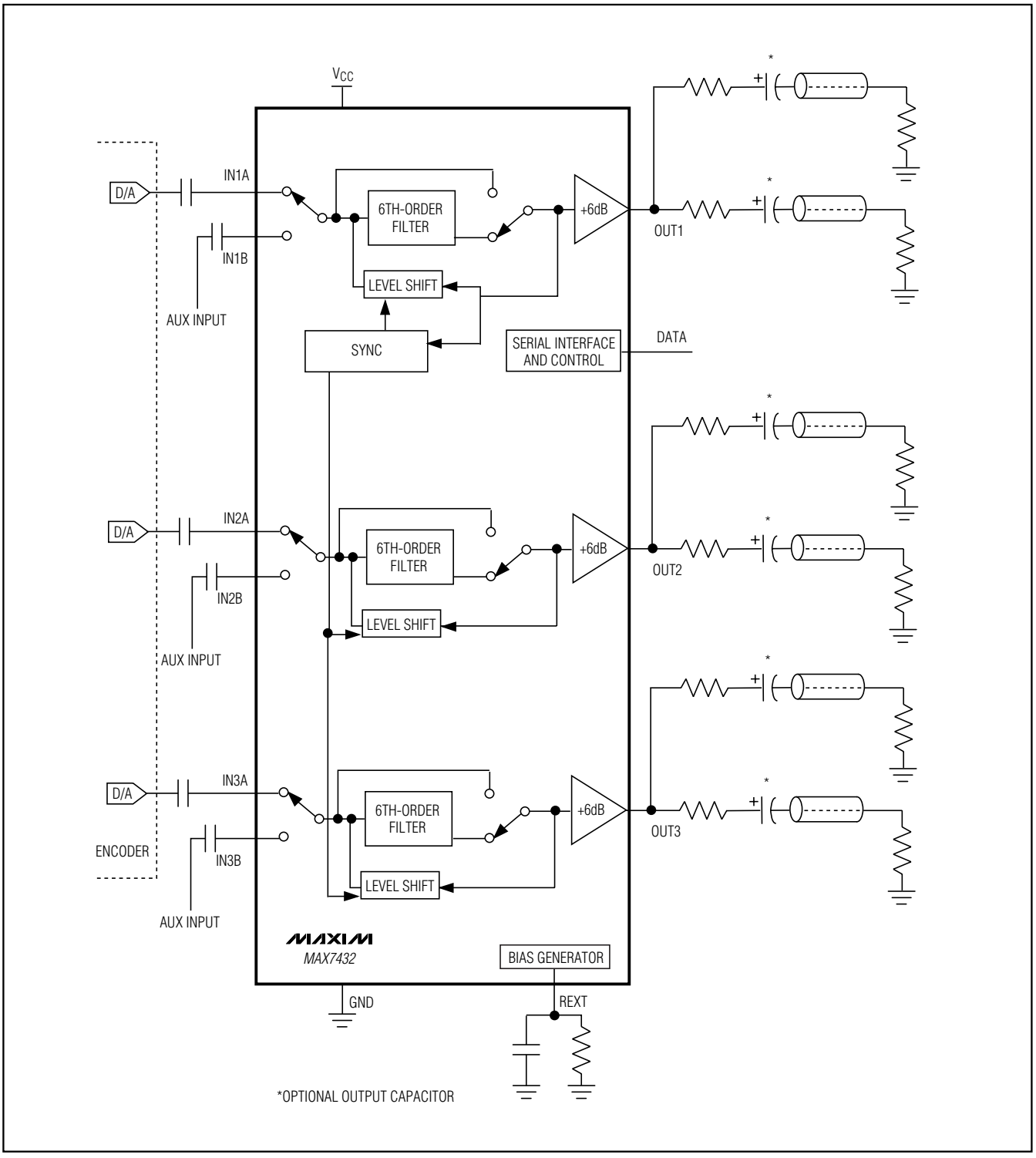


Functional Diagrams (continued)



Standard Definition Video Reconstruction Filters and Buffers

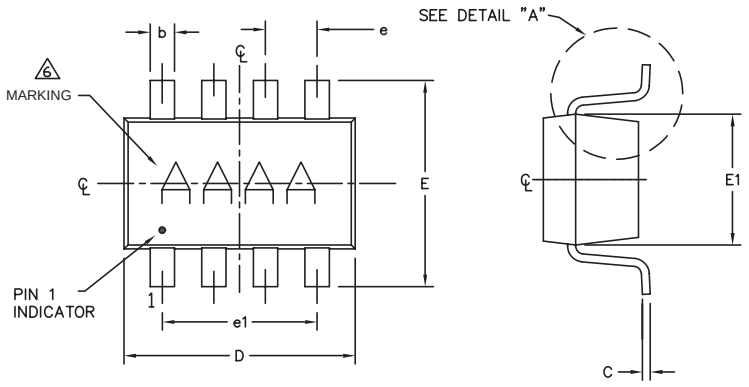
Functional Diagrams (continued)



Package Information

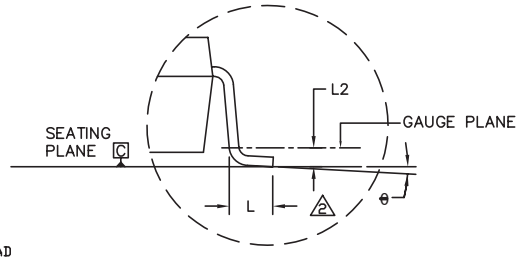
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS



SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.06	0.15
A2	0.90	1.10	1.30
b	0.22	0.30	0.38
C	0.08	0.15	0.22
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.30	0.45	0.60
L2	0.25 BSC.		
e	0.65 BSC.		
e1	1.95 REF.		
θ	0°	3°	8°

PKG CODES:
K8-1, K8-2, K8F-4, K8FH-4, K8-5, K8C-6; K8SN-1



DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

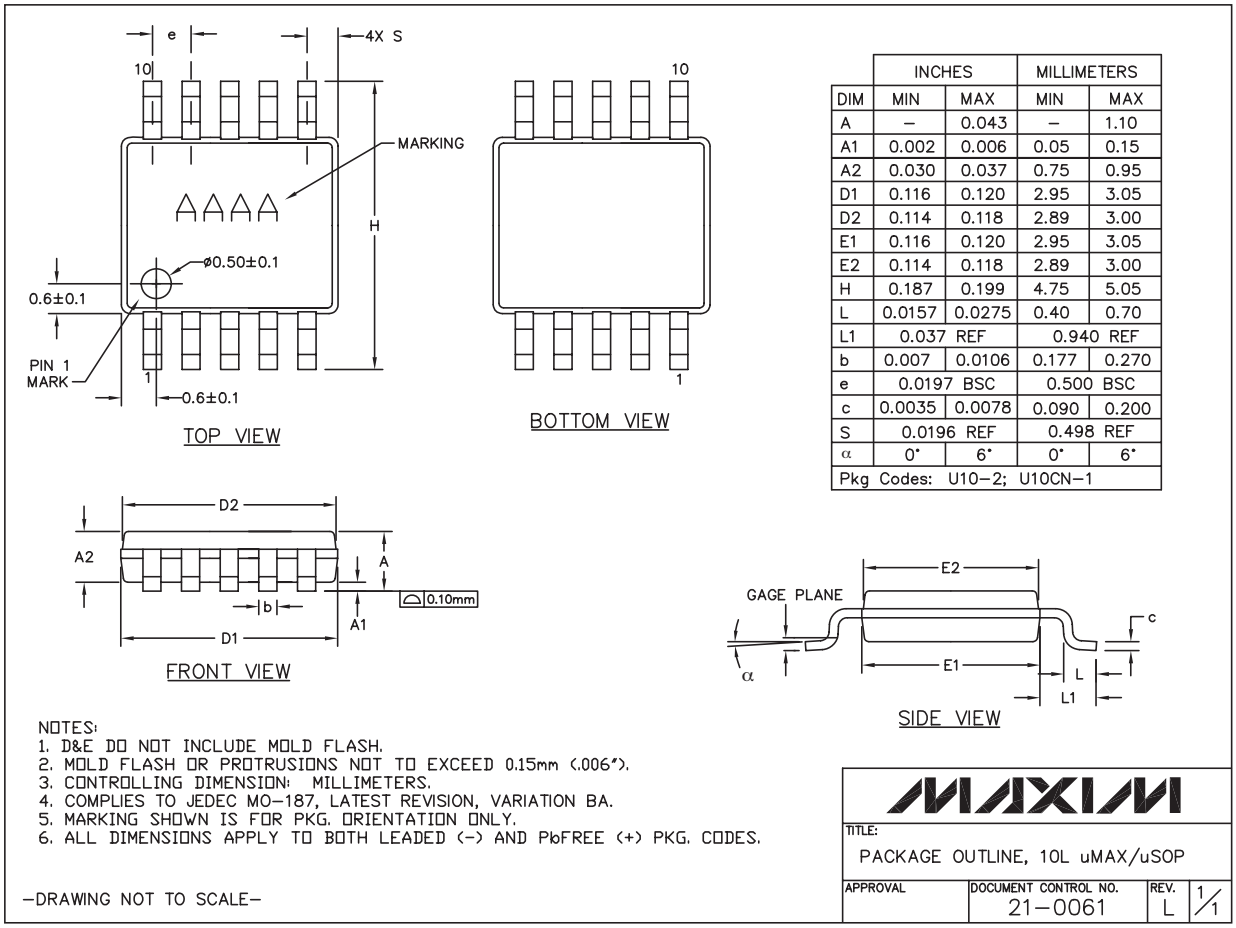
TITLE:
PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	H	1/1

Standard Definition Video Reconstruction Filters and Buffers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

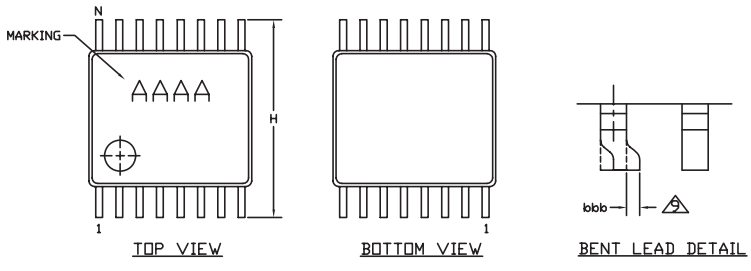


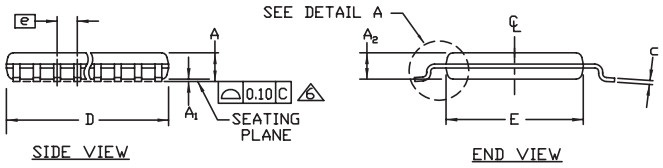
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°
Pkg Codes: U10-2; U10CN-1				

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS





SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1; U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1; U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2; U20M-2 U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1; U28-2; U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.
10. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	J	1/1

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX7428EKA+T