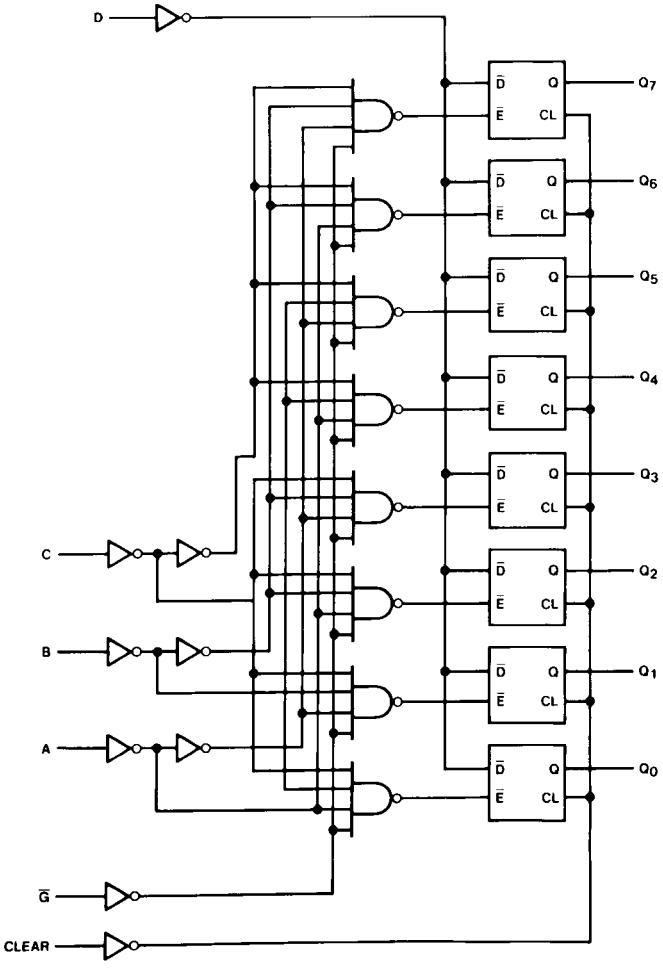
Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20$ μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0V		8.0	80	160	μA
		I_{OUT} = 0 μA						

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

(V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6 ns, C_L = 15 pF unless otherwise specified.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		20	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		20	35	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		17	27	ns
t_W	Minimum Enable Pulse Width		10	16	ns
t_W	Minimum Clear Pulse Width		10	16	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	ns
t_S	Minimum Setup Time Select or Data to Enable		15	20	ns
t_H	Minimum Hold Time Data or Address to Enable		–2	0	ns

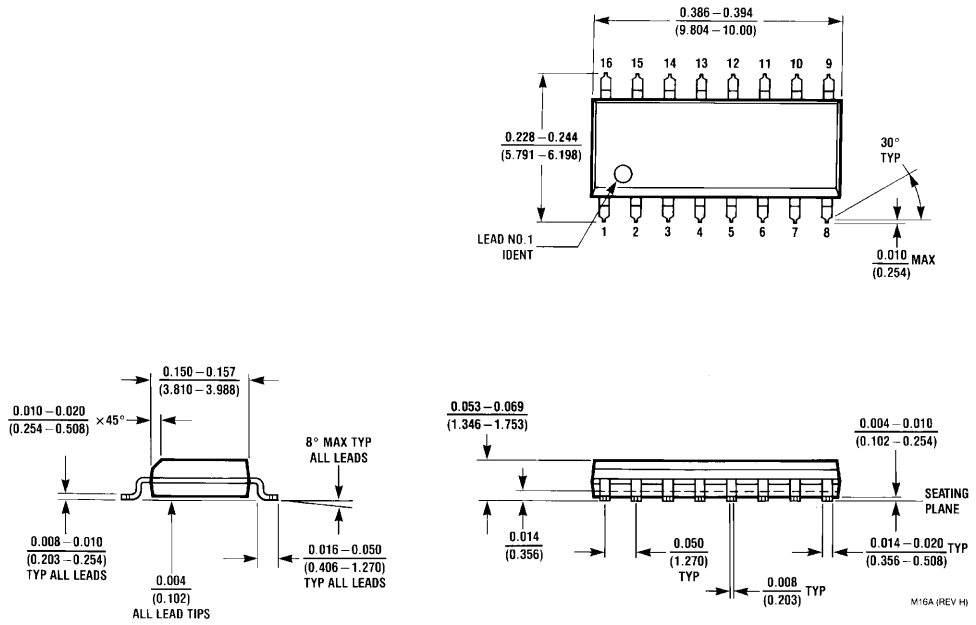
AC Electrical Characteristics

t_r = t_f = 6 ns, C_L = 50 pF, V_{CC} = 2.0V – 6.0V

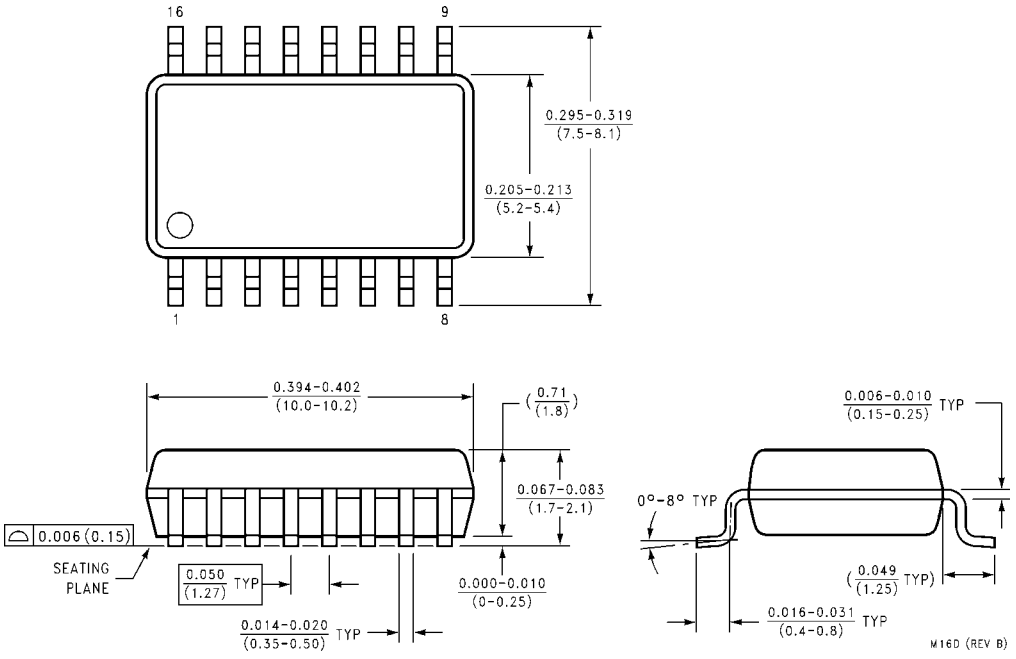
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = –40 to 85°C	T_A = –55 to 125°C		Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	180	225	250	ns
	Data to Output		4.5V	19	37	46	52	ns
			6.0V	17	32	40	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	72	220	275	310	ns
	Select to Output		4.5V	21	43	54	60	ns
			6.0V	18	37	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	65	200	250	280	ns
	Enable to Output		4.5V	27	40	50	58	ns
			6.0V	23	35	44	50	ns
t_{PHL}	Maximum Propagation Delay		2.0V	50	150	190	210	ns
	Clear to Output		4.5V	18	31	39	44	ns
			6.0V	16	26	32	37	ns
t_W	Minimum Pulse Width		2.0V		80	100	120	ns
	Clear or Enable		4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_S	Minimum Setup Time Address		2.0V		100	125	150	ns
	or Data to Enable		4.5V		20	25	28	ns
			6.0V		15	19	25	ns
t_H	Minimum Hold Time Address		2.0V	–10	0	0	0	ns
	or Data to Enable		4.5V	–2	0	0	0	ns
			6.0V	–2	0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} s V_{CC} sf + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

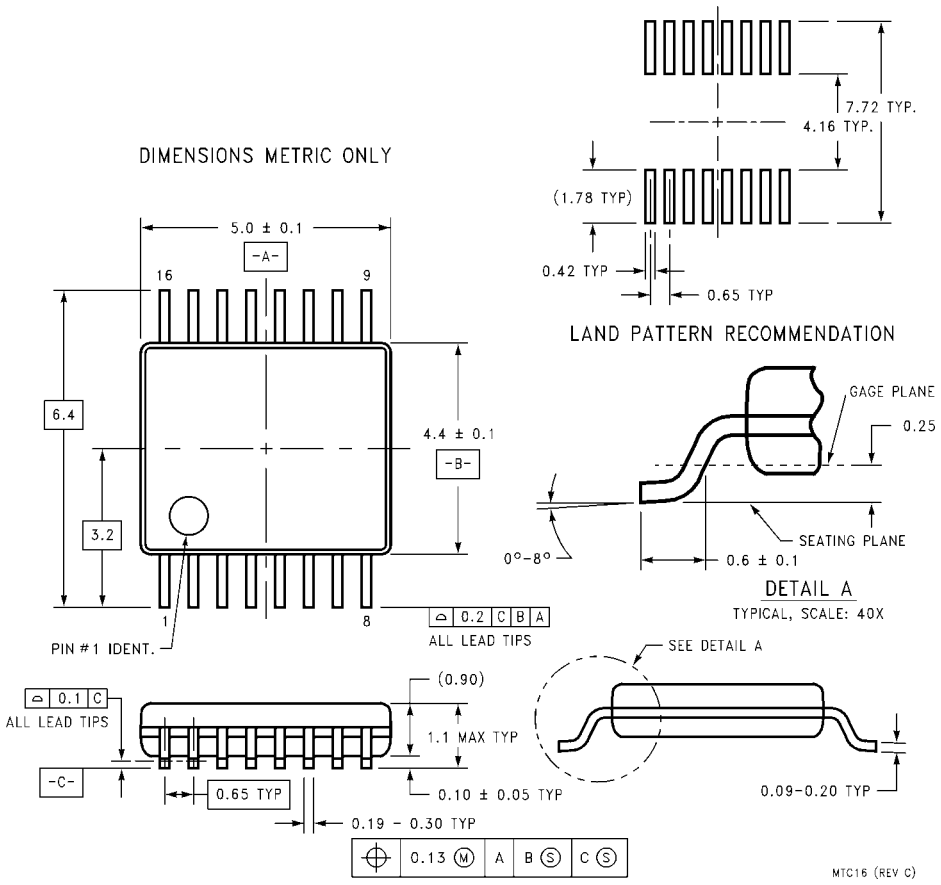


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A



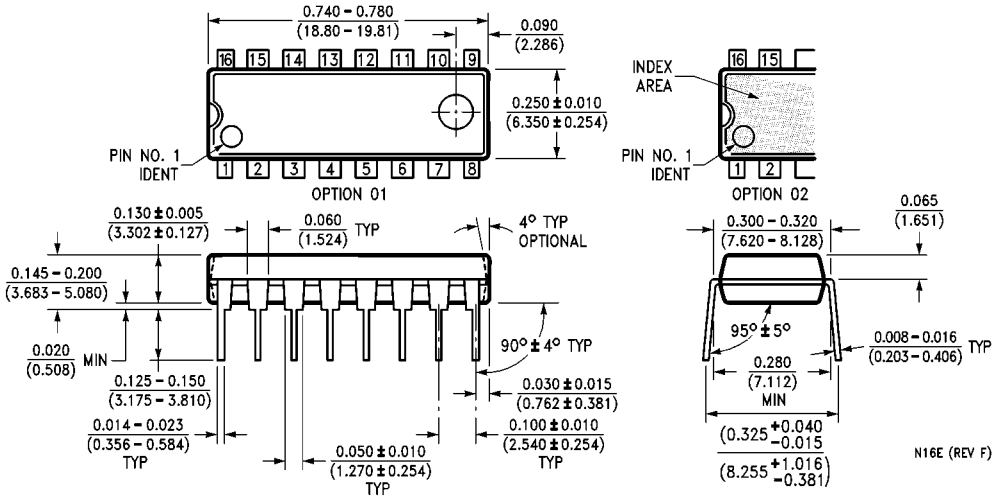
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:
MM74HC259SJX MM74HC259MX MM74HC259M MM74HC259N MM74HC259SJ MM74HC259MTC MM74HC259MTCX