

Z87010/Z87L10

Audio Encoder/Decoders



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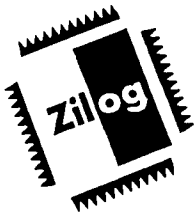
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Z87010/Z87L10 AUDIO ENCODER/DECODERS

FEATURES

| Device | ROM (Kbyte) | I/O Lines | Package Information |
|--------|-------------|-----------|---------------------------|
| Z87010 | 4 | 16 | 44-Pin PLCC 44-Pin QFP |
| Z87L10 | 4 | 16 | 44-Pin QFP |

Hardware

- 16-Bit DSP Processor
- 3.0V to 3.6V; -20° to +70°C, Z87L10
4.5V to 5.5V, -20° to +70°C, Z87010
- Static Architecture
- 512 Word On-Chip RAM
- Modified Harvard Architecture
- Direct Interface to Z87000 Frequency Hopping Spreader/Despreader

GENERAL DESCRIPTION

The Z87010/Z87L10 is a second generation CMOS Digital Signal Processor (DSP) that has been ROM-coded by Zilog to provide full-duplex 32 Kbps, Adaptive Delta Pulse Code Modulation (ADPCM) speech coding/decoding (CODEC), and interface to the Z87000/Z87L00 Spread Spectrum Cordless Telephone Controller. Together the Z87000/Z87L00 and Z87010/Z87L10 devices support the implementation of a 900 MHz frequency-hopping spread spectrum cordless telephone in conformance with United States FCC regulations for unlicensed operation.

The Z87010 and Z87L10 are distinct 5V and 3.3V versions of the ADPCM Audio Encoder/Decoder. For the sake of brevity, all subsequent references to the Z87010 in this document also are applicable to the Z87L10, unless specifically noted.

- Direct Interface to 8-Bit μ -law Telephone CODEC
- I/O Bus (16-Bit Tristable Data, 3-Bit Address)
- Wait State Generator
- Two External Interrupts
- Four Separate I/O Pins (2 Input, 2 Output)

Software

- Full Duplex 32 Kbps ADPCM Encoding/Decoding
- Single Tone and DTMF Signal Generation
- Sidetone, Volume Control, Mute Functions
- Large Phone Number Memory (21 numbers of 23 digits each)
- Master-Slave Protocol Interface to Z87000 Spreader/Despreader

The Z87010's single cycle instruction execution and Harvard bus structure promote efficient algorithm execution. The processor contains a 4K word program ROM and 512 word data RAM. Six dual operand fetching. Three vectored interrupts are complemented by a six level stack. The CODEC interface enables high-speed transfer rate to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface. An additional 13-bit timer is dedicated for general-purpose use.

The Z87010's circuitry is optimized to accommodate intricate signal processing algorithms and is used here for speech compression/decompression, generation of DTMF tones and other cordless telephone functions. Dedicated hardware allows direct interface to a variety of CODEC

GENERAL DESCRIPTION (Continued)

ICs. As configured by the Zilog-provided embedded software for digital cordless phones, the Z87010 supports a low-cost 8-bit μ -law telephone CODEC. The Z87010 is to

be used with the Z87000 and operates at 16.384 MHz, providing 16 MIPS of processing power needed for the cordless telephone application.

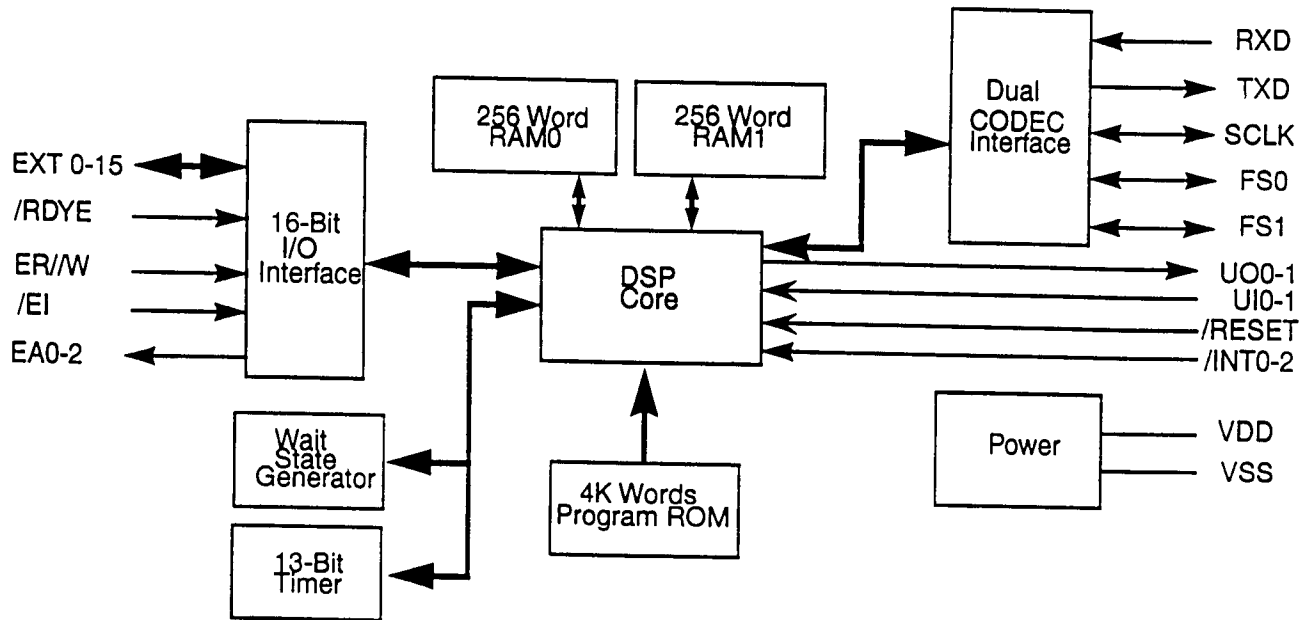


Figure 1. Z87010 Functional Block Diagram

Notes: All signals with a preceding front slash, '/', are active Low, e.g., B/**W** (WORD is active Low); /B/**W** (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|------------|-----------------|-----------------|
| Power | V _{CC} | V _{DD} |
| Ground | GND | V _{SS} |

PIN DESCRIPTION

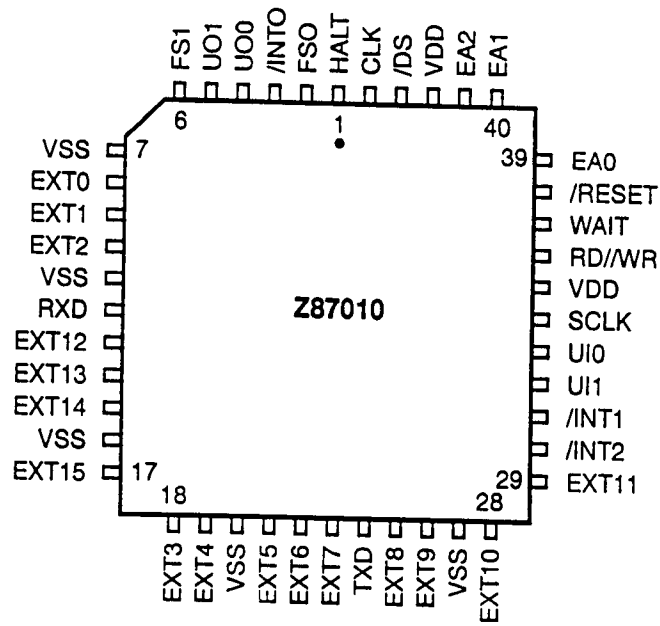


Figure 2. 44-Pin PLCC Pin Assignments

Table 1. 44-Pin PLCC Pin Identification

| No. | Symbol | Function | Direction |
|---------------|-----------------|------------------------------|---------------|
| 1 | HALT | Stop execution | Input |
| 2 | FS0 | CODEC0 frame sync | Input/Output* |
| 3 | /INT0 | Interrupt | Input |
| 4-5 | U00-U01 | User output | Output |
| 6 | FS1 | CODEC1 frame sync | Input/Output* |
| 7,11,16,20,27 | V _{SS} | Ground | |
| 8-10 | EXT0-EXT2 | External data bus | Input/Output |
| 12 | RXD | Serial input from CODECs | Input |
| 13-15 | EXT12-EXT14 | External data bus | Input/Output |
| 17 | EXT15 | External data bus | Input/Output |
| 18-19 | EXT3-EXT4 | External data bus | Input/Output |
| 21-23 | EXT5-EXT7 | External data bus | Input/Output |
| 24 | TXD | Serial output to CODECs | Output |
| 25-26 | EXT8-EXT9 | External data bus | Input/Output |
| 28-29 | EXT10-EXT11 | External data bus | Input/Output |
| 30 | /INT2 | Interrupt | Input |
| 31 | /INT1 | Interrupt | Input |
| 32 | UI1 | User input | Input |
| 33 | UI0 | User input | Input |
| 34 | SCLK | CODEC serial clock | Input/Output* |
| 35,42 | V _{DD} | Power supply | Input |
| 36 | RD/WR | RD /WR strobe for EXT bus | Output |
| 37 | WAIT | WAIT state | Input |
| 38 | /RESET | Reset | Input |
| 39-41 | EA0-EA2 | External address bus | Output |
| 43 | /DS | Data strobe for external bus | Output |
| 44 | CLK | Clock | Input |

Note: *Defined input or output by interface mode selection

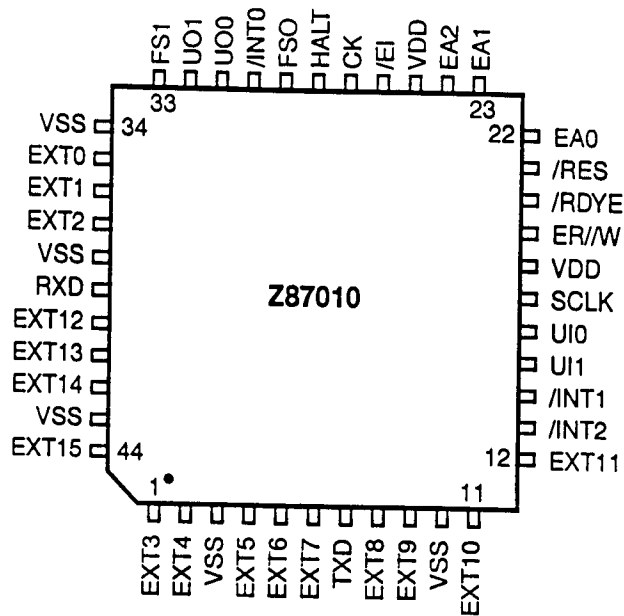


Figure 3. 44-Pin QFP Pin Assignments

Table 2. 44-Pin QFP Pin Identification

| No. | Symbol | Function | Direction |
|-------|-----------------|------------------------------|---------------|
| 1-2 | EXT3-EXT4 | External data bus | Input/Output |
| 3,10 | V _{SS} | Ground | — |
| 4-6 | EXT5-EXT7 | External data bus | Input/Output |
| 7 | TXD | Serial output to CODECs | Output |
| 8-9 | EXT8-EXT9 | External data bus | Input/Output |
| 11-12 | EXT10-EXT11 | External data bus | Input/Output |
| 13 | /INT2 | Interrupt | Input |
| 14 | /INT1 | Interrupt | Input |
| 15 | UI1 | User input | Input |
| 16 | UI0 | User input | Input |
| 17 | SCLK | CODEC serial clock | Input/Output* |
| 18,25 | V _{DD} | Power supply | Input |
| 19 | ER/W | R/W for External Bus | Output |
| 20 | /RDYE | Data Ready | Input |
| 21 | /RES | Reset | Input |
| 22-24 | EA0-EA2 | External Address Bus | Output |
| 26 | /EI | Data Strobe for External Bus | Output |
| 27 | CK | Clock | Input |
| 28 | HALT | Stop Execution | Input |
| 29 | FS0 | CODEC0 Frame Sync | Input/Output* |
| 30 | /INT0 | Interrupt | Input |
| 31-32 | U00-U01 | User Output | — |
| 33 | FS1 | CODEC1 Frame Sync | Input/Output* |
| 34 | V _{SS} | Ground | Input |
| 35-37 | EXT0-EXT2 | External data bus | Input/Output |
| 38 | V _{SS} | Ground | Input |
| 39 | RXD | Serial Input to CODEC | Input |
| 40-42 | EXT12-EXT14 | External Data Bus | Input/Output |
| 43 | V _{SS} | Ground | Input |
| 44 | EXT15 | External Data Bus | Input/Output |

Note: *Input or output is defined by interface mode selection.

ABSOLUTE MAXIMUM RATING

| Symbol | Description | Min. | Max. | Units |
|-----------|--------------------|-------|--------|-------|
| V_{DD} | Supply Voltage | -0.3 | +7.0 | V |
| T_{STG} | Storage Temp | -65°C | +150°C | C |
| T_A | Oper. Ambient Temp | -25° | +70° | C |

Note: *Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 4).

Standard test conditions are as follows:

$$3.0V \leq V_{DD} \leq 3.6V \text{ (Z87L10)}$$

$$4.5V \leq V_{DD} \leq 5.5V \text{ (Z87010)}$$

$$V_{SS} = 0V$$

$$T_A = -20^\circ \text{ to } +70^\circ\text{C}$$

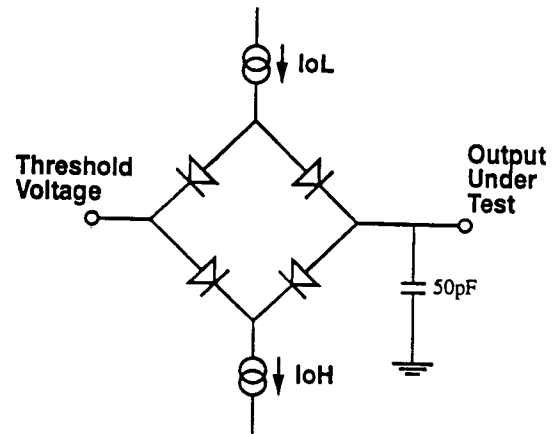


Figure 4. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 4.5V$ to $5.5V$ (Z87010)

| Symbol | Parameter | Condition | $T_A = -20^\circ C$ to $+70^\circ C$ | | Units |
|----------|---------------------------------|---|--------------------------------------|-----|---------|
| | | | Min | Max | |
| I_{DD} | Supply Current | $V_{DD}=5.5V$ $f_{clock}=16.384$ MHz | | 40 | mA |
| I_{DC} | DC Power Consumption | $V_{DD}=5.5V$ | | 0.2 | mA |
| V_{IH} | Input High Level | | 2.7 | | V |
| V_{IL} | Input Low Level | | | 0.8 | V |
| I_L | Input Leakage | | | 10 | μA |
| V_{OH} | Output High Voltage | $I_{OH}=-100\mu A$ | $V_{DD}-0.2$ | | V |
| V_{OL} | Output Low Voltage | $I_{OL}=2.0$ mA | | 0.5 | V (1) |
| I_{FL} | Output Floating Leakage Current | | | 10 | μA |

Note:

5. The following specifications are pin specific: EA0-2 has $I_{OL} = 5$ mA @ 0.5V
6. $I_{OH} = 1$ mA @ 3.3V

$V_{DD} = 3.0V$ to $3.6V$ (Z87L10)

| Symbol | Parameter | Condition | $T_A = -20^\circ C$ to $+70^\circ C$ | | Units |
|----------|---------------------------------|---|--------------------------------------|-------------|---------|
| | | | Min | Max | |
| I_{DD} | Supply Current | $V_{DD}=3.6V$ $f_{clock}=16.384$ MHz | | 25 | mA |
| I_{DC} | DC Power Consumption | $V_{DD}=3.6V$ | | 0.2 | mA |
| V_{IH} | Input High Level | | $.7V_{DD}$ | $V_{DD}+.3$ | V |
| V_{IL} | Input Low Level | | $V_{SS}-.3$ | $.1V_{DD}$ | V |
| I_L | Input Leakage | | | 10 | μA |
| V_{OH} | Output High Voltage | $I_{OH}=-50\mu A$ | $V_{DD}-0.2$ | | V |
| V_{OL} | Output Low Voltage | $I_{OL}=1.0$ mA | | 0.5 | V (1) |
| I_{FL} | Output Floating Leakage Current | | | 10 | μA |

Note:

7. The following specifications are pin specific: EA0-2 has $I_{OL} = 5$ mA @ 0.5V
8. $I_{OH} = 1$ mA @ 3.3V

AC ELECTRICAL CHARACTERISTICS

)

| Symbol | Parameter | $T_A = -20^\circ\text{C to } +70^\circ\text{C}$ | |
|--------|-------------------------------|---|----------|
| | | Min (ns) | Max (ns) |
| TCY | Clock Cycle Time | 50 | - |
| PWW | Clock Pulse Width | 23 | - |
| Tr | Clock Rise Time | - | 2 |
| Tf | Clock Fall Time | - | 2 |
| TEAD | EA, ER/W Delay from CK | 5 | 28 |
| TXVD | EXT Data Output Valid from CK | 5 | 33 |
| TXWH | EXT Data Output Hold from CK | 3 | 25 |
| TXRS | EXT Data Input Setup Time | 10 | - |
| TXRH | EXT Data Input Hold from CK | 10 | 25 |
| TIEDR | /EI Delay Time from CK | 3 | 15 |
| TIEDF | | 0 | 15 |
| RDYS | Ready Setup Time | 8 | - |
| RDYH | Ready Hold Time | 5 | - |
| TINS | Int. Setup Time to CLK Fall | 3 | - |
| TINL | Int. Low Pulse Width | 10 | - |
| THS | Halt Setup Time to CLK Rise | 3 | - |
| THH | Halt Hold Time to CLK Rise | 10 | - |

AC TIMING DIAGRAMS

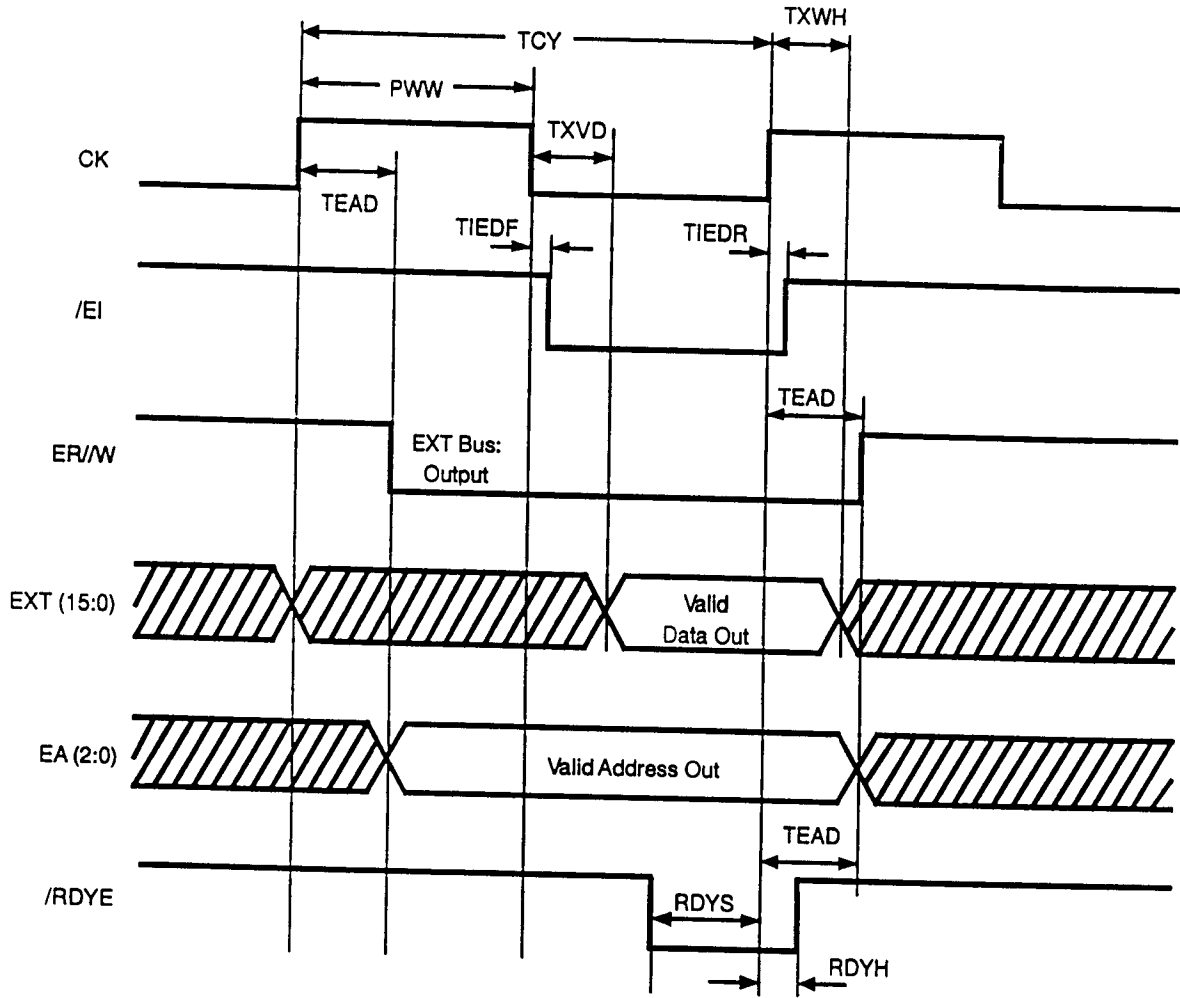


Figure 5. Write to External Device Timing

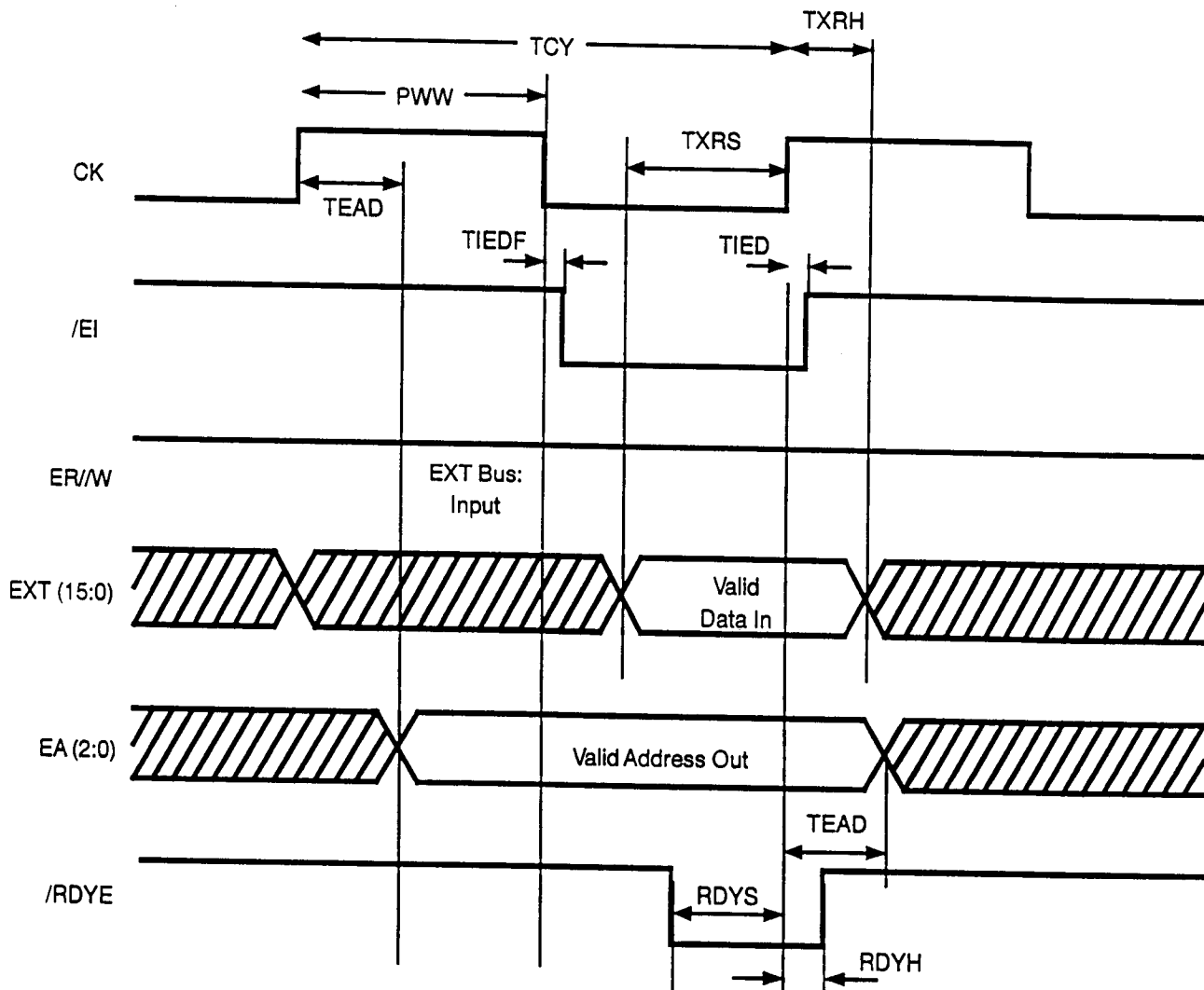


Figure 6. Read From External Device Timing

AC TIMING DIAGRAMS (Continued)

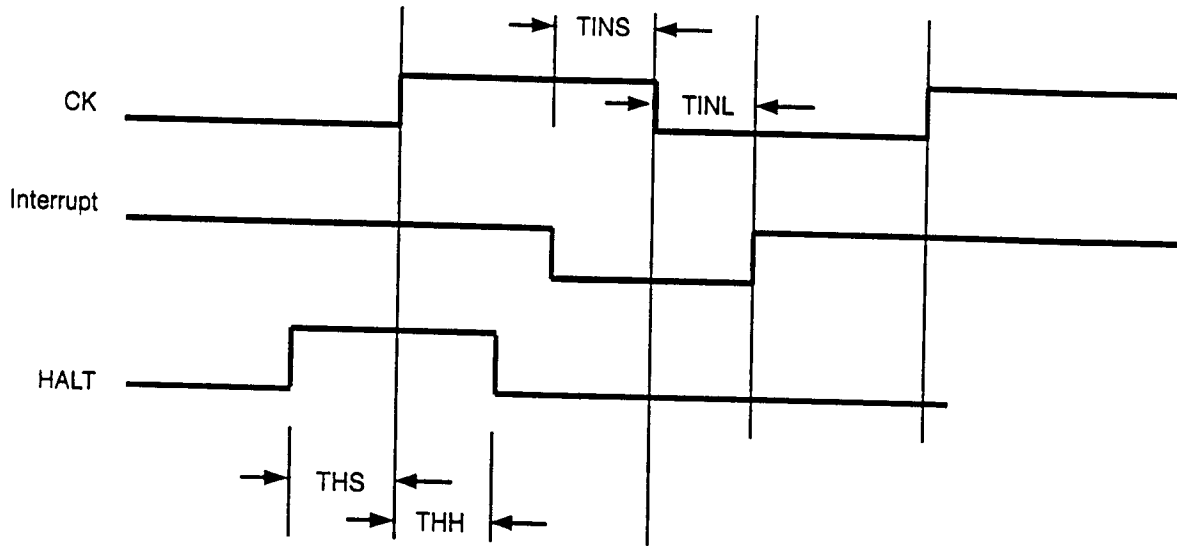


Figure 7. Interrupt/HALT Timing

Table 3. CODEC Interface-AC Timing

| Internal SCLK | | Min | Max |
|---------------|--|-----|-----|
| SDCR | SCLK down from CLK rise | - | 15 |
| SUCR | SCLK up from CLK rise | - | 15 |
| FDCR | FS0, FS1 down from SCLK rise | - | 6 |
| FUCR | FS0, FS1 up from SCLK rise | - | 6 |
| TDSR | TXD down from SCLK rise | - | 7 |
| TUSR | TXD up from SCLK rise | - | 7 |
| RSU | RXD Setup time in respect to SCLK fall | 7 | |
| RH | RXD Hold time in respect to SCLK fall | 0 | |
| FDCR | FS0,FS1 down from SCLK rise | - | 13 |
| FUCR | FS0, FS1 up from SCLK rise | - | 13 |
| TDSR | TXD down from SCLK rise | - | 12 |
| TUSR | TXD up from SCLK rise | - | 12 |
| RSU | RXD setup time in respect to SCLK fall | 1 | |
| RH | RXD Hold Time in respect to SCLK fall | 6 | |

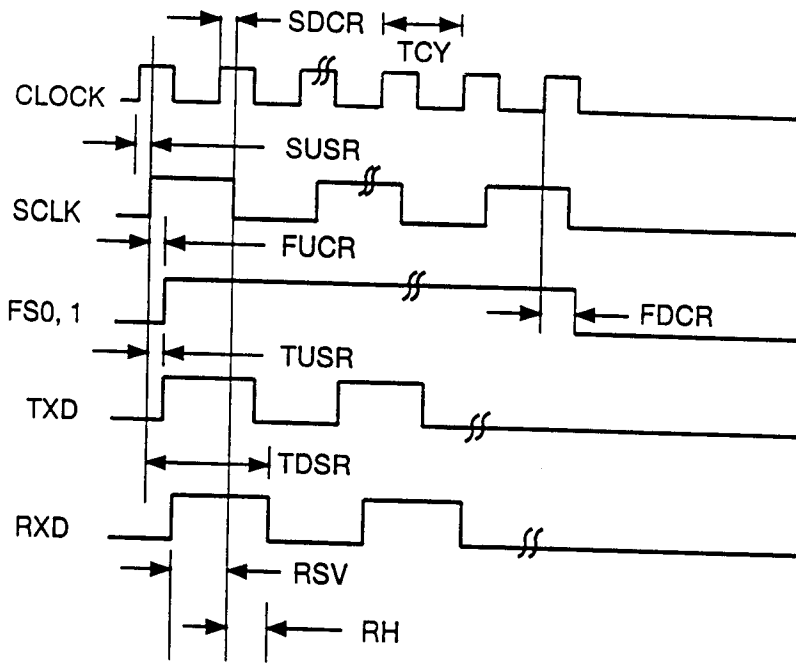


Figure 8. CODEC Interface Timing

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