2N3771, 2N3772

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

	Symbol	Min	Max	Unit
		•	•	•
2N3771 2N3772	V _{CEO(sus)}	40 60	- -	Vdc
2N3771 2N3772	V _{CEX(sus)}	50 80	- -	Vdc
2N3771 2N3772	V _{CER(sus)}	45 70	- -	Vdc
2N3771 2N3772	I _{CEO}	- -	10 10	mAdc
2N3771 2N3772 2N6257 2N3771 2N3772	I _{CEV}	- - - -	2.0 5.0 4.0 10	mAdc
2N3771 2N3772	I _{CBO}	- -	2.0 5.0	mAdc
2N3771 2N3772	I _{EBO}	- -	5.0 5.0	mAdc
2N3771 2N3772 2N3771 2N3772	h _{FE}	15 15 5.0 5.0	60 60 - -	-
2N3771 2N3772 2N3771 2N3772	V _{CE(sat)}	- - - -	2.0 1.4 4.0 4.0	Vdc
2N3771 2N3772	V _{BE(on)}	- -	2.7 2.2	Vdc
	f _T	0.2	-	MHz
	h _{fe}	40	-	-
				_
epetitive) 2N3771 2N3772	I _{S/b}	3.75 2.5	- -	Adc
	2N3772 2N3771 2N3772	2N3771	2N3771	2N3771

Indicates JEDEC registered data.
 Pulse Test: 300 μs, Rep. Rate 60 cps.

2N3771, 2N3772

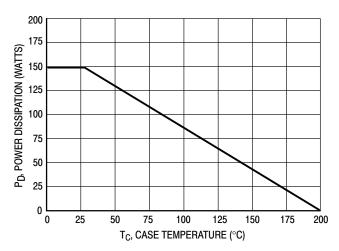


Figure 1. Power Derating

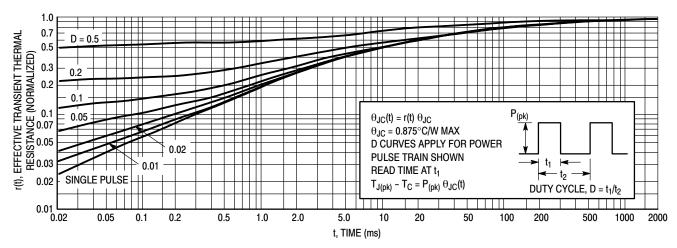


Figure 2. Thermal Response — 2N3771, 2N3772

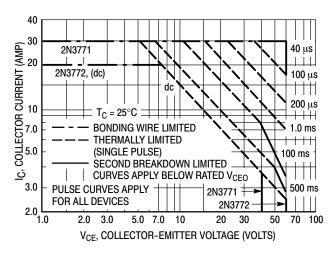
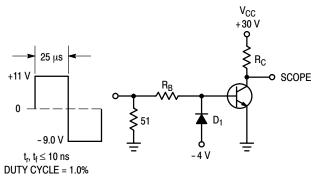


Figure 3. Active-Region Safe Operating Area — 2N3771, 2N3772

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}$ C. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

2N3771, 2N3772



R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, e.g.: 1N5825 USED ABOVE I $_B\approx 100$ mA MSD6100 USED BELOW I $_B\approx 100$ mA

Figure 4. Switching Time Test Circuit

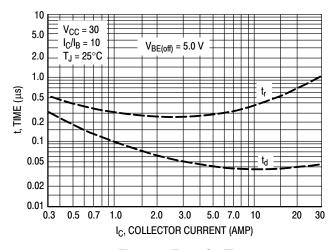


Figure 5. Turn-On Time

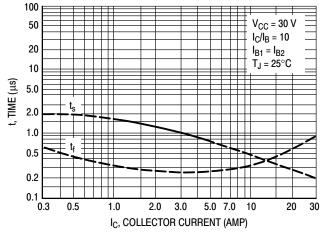


Figure 6. Turn-Off Time

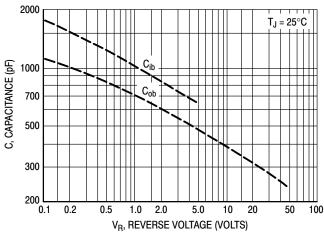


Figure 7. Capacitance

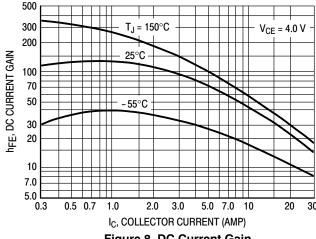


Figure 8. DC Current Gain

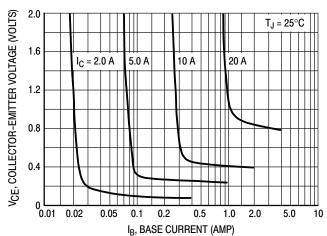
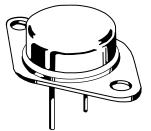


Figure 9. Collector Saturation Region

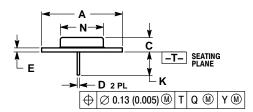


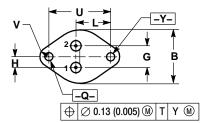


TO-204 (TO-3) **CASE 1-07 ISSUE Z**

DATE 05/18/1988







- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
 ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.550 REF		39.37 REF		
В		1.050		26.67	
С	0.250	0.335	6.35	8.51	
D	0.038	0.043	0.97	1.09	
Е	0.055	0.070	1.40	1.77	
G	0.430 BSC		10.92 BSC		
Н	0.215 BSC		5.46 BSC		
K	0.440	0.480	11.18	12.19	
L	0.665 BSC		16.89 BSC		
N		0.830		21.08	
Q	0.151	0.165	3.84	4.19	
U	1.187 BSC		30.15 BSC		
٧	0.131	0.188	3.33	4.77	

STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR	STYLE 2: PIN 1. BASE 2. COLLECTOR CASE: EMITTER	STYLE 3: PIN 1. GATE 2. SOURCE CASE: DRAIN	STYLE 4: PIN 1. GROUND 2. INPUT CASE: OUTPUT	STYLE 5: PIN 1. CATHODE 2. EXTERNAL TRIP/DELAY CASE: ANODE
STYLE 6:	STYLE 7:	STYLE 8:	STYLE 9:	
PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE #1	PIN 1. ANODE #1	
2. EMITTER	2. OPEN	2. CATHODE #2	2. ANODE #2	
CASE: COLLECTOR	CASE: CATHODE	CASE: ANODE	CASE: CATHODE	

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