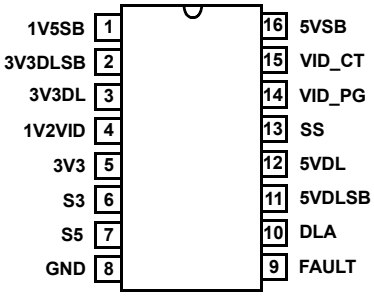
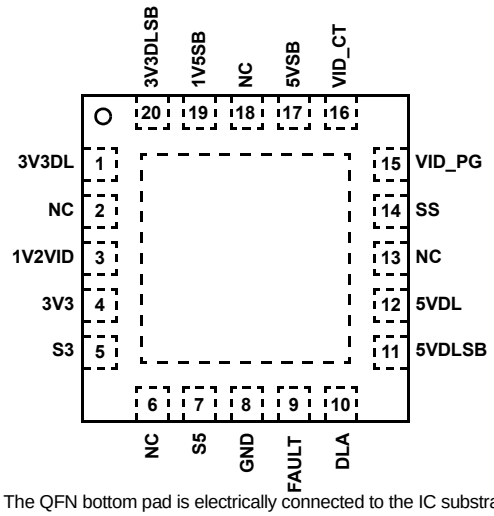
Pinouts

ISL6504/A (WIDE BODY SOIC)
TOP VIEW



NOTE: SOIC layout should accomodate both wide and narrow footprints.

ISL6504/A (6x6 QFN)
TOP VIEW



NOTE: The QFN bottom pad is electrically connected to the IC substrate, at GND potential. It can be left unconnected, or connected to GND; do NOT connect to another potential.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL6504CB	0 to 70	16 Ld SOIC	M16.3
ISL6504CBZ (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.3
ISL6504CBN	0 to 70	16 Ld SOIC	M16.15
ISL6504CBNZ (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
ISL6504CR	0 to 70	20 Ld 6x6 QFN	L20.6x6
ISL6504CRZ (Note)	0 to 70	20 Ld 6x6 QFN (Pb-free)	L20.6x6
ISL6504EVAL1	Evaluation Board		
ISL6504ACB	0 to 70	16 Ld SOIC	M16.3
ISL6504ACBZ (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.3
ISL6504ACBN	0 to 70	16 Ld SOIC	M16.15
ISL6504ACBNZ (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
ISL6504ACR	0 to 70	20 Ld 6x6 QFN	L20.6x6
ISL6504ACRZ (Note)	0 to 70	20 Ld 6x6 QFN (Pb-free)	L20.6x6
ISL6504AEVAL1	Evaluation Board		

Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram

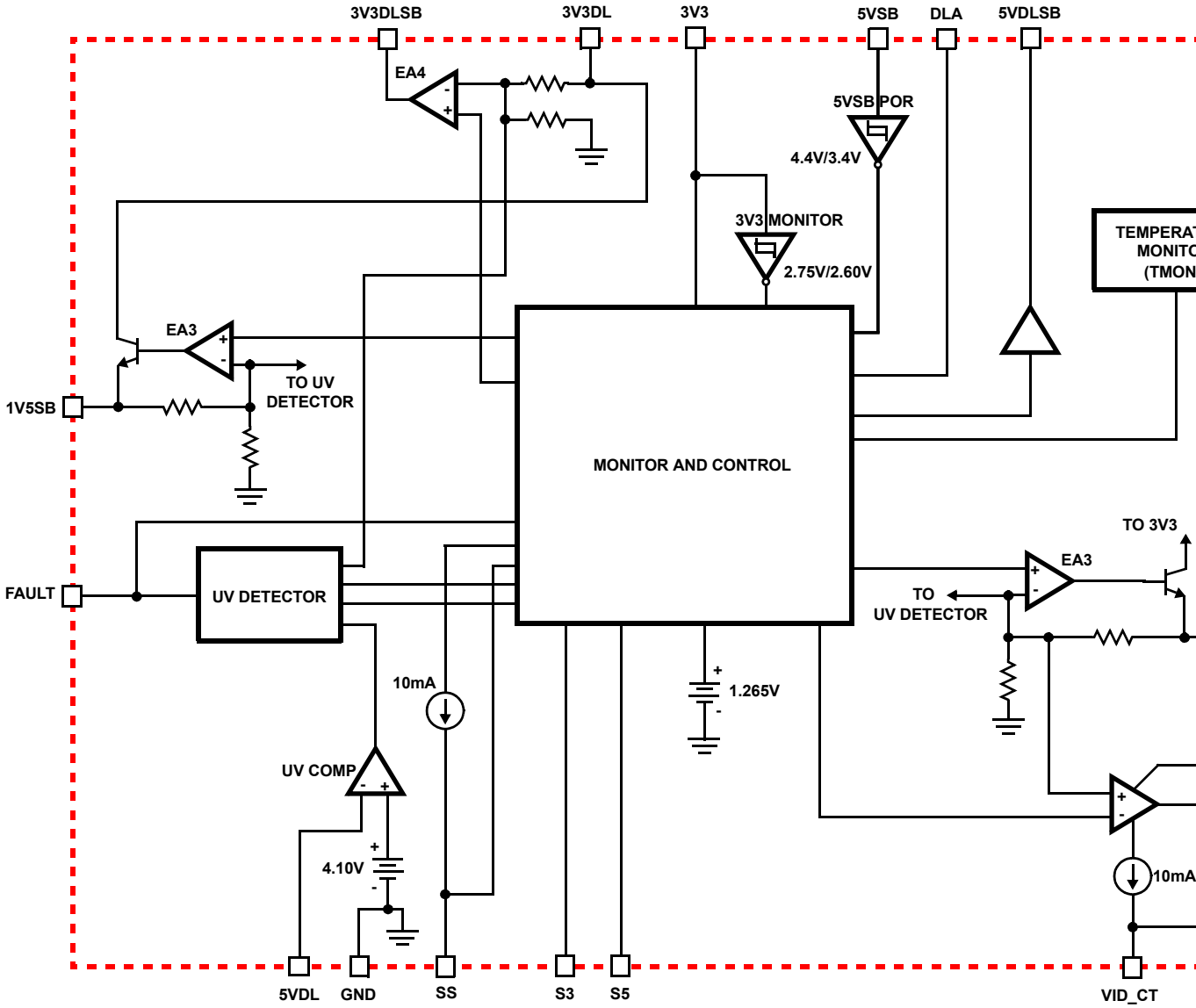


FIGURE 1.

Simplified Power System Diagram

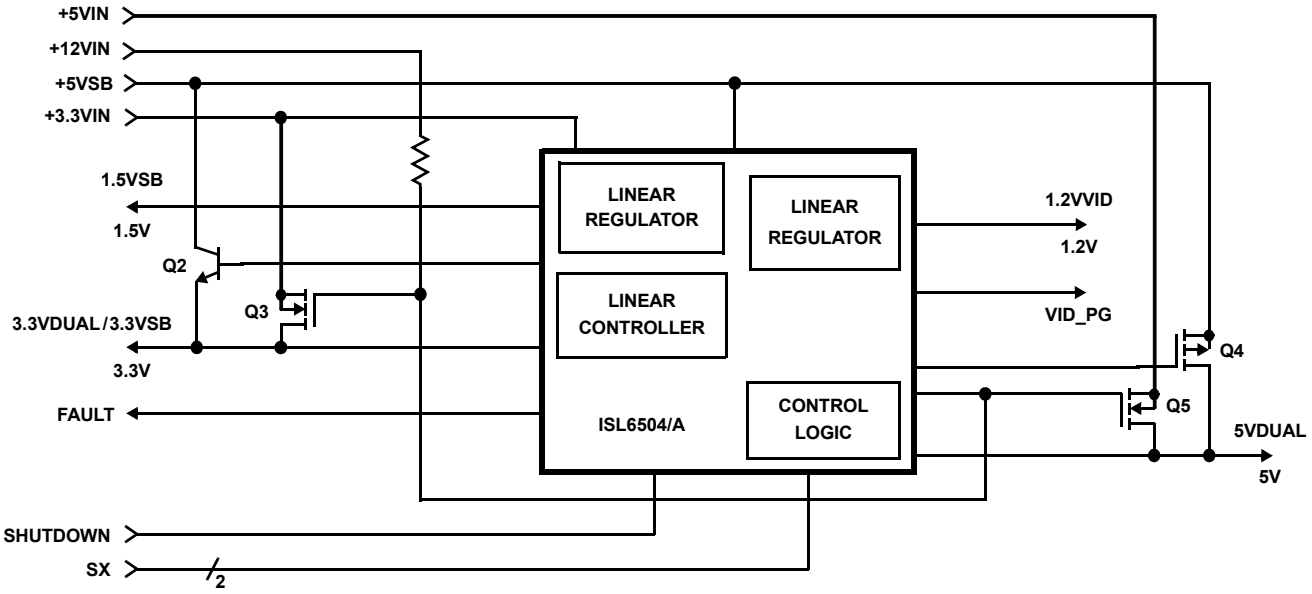


FIGURE 2.

Typical Application

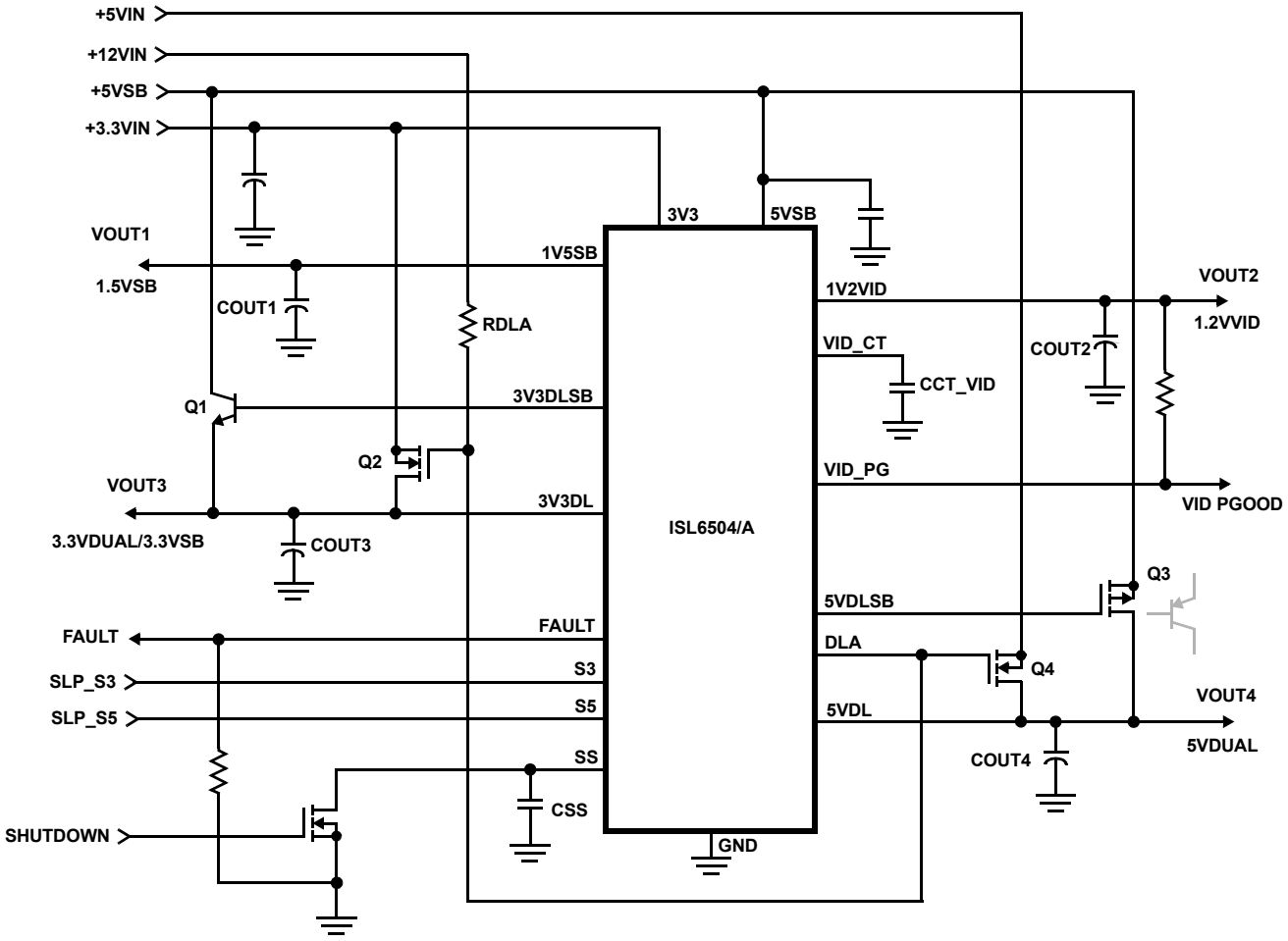


FIGURE 3.

Absolute Maximum Ratings

Supply Voltage, V_{5VSB} . . . . . +7.0V
DLA . . . . . GND - 0.3V to +14.5V
All Other Pins . . . . . + 7.0V
ESD Classification (Human Body Model) 2kV

Recommended Operating Conditions

Supply Voltage, V_{5VSB} . . . . . +5V ±5%
Lowest 5VSB Supply Voltage Guaranteeing Parameters . . . . +4.5V
Digital Inputs, $V_{\overline{Sx}}$ . . . . . .0 to +5.5V
Ambient Temperature Range. . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package (Note 1)	70	N/A
QFN Package (Note 2)	32	4.0

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)
For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC}, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{5VSB}		-	17	-	mA
Shutdown Supply Current	$I_{5VSB(OFF)}$	V_{SS} = 0.8V	-	4	-	mA
POWER-ON RESET, SOFT-START, AND VOLTAGE MONITORS						
Rising 5VSB POR Threshold			-	-	4.5	V
5VSB POR Hysteresis			-	0.9	-	V
Rising 3V3 Threshold			-	2.75	-	V
3V3 Hysteresis			-	150	-	mV
Falling Threshold Timeout (All Monitors)			-	10	-	µs
Soft-Start Current	I_{SS}		-	10	-	µA
Shutdown Voltage Threshold	V_{SD}		-	-	0.8	V
VID_PG Rising Threshold			-	1.02	-	V
VID_PG Hysteresis			-	56	-	mV
1.5V_{SB} LINEAR REGULATOR (V_{OUT1})						
Regulation			-	-	2.0	%
1V5SB Nominal Voltage Level	V_{1V5SB}		-	1.5	-	V
1V5SB Undervoltage Rising Threshold			-	1.25	-	V
1V5SB Undervoltage Hysteresis			-	75	-	mV
1V5SB Output Current	I_{1V5SB}	V_{3V3DL} = 3.3V	85	-	-	mA
1.2V_{VID} LINEAR REGULATOR (V_{OUT2})						
Regulation			-	-	2.0	%
1V2VID Nominal Voltage Level	V_{1V2VID}		-	1.2	-	V
1V2VID Undervoltage Rising Threshold			-	0.96	-	V
1V2VID Undervoltage Hysteresis			-	60	-	mV
1V2VID Output Current	I_{1V2VID}	V_{3V3} = 3.3V	40	-	-	mA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$3.3V_{DUAL}/3.3V_{SB}$ LINEAR REGULATOR (V_{OUT3})						
Sleep State Regulation			-	-	2.0	%
3V3DL Nominal Voltage Level	V_{3V3DL}		-	3.3	-	V
3V3DL Undervoltage Rising Threshold			-	2.75	-	V
3V3DL Undervoltage Hysteresis			-	150	-	mV
3V3DLSB Output Drive Current	$I_{3V3DLSB}$	V_{5VSB} = 5V	5	8	-	mA
$5V_{DUAL}$ SWITCH CONTROLLER (V_{OUT4})						
5VDL Undervoltage Rising Threshold			-	4.10	-	V
5VDL Undervoltage Hysteresis			-	200	-	mV
5VDLSB Output Drive Current	I_{5VDLSB}	V_{5VDLSB} = 4V, V_{5VSB} = 5V	-20	-	-40	mA
TIMING INTERVALS						
Active State Assessment Past Input UV Thresholds (Note 3)			20	25	30	ms
Active-to-Sleep Control Input Delay			-	200	-	µs
VID_CT Charging Current	I_{VID_CT}	V_{VID_CT} = 0V	-	10	-	µA
CONTROL I/O ($\overline{S3}$, $\overline{S5}$, FAULT)						
High Level Input Threshold			-	-	2.2	V
Low Level Input Threshold			0.8	-	-	V
$\overline{S3}$, $\overline{S5}$ Internal Pull-up Impedance to 5VSB			-	50	-	kΩ
FAULT Output Impedance		FAULT = high	-	100	-	Ω
TEMPERATURE MONITOR						
Fault-Level Threshold (Note 4)			125	-	-	^oC
Shutdown-Level Threshold (Note 4)			-	155	-	^oC

NOTES:

3. Guaranteed by Correlation.
4. Guaranteed by Design.

Functional Pin Description (SOIC pinout)

3V3 (Pin 5)

Connect this pin to the ATX 3.3V output. This pin provides the output current for the 1V2VID pin, and is monitored for power quality.

5VSB (Pin 16)

Provide a very well de-coupled 5V bias supply for the IC to this pin by connecting it to the ATX $5V_{SB}$ output. This pin provides all the chip's bias as well as the base current for Q2 (see typical application diagram). The voltage at this pin is monitored for power-on reset (POR) purposes.

GND (Pin 8)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

$\overline{S3}$ and $\overline{S5}$ (Pins 6 and 7)

These pins switch the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states. These are digital inputs featuring internal 50kΩ (typical) resistor pull-ups to 5VSB. Internal circuitry de-glitches these pins for disturbances lasting as long as 2μs (typically). Additional circuitry blocks any illegal state transitions (such as S3 to S4/S5 or vice versa). Respectively, connect $\overline{S3}$ and $\overline{S5}$ to the computer system's $\overline{SLP\_S3}$ and $\overline{SLP\_S5}$ signals.

FAULT (Pin 9)

In case of an undervoltage on any of the controlled outputs, on any of the monitored ATX voltages, or in case of an overtemperature event, this pin is used to report the fault condition by being pulled to 5VSB. Connect a 1kΩ resistor from this pin to GND.

SS (Pin 13)

Connect this pin to a small ceramic capacitor (no less than 5nF; 0.1μF recommended). The internal soft-start (SS) current source along with the external capacitor creates a voltage ramp used to control the ramp-up of the output voltages. Pulling this pin low with an open-drain device shuts down all the outputs as well as force the FAULT pin low. The C_{SS} capacitor is also used to provide a controlled voltage slew rate during active-to-sleep transitions on the $3.3V_{DUAL}/3.3V_{SB}$ output.

3V3DL (Pin 3)

Connect this pin to the 3.3V dual/stand-by output (V_{OUT3}). In sleep states, the voltage at this pin is regulated to 3.3V; in active states, ATX 3.3V output is delivered to this node through a fully-on N-MOS transistor. During all operating states, this pin is monitored for undervoltage events. This pin provides all the output current delivered by the 1V5SB pin.

3V3DLSB (Pin 2)

Connect this pin to the base of a suitable NPN transistor. In sleep state, this transistor is used to regulate the voltage at the 3V3DL pin to 3.3V.

DLA (Pin 10)

This pin is an open-collector output. Connect a 1kΩ resistor from this pin to the ATX 12V output. This resistor is used to pull the gates of suitable N-MOSFETs to 12V, which in active state, switch in the ATX 3.3V and 5V outputs into the $3.3V_{DUAL}/3.3V_{SB}$ and $5V_{DUAL}$ outputs, respectively.

5VDL (Pin 12)

Connect this pin to the $5V_{DUAL}$ output (V_{OUT4}). In either operating state (when on), the voltage at this pin is provided through a fully-on MOS transistor. This pin is also monitored for undervoltage events.

5VDLSB (Pin 11)

Connect this pin to the gate of a suitable P-MOSFET or bipolar PNP. ISL6504: In S3 sleep state, this transistor is switched on, connecting the ATX $5V_{SB}$ output to the $5V_{DUAL}$ regulator output. ISL6504A: In S3 and S4/S5 sleep state, this transistor is switched on, connecting the ATX $5V_{SB}$ output to the $5V_{DUAL}$ regulator output.

1V5SB (Pin 1)

This pin is the output of the internal 1.5V regulator (V_{OUT1}). This internal regulator operates for as long as $5V_{SB}$ is applied to the IC and draws its output current from the 3V3DL pin. This pin is monitored for undervoltage events.

1V2VID (Pin 4)

This pin is the output of the internal 1.2V voltage identification (VID) regulator (V_{OUT2}). This internal regulator operates only in active states (S0, S1/S2) and is shut off during any sleep state. This regulator draws its output current from the 3V3 pin. This pin is monitored for undervoltage events.

VID_PG (Pin 14)

This pin is the open collector output of the 1V2VID power good comparator. Connect a 10kΩ pull-up resistor from this pin to the 1V2VID output. As long as the 1V2VID output is below its UV threshold, this pin is pulled low.

VID_CT (Pin 15)

Connect a small capacitor from this pin to ground. The capacitor is used to delay the VID_PG reporting the 1V2VID has reached power good limits.

Description

Operation

The ISL6504/A controls 4 output voltages (Refer to Figures 1, 2, and 3). It is designed for microprocessor computer applications with 3.3V, 5V, $5V_{SB}$, and 12V bias input from an ATX power supply. The IC is composed of three linear controllers/regulators supplying the computer system's $1.5V_{SB}$ (V_{OUT1}), $3.3V_{SB}$ and PCI slots' $3.3V_{AUX}$ power (V_{OUT3}), the 1.2V VID circuitry power (V_{OUT2}), a dual switch controller supplying the $5V_{DUAL}$ voltage (V_{OUT4}), as

well as all the control and monitoring functions necessary for complete ACPI implementation.

Initialization

The ISL6504/A automatically initializes upon receipt of input power. The Power-On Reset (POR) function continually monitors the $5V_{SB}$ input supply voltage, initiating $3.3V_{DUAL}/3.3V_{SB}$ and $1.5V_{SB}$ soft-start operation shortly after exceeding POR threshold.

Dual Outputs Operational Truth Table

Table 1 describes the truth combinations pertaining to the $3.3V_{DUAL/SB}$ and $5V_{DUAL}$ outputs. The last two lines highlight the only difference between the ISL6504 and ISL6504A. The internal circuitry does not allow the transition from an S3 (suspend to RAM) state to an S4/S5 (suspend to disk/soft off) state or vice versa. The only 'legal' transitions are from an active state (S0, S1) to a sleep state (S3, S5) and vice versa.

TABLE 1. $5V_{DUAL}$ OUTPUT (V_{OUT4}) TRUTH TABLE

$\overline{S5}$	$\overline{S3}$	3.3VDL/SB	5VDL	COMMENTS
1	1	3.3V	5V	S0/S1/S2 States (Active)
1	0	3.3V	5V	S3
0	1	Note		Maintains Previous State
0	0	3.3V	0V	S4/S5 (ISL6504)
0	0	3.3V	5V	S4/S5 (ISL6504A)

NOTE: Combination Not Allowed.

Functional Timing Diagrams

Figures 4 (ISL6504), 5 (ISL6504A), and 6 are timing diagrams, detailing the power up/down sequences of all the outputs in response to the status of the sleep-state pins ($\overline{S3}$, $\overline{S5}$), as well as the status of the input ATX supply. Not shown in these diagrams is the deglitching feature used to protect against false sleep state tripping. Both $\overline{S3}$ and $\overline{S5}$ pins are protected against noise by a 2µs filter (typically 1–4µs). This feature is useful in noisy computer environments if the control signals have to travel over significant distances. Additionally, the $\overline{S3}$ pin features a 200µs delay in transitioning to sleep states. Once the $\overline{S3}$ pin goes low, an internal timer is activated. At the end of the 200µs interval, if the $\overline{S5}$ pin is low, the ISL6504/A switches into S5 sleep state; if the $\overline{S5}$ pin is high, the ISL6504/A goes into S3 sleep state.

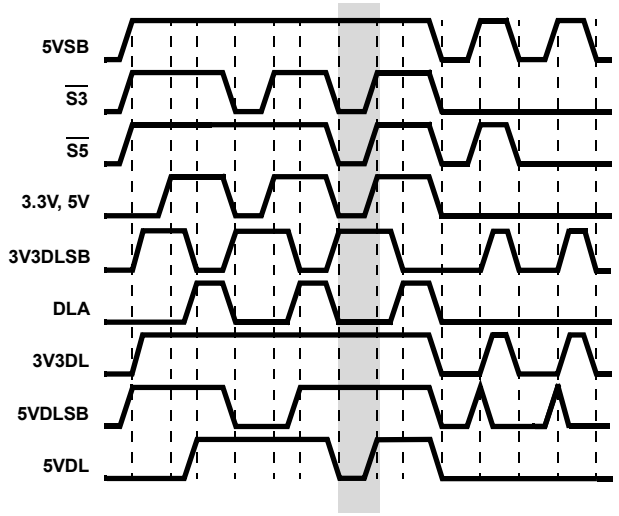


FIGURE 4. $5V_{DUAL}$ AND $3.3V_{DUAL}/3.3V_{SB}$ TIMING DIAGRAM; ISL6504

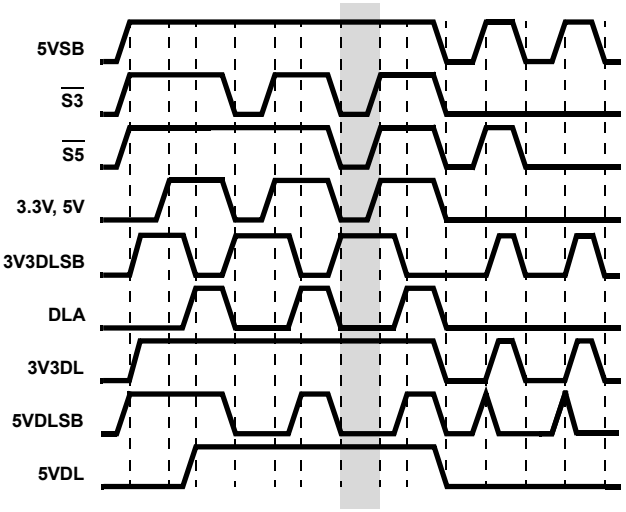


FIGURE 5. $5V_{DUAL}$ AND $3.3V_{DUAL}/3.3V_{SB}$ TIMING DIAGRAM; ISL6504A

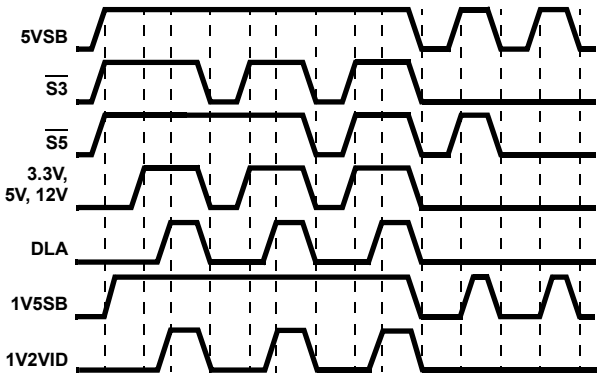


FIGURE 6. $1.5V_{SB}$, AND $1.2V_{VID}$ TIMING DIAGRAM

Soft-Start into Sleep States (S3, S4/S5)

The $5V_{SB}$ POR function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor. The error amplifiers reference inputs are clamped to a level proportional to the SS (soft-start) pin voltage. As the SS pin voltage slews from about 1.25V to 2.5V, the input clamp allows a rapid and controlled output voltage rise.

Figures 7 (ISL6504) and 8 (ISL6504A) show the soft-start sequence for the typical application start-up into a sleep state. At time T0 $5V_{SB}$ (bias) is applied to the circuit. At time T1, the $5V_{SB}$ surpasses POR level. An internal fast charge circuit quickly raises the SS capacitor voltage to approximately 1V, then the 10µA current source continues the charging.

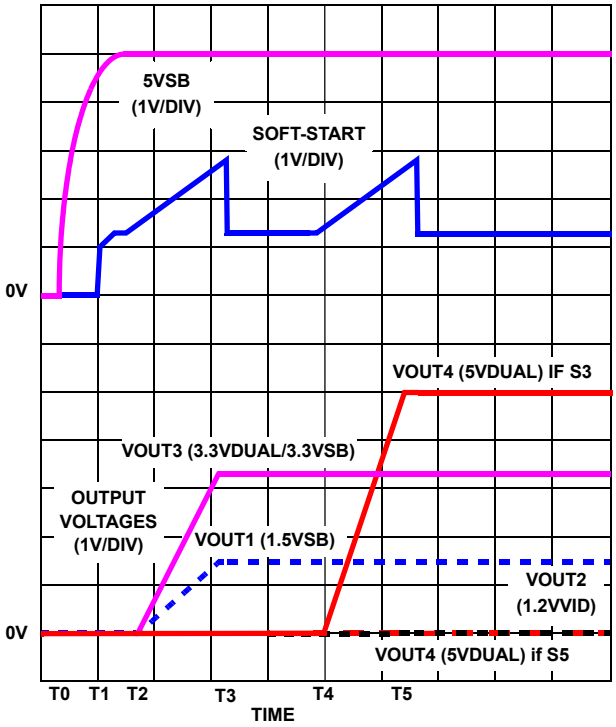


FIGURE 7. SOFT-START INTERVAL IN A SLEEP STATE; ISL6504

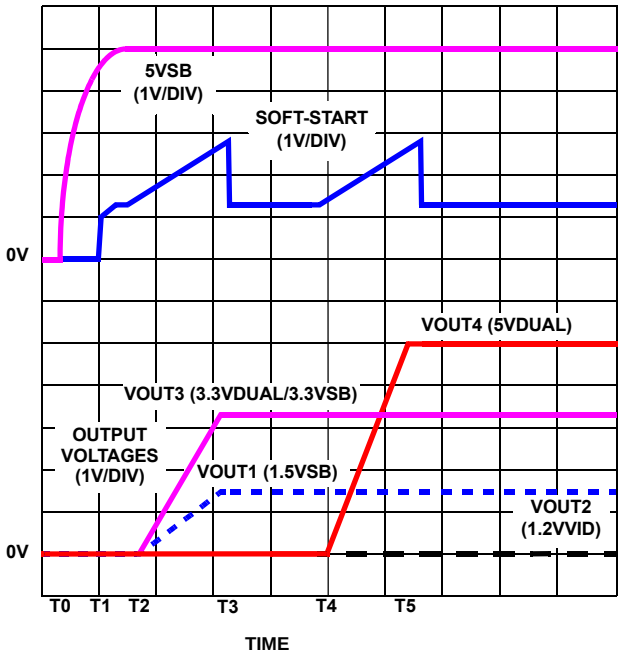


FIGURE 8. SOFT-START INTERVAL IN A SLEEP STATE; ISL6054A

The soft-start capacitor voltage reaches approximately 1.25V at time T2, at which point the $3.3V_{DUAL}/3.3V_{SB}$ and $1.5V_{SB}$ error amplifiers' reference inputs start their transition, resulting in the output voltages ramping up proportionally. The ramp-up continues until time T3 when the two voltages reach the set value. As the soft-start capacitor voltage reaches approximately 2.75V, the undervoltage monitoring circuit of this output is activated and the soft-start capacitor is quickly discharged to approximately 1.25V. Following the 3ms (typical) time-out between T3 and T4, the soft-start capacitor commences a second ramp-up designed to smoothly bring up the remainder of the voltages required by the system. At time T5, voltages are within regulation limits, and as the SS voltage reaches 2.75V, all the remaining UV monitors are activated and the SS capacitor is quickly discharged to 1.25V, where it remains until the next transition. As the $1.2V_{VID}$ output is only active while in an active state, it does not come up, but rather waits until the main ATX outputs come up within regulation limits.

Soft-Start into Active States (S0, S1)

If both $\overline{S3}$ and $\overline{S5}$ are logic high at the time the $5V_{SB}$ is applied, the ISL6504/A will assume active state wake-up and keep off the required outputs until some time (typically 25ms) after the monitored main ATX output (3.3V) exceeds the set threshold. This time-out feature is necessary in order to ensure the main ATX outputs are stabilized. The time-out also assures smooth transitions from sleep into active when sleep states are being supported. $3.3V_{DUAL}/3.3V_{SB}$ and $1.5V_{SB}$ outputs will come up right after bias voltage surpasses POR level.

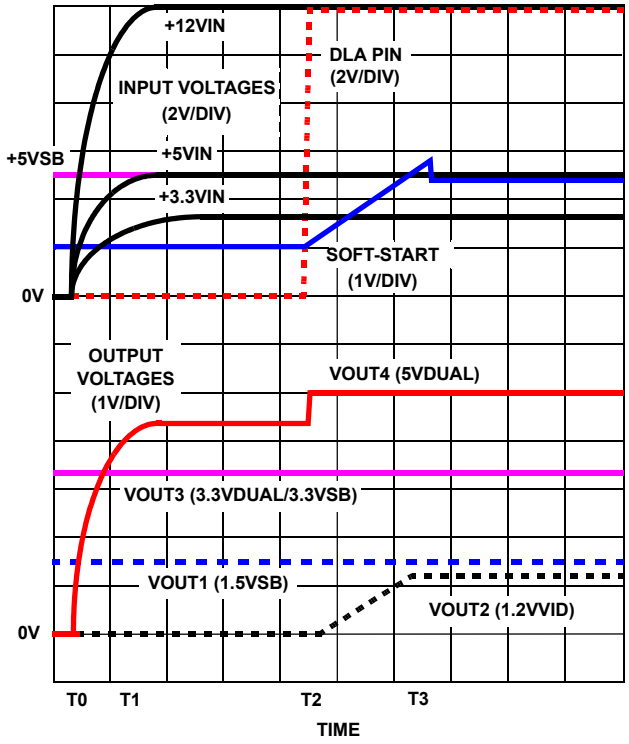


FIGURE 9. SOFT-START INTERVAL IN ACTIVE STATE

During sleep-to-active state transitions from conditions where the $5V_{DUAL}$ output is initially 0V (such as S5 to S0 transition, or simple power-up sequence directly into active state), the circuit goes through a quasi soft-start, the $5V_{DUAL}$ output being pulled high through the body diode of the N-Channel MOSFET connected between it and the 5V ATX. Figure 9 exemplifies this start-up case. $5V_{SB}$ is already present when the main ATX outputs are turned on, at time T0. As a result of $+5V_{IN}$ ramping up, the $5V_{DUAL}$ output capacitors charge up through the body diode of Q4 (see Typical Application). At time T1, all main ATX outputs exceed the ISL6504/A's undervoltage thresholds, and the internal 25ms (typical) timer is initiated. At T2, the time-out initiates a soft-start, and the 1.2V voltage ID output is ramped-up, reaching regulation limits at time T3. Simultaneous with the beginning of this ramp-up, at time T2, the DLA pin is released, allowing the pull-up resistor to turn on Q2 and Q4, and bring the $5V_{DUAL}$ output in regulation. Shortly after time T3, as the SS voltage reaches 2.75V, the soft-start capacitor is quickly discharged down to approximately 2.45V, where it remains until a valid sleep state request is received from the system.

Fault Protection

All the outputs are monitored against undervoltage events. A severe overcurrent caused by a failed load on any of the outputs, would, in turn, cause that specific output to suddenly drop. If any of the output voltages drops below 80% (typical) of their set value, such event is reported by having the FAULT pin pulled to 5V. Additionally, exceeding the maximum current rating of an integrated regulator (output with pass regulator on chip) can lead to output voltage drooping; if excessive, this droop can ultimately trip the undervoltage detector and send a FAULT signal to the computer system.

A FAULT condition occurring on an output when controlled through an external pass transistor will only set off the FAULT flag, and it will not shut off or latch off any part of the circuit. A FAULT condition occurring on an output controlled through an internal pass transistor, will set off the FAULT flag, and it will shut off the respective faulting regulator only. If shutdown or latch off of the entire circuit is desired in case of a fault, regardless of the cause, this can be achieved by externally pulling or latching the SS pin low. Pulling the SS pin low will also force the FAULT pin to go low and reset any internally latched-off output.

Special consideration is given to the initial start-up sequence. If, following a $5V_{SB}$ POR event, any of the $1.5V_{SB}$ or $3.3V_{DUAL}/3.3V_{SB}$ outputs is ramped up and is subject to an undervoltage event before the end of the second soft-start ramp, then the FAULT output goes high and the entire IC latches off. Latch-off condition can be reset by cycling the bias power ($5V_{SB}$). Undervoltage events on the $1.5V_{SB}$ and the $3.3V_{DUAL}/3.3V_{SB}$ outputs at any other times are handled according to the description found in the second paragraph under the current heading.

Another condition that could set off the FAULT flag is chip overtemperature. If the ISL6504/A reaches an internal temperature of $140^{o}C$ (typical), the FAULT flag is set, but the chip continues to operate until the temperature reaches $155^{o}C$ (typical), when unconditional shutdown of all outputs takes place. Operation resumes only after powering down the IC (to create a $5V_{SB}$ POR event) and a start-up (assuming the cause of the fault has been removed; if not, as it heats up again, it will repeat the FAULT cycle).

In ISL6504/A applications, loss of the active ATX output ($3.3V_{IN}$; as detected by the on-board voltage monitor) during active state operation causes the chip to switch to S5 sleep state, in addition to reporting the input UV condition on the FAULT pin. Exiting from this forced S5 state can only be achieved by returning the faulting input voltage above its UV threshold, by resetting the chip through removal of $5V_{SB}$ bias voltage, or by bringing the SS pin at a potential lower than 0.8V.

Application Guidelines

Soft-Start Interval

The $5V_{SB}$ output of a typical ATX supply is capable of 725mA, with newer models rated for 1.0A, and even 2.0A. During power-up in a sleep state, the $5V_{SB}$ ATX output needs to provide sufficient current to charge up all the applicable output capacitors and, simultaneously, provide some amount of current to the output loads. Drawing

excessive amounts of current from the $5V_{SB}$ output of the ATX can lead to voltage collapse and induce a pattern of consecutive restarts with unknown effects on the system's behavior or health.

The built-in soft-start circuitry allows tight control of the slew-up speed of the output voltages controlled by the ISL6504, thus enabling power-ups free of supply drop-off events. Since the outputs are ramped up in a linear fashion, the current dedicated to charging the output capacitors can be calculated with the following formula:

$$I_{COUT} = \frac{I_{SS}}{C_{SS} \times V_{BG}} \times \Sigma(C_{OUT} \times V_{OUT})$$, where

I_{SS} - soft-start current (typically 10µA)

C_{SS} - soft-start capacitor

V_{BG} - bandgap voltage (typically 1.26V)

$\Sigma(C_{OUT} \times V_{OUT})$ - sum of the products between the capacitance and the voltage of an output (total charge delivered to all outputs)

Due to the various system timing events and their interaction, it is recommended that the soft-start interval not be set to exceed 30ms. For most applications, a 0.1µF capacitor is recommended.

Shutdown

In case of a FAULT condition that might endanger the computer system, or at any other time, all the ISL6504/A outputs can be shut down by pulling the SS pin below the specified shutdown level (typically 0.8V) with an open drain or open collector device capable of sinking a minimum of 2mA. Pulling the SS pin low effectively shuts down all the pass elements. Upon release of the SS pin, the ISL6504 undergoes a new soft-start cycle and resumes normal operation in accordance to the ATX supply and control pins status.

VID_PG Delay

During power-up and initial soft-start, the VID_PG and VID_CT pins are held low. As the 1V2VID output exceeds its rising power-good threshold, the capacitor connected at the VID_CT pin starts to charge up through the internal 10µA current source. As the voltage on this capacitor exceeds 1.25V, the open-collector VID_PG pin is released and VID POWER GOOD status is thus reported.

The value of the VID_CT capacitor to be used to obtain a given VID_PG delay can be determined from the graph in Figure 10. For extended delays exceeding the range of the graph, use the following formula:

$$C = \frac{t_{DELAY}}{125000}$$, where

t_{DELAY} - desired delay time (s)

C - VID_CT capacitor to obtain desired delay time (F)

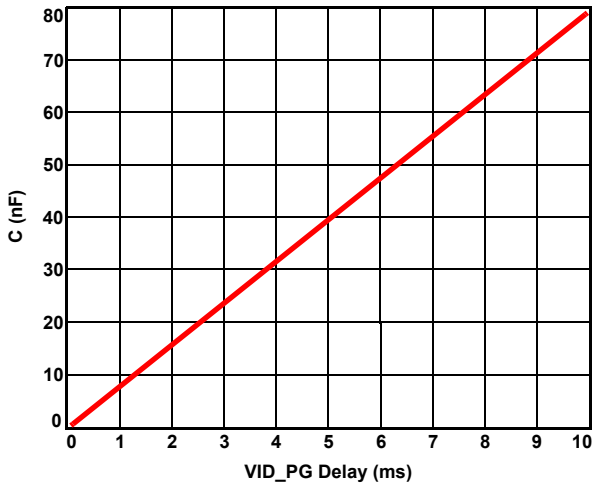


FIGURE 10. VID_PG DELAY DEPENDENCE ON VID_CT CAPACITOR

Layout Considerations

The typical application employing an ISL6504/A is a fairly straight forward implementation. Like with any other linear regulator, attention has to be paid to the few potentially sensitive small signal components, such as those connected to sensitive nodes or those supplying critical bypass current.

The power components (pass transistors) and the controller IC should be placed first. The controller should be placed in a central position on the motherboard, closer to the memory controller chip and processor, but not excessively far from the $3.3V_{DUAL}$ island or the I/O circuitry. Ensure the 1V5SB, 1V2VID, 3V3, and 3V3DL connections are properly sized to carry 100mA without exhibiting significant resistive losses at the load end. Similarly, the input bias supply ($5V_{SB}$) can carry a significant level of current - for best results, ensure it is connected to its respective source through an adequately sized trace. The pass transistors should be placed on pads capable of heatsinking matching the device's power dissipation. Where applicable, multiple via connections to a large internal plane can significantly lower localized device temperature rise.

Placement of the decoupling and bulk capacitors should follow a placement reflecting their purpose. As such, the high-frequency decoupling capacitors should be placed as close as possible to the load they are decoupling; the ones decoupling the controller close to the controller pins, the ones decoupling the load close to the load connector or the load itself (if embedded). Even though bulk capacitance (aluminum electrolytics or tantalum capacitors) placement is not as critical as the high-frequency capacitor placement, having these capacitors close to the load they serve is preferable.

The critical small signal components include the soft-start capacitor, C_{SS}, as well as all the high-frequency decoupling capacitors. Locate these components close to the respective

pins of the control IC, and connect them to ground through a via placed close to the ground pad. Minimize any leakage current paths from the SS node, as the internal current source is only 10µA (typical).

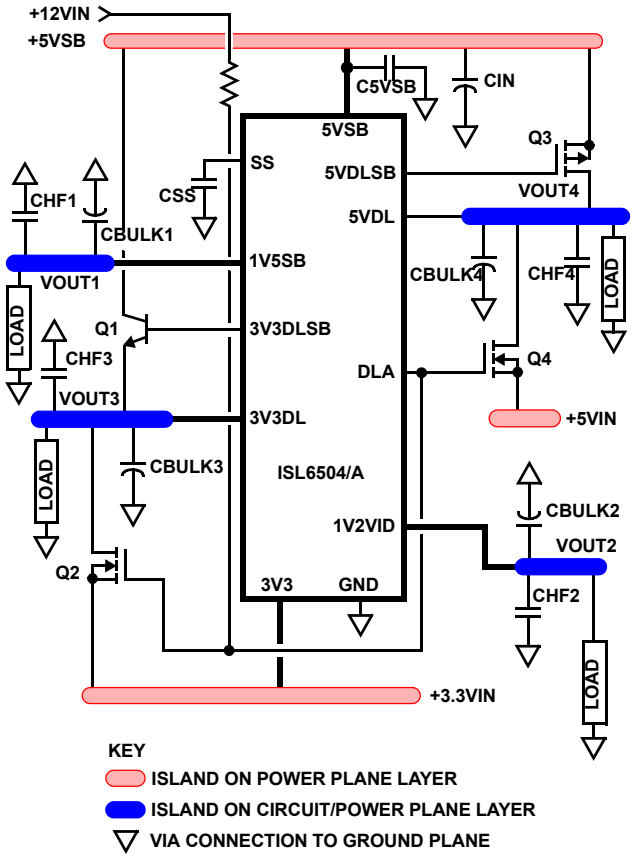


FIGURE 11. PRINTED CIRCUIT BOARD ISLANDS

A multi-layer printed circuit board is recommended. Figure 11 shows the connections to most of the components in the circuit. Note that the individual capacitors shown each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections through vias placed as close to the component terminal as possible. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Ideally, the power plane should support both the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers to create power islands connecting the filtering components (output capacitors) and the loads. Use the remaining printed circuit layers for small signal wiring.

Component Selection Guidelines

Output Capacitors Selection

The output capacitors should be selected to allow the output voltage to meet the dynamic regulation requirements of active state operation (S0, S1). The load transient for the various microprocessor system's components may require high quality capacitors to supply the high slew rate (di/dt) current demands. Thus, it is recommended that the output capacitors be selected for transient load regulation, paying attention to their parasitic components (ESR, ESL).

Also, during the transition between active and sleep states on the $3.3V_{DUAL}/3.3V_{SB}$ and $5V_{DUAL}$ outputs, there is a short interval of time during which none of the power pass elements are conducting - during this time the output capacitors have to supply all the output current. The output voltage drop during this brief period of time can be easily approximated with the following formula:

$$\Delta V_{OUT} = I_{OUT} \times \left(ESR_{OUT} + \frac{t_t}{C_{OUT}} \right), \text{ where}$$

ΔV_{OUT} - output voltage drop

ESR_{OUT} - output capacitor bank ESR

I_{OUT} - output current during transition

C_{OUT} - output capacitor bank capacitance

t_t - active-to-sleep or sleep-to-active transition time (10µs typ.)

The output voltage drop is heavily dependent on the ESR (equivalent series resistance) of the output capacitor bank, the choice of capacitors should be such as to maintain the output voltage above the lowest allowable regulation level.

Input Capacitors Selection

The input capacitors for an ISL6504/A application must have a sufficiently low ESR so as not to allow the input voltage to dip excessively when energy is transferred to the output capacitors. If the ATX supply does not meet the specifications, certain imbalances between the ATX's outputs and the ISL6504/A's regulation levels could have as a result a brisk transfer of energy from the input capacitors to the supplied outputs. At the transition between active and sleep states, such phenomena could be responsible for the $5V_{SB}$ voltage drooping excessively and affecting the output regulation. The solution to such a potential problem is using larger input capacitors with a lower total combined ESR.

Transistor Selection/Considerations

The ISL6504/A usually requires one P-Channel (or bipolar PNP), two N-Channel MOSFETs, and one bipolar NPN transistors.

One important criteria for selection of transistors for all the linear regulators/switching elements is package selection for efficient removal of heat. The power dissipated in a linear regulator or an ON/OFF switching element is

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the rating with the maximum expected ambient temperature.

Q1

The NPN transistor used as sleep state pass element on the $3.3V_{DUAL}$ output has to have a minimum current gain of 100 at 1.5V V_{CE} and 650mA I_{CE} throughout the in-circuit operating temperature range. For larger current ratings on the $3.3V_{DUAL}$ output (providing the ATX $5V_{SB}$ output rating is equally extended), selection criteria for Q1 include an appropriate current gain (h_{fe}) and saturation characteristics.

Q2, Q4

These N-Channel MOSFETs are used to switch the 3.3V and 5V inputs provided by the ATX supply into the $3.3V_{DUAL}$/$3.3V_{SB}$ and $5V_{DUAL}$ outputs while in active (S0, S1) state. The main criteria for the selection of these transistors is output voltage budgeting. The maximum $r_{DS(ON)}$ allowed at highest junction temperature can be expressed with the following equation:

$$r_{DS(ON)max} = \frac{V_{INmin} - V_{OUTmin}}{I_{OUTmax}}, \text{ where}$$

V_{INmin} - minimum input voltage

V_{OUTmin} - minimum output voltage allowed

I_{OUTmax} - maximum output current

Q3

If a P-Channel MOSFET is used to switch the $5V_{SB}$ output of the ATX supply into the $5V_{DUAL}$ output during sleep states, then the selection criteria of this device is proper voltage budgeting. The maximum $r_{DS(ON)}$, however, has to be achieved with only 4.5V of gate-to-source voltage, so a logic level MOSFET needs to be selected. If a PNP device is chosen to perform this function, it has to have a low-saturation voltage while providing the maximum sleep current and have a current gain sufficiently high to be saturated using the minimum drive current (typically 20mA).

ISL6504 Application Circuit

Figure 12 shows a typical application circuit for the ISL6504/A. The circuit provides the $3.3V_{DUAL}$/$3.3V_{SB}$ voltage, the ICH4 resume well $1.5V_{SB}$ voltage, the $1.2V_{VID}$ voltage identification output, and the $5V_{DUAL}$ keyboard/mouse voltage from +3.3V, $+5V_{SB}$, +5V, and +12VDC ATX supply outputs. Q3 can also be a PNP transistor, such as an MMBT2907AL. For additional, more detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN1001. Also see Intersil Corporation's web page (www.intersil.com).

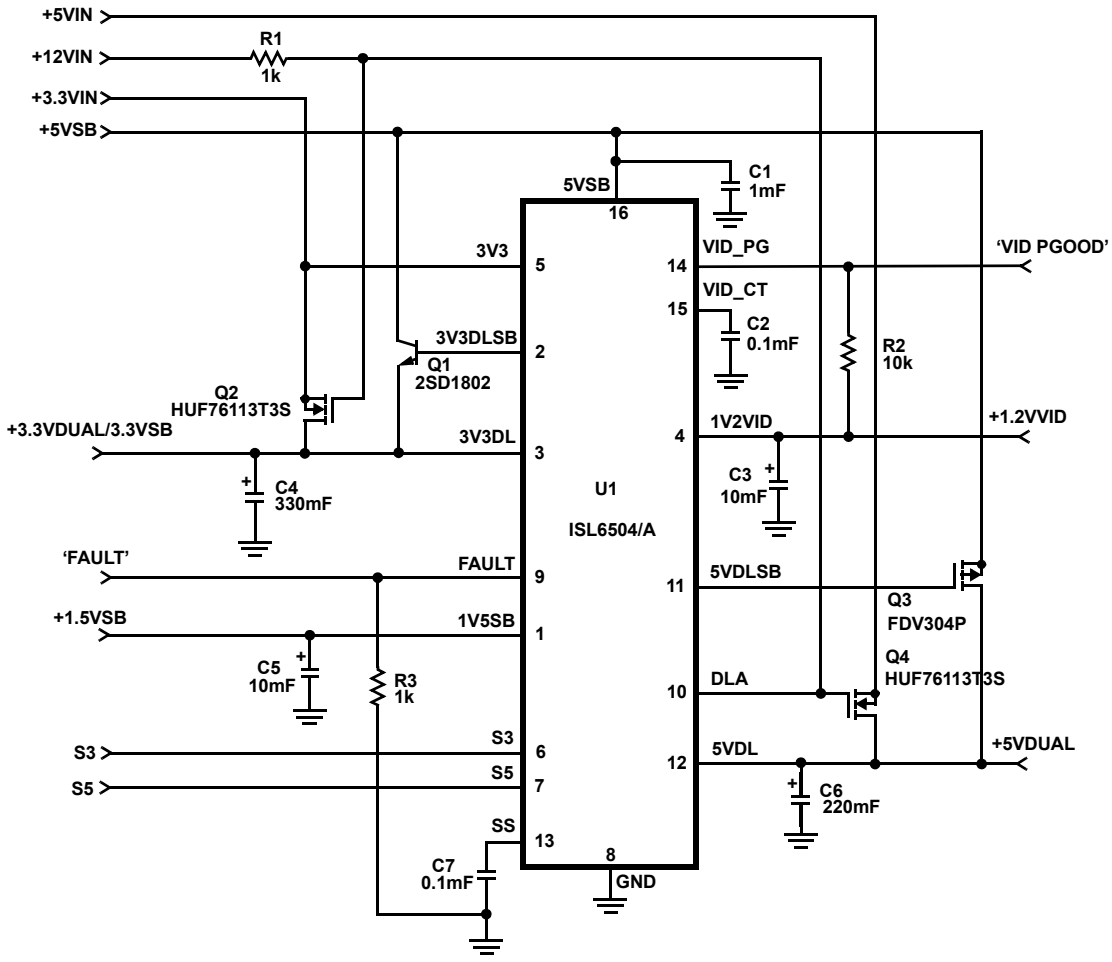
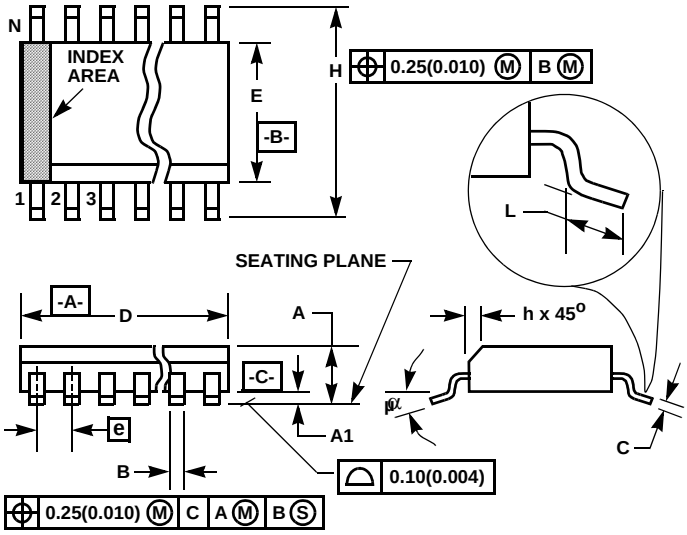


FIGURE 12. TYPICAL ISL6504/A APPLICATION DIAGRAM

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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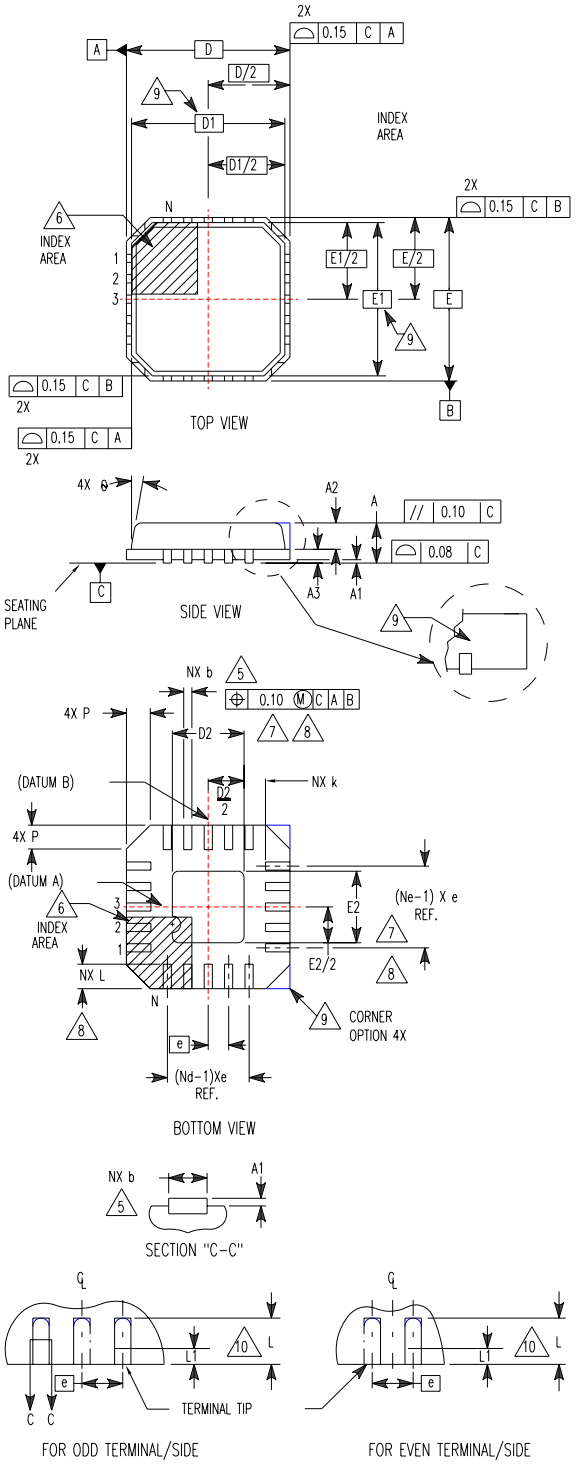
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.6x6

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJB ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.55	3.70	3.85	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.55	3.70	3.85	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

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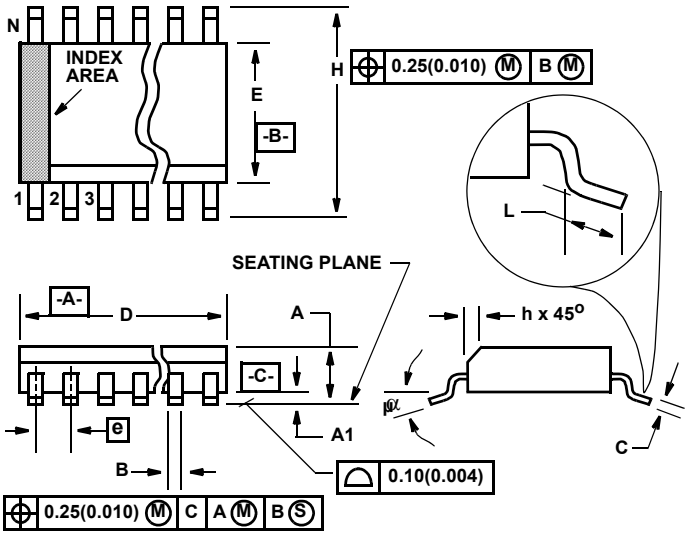
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 02/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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