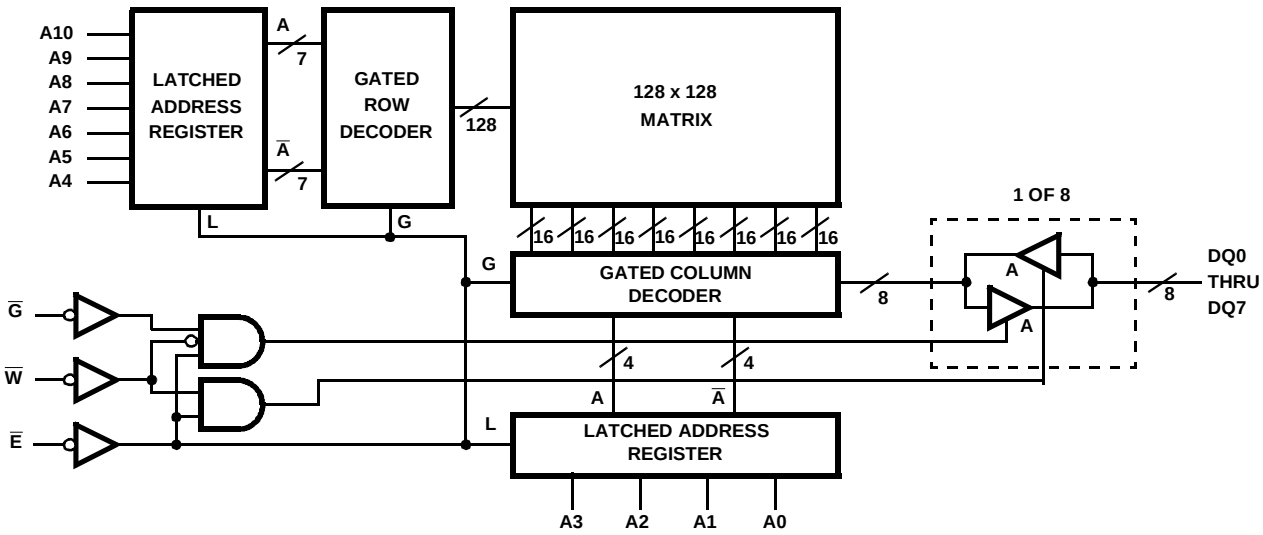
Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades. . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Ranges:
HM-6516B-9, HM-6516-9 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$48^oC/W$	$8^oC/W$
CLCC Package	$66^oC/W$	$12^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature. . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s). . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 25953 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-6516B-9, HM-6516-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	50	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V, HM-6516B-9
		-	100	µA	IO = 0mA, VI = V_{CC} or GND, HM-6516-9
ICCOP	Operating Supply Current (Note 1)	-	10	mA	f = 1MHz, IO = 0mA, $\overline{G}$ = V_{CC}, V_{CC} = 5.5V, VI = V_{CC} or GND
ICCDR	Data Retention Supply Current	-	25	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}, HM-6516B-9
		-	50	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}, HM-6516-9
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = V_{CC} or GND, V_{CC} = 5.5V
V_{IL}	Input Low Voltage	-0.3	0.8	V	V_{CC} = 4.5V
V_{IH}	Input High Voltage	2.4	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA, V_{CC} = 4.5V
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IO = -100µA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	8	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6516B-9, HM-6516-9)

SYMBOL	PARAMETER	LIMITS				UNITS	TEST CONDITIONS
		HM-6516B-9		HM-6516-9			
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	120	-	200	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	120	-	200	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	10	-	10	-	ns	(Notes 2, 3)
(4) TWLQZ	Write Enable Output Disable Time	-	50	-	80	ns	(Notes 2, 3)
(5) TEHQZ	Chip Enable Output Disable Time	-	50	-	80	ns	(Notes 2, 3)
(6) TGLQV	Output Enable Output Valid Time	-	80	-	80	ns	(Notes 1, 3)
(7) TGLQX	Output Enable Output Enable Time	10	-	10	-	ns	(Notes 2, 3)
(8) TGHQZ	Output Enable Output DisableTime	-	50	-	80	ns	(Notes 2, 3)
(9) TELEH	Chip Enable Pulse Negative Width	120	-	200	-	ns	(Notes 1, 3)
(10) TEHEL	Chip Enable Pulse Positive Width	50	-	80	-	ns	(Notes 1, 3)
(11) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(12) TELAX	Address Hold Time	30	-	50	-	ns	(Notes 1, 3)
(13) TWLWH	Write Enable Pulse Width	120	-	200	-	ns	(Notes 1, 3)
(14) TWLEH	Write Enable Pulse Setup Time	120	-	200	-	ns	(Notes 1, 3)
(15) TELWH	Write Enable Pulse Hold Time	120	-	200	-	ns	(Notes 1, 3)
(16) TDVWH	Data Setup Time	50	-	80	-	ns	(Notes 1, 3)
(17) TWHDX	Data Hold Time	10	-	10	-	ns	(Notes 1, 3)
(18) TELEL	Read or Write Cycle Time	170	-	280	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} - 2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

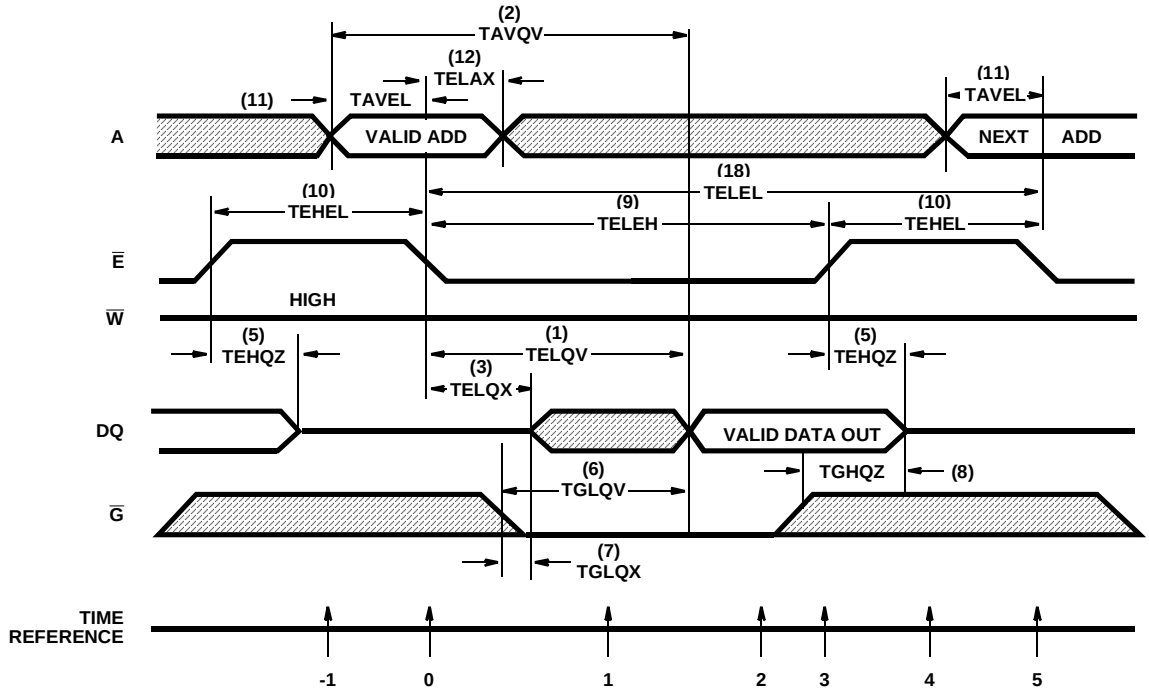


FIGURE 1. READ CYCLE

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical “1” state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Timing Waveforms (Continued)

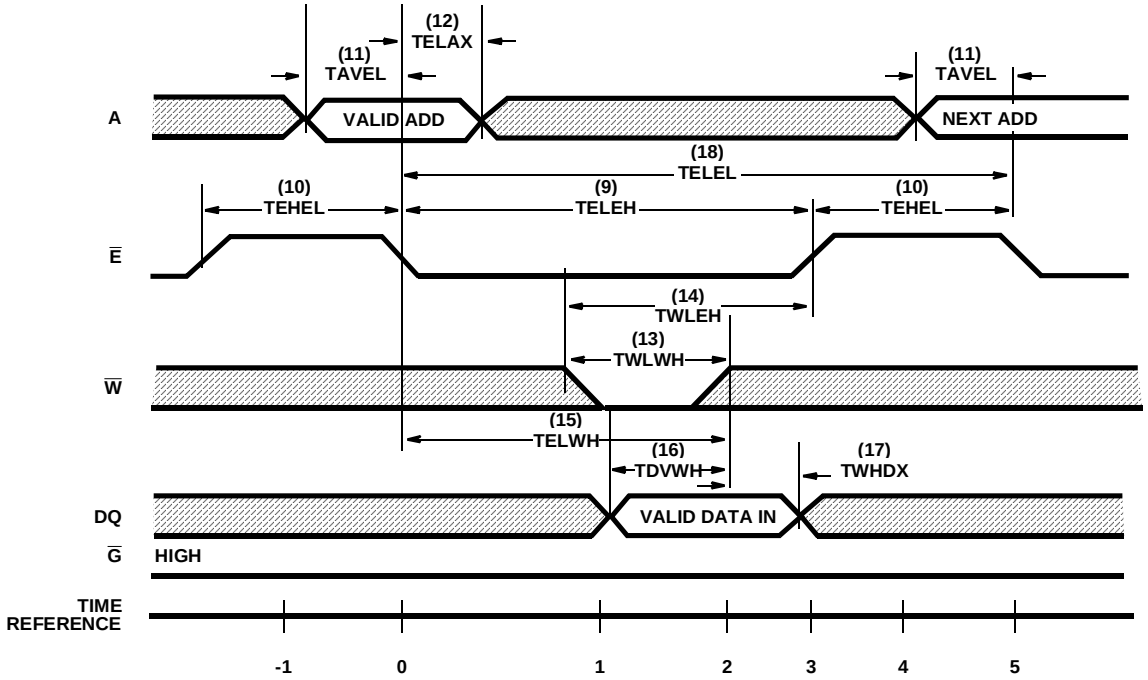


FIGURE 2. WRITE CYCLE

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising of $\overline{E}$.

Typical Performance Curve

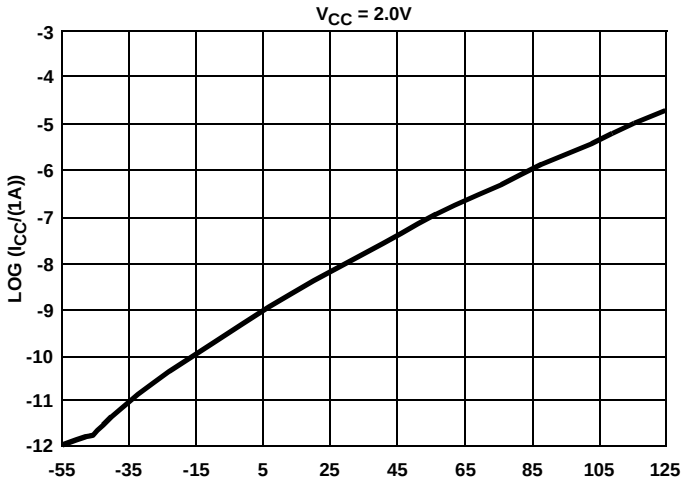


FIGURE 3. TYPICAL ICCDR vs T_A

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