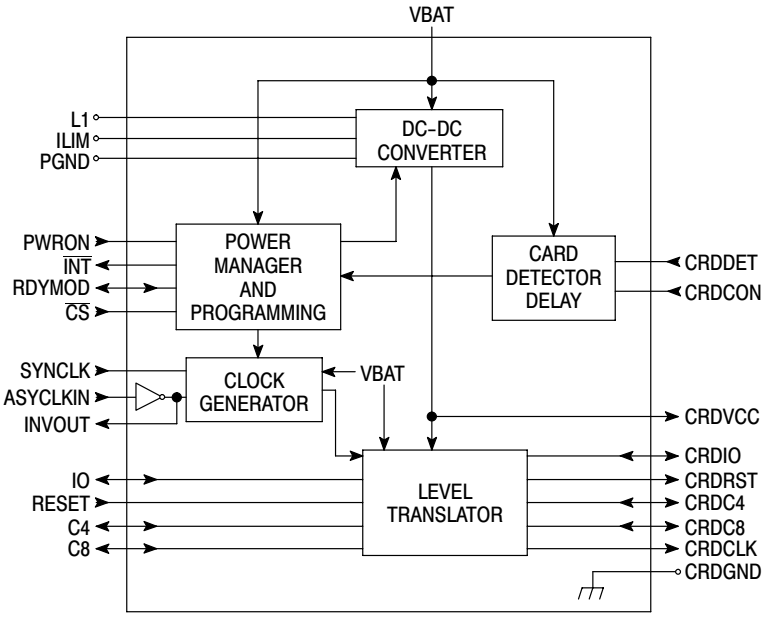


Figure 1. Simplified Functional Block Diagram

MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
V_{BAT}	Battery Supply Voltage	7.0	V
I_{BAT}	Battery Supply Current	±200	mA
V_{CC}	Power Supply Voltage	6.0	V
I_{CC}	Power Supply Current	±150	mA
V_{IN} I_{IN}	Digital Input Pins 2, 4, 5, 6, 7, 9, 10, 17, 18, 20, 21	−0.5 to V_{BAT} +0.5 but < 7.0 ±5.0	V mA
V_{OUT} I_{OUT}	Digital Output Pins 3, 4, 8	−0.5 to V_{BAT} +0.5 but < 7.0 ±10	V mA
V_{Card} I_{Card}	Card Interface Pins 11, 13, 14, 15, 16, 19	−0.5 to V_{CC} + 0.5 ±25	V mA
I_L	Coil Driver Pin 22, ILIM (Pin 24) Power Ground (Pin 1)	±200 ±100	mA
V_{ESD}	ESD Capability: (Note 2) Standard Pins 2, 3, 4, 5, 6, 7, 8, 9, 10, 17, 18, 20, 21, 22, 23, 24 Card Interface Pins 11, 13, 14, 15, 16, 19	 2.0 4.0	 kV kV
P_{Ds} $R_{\theta JAs}$	SO−24 Package: Power Dissipation @ T_A = 85°C Thermal Resistance Junction−to−Air	 285 140	 mW °C/W
P_{Dt} $R_{\theta JAt}$	TSSOP−24 Package: Power Dissipation @ T_A = 85°C Thermal Resistance Junction−to−Air	 220 180	 mW °C/W
T_A	Operating Ambient Temperature Range	−40 to +85	°C
T_J	Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}	Maximum Junction Temperature (Note 3)	150	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum electrical ratings are those values beyond which damage to the device may occur. T_A = 25°C.
2. Human body model, R = 1500 Ω, C = 100 pF.
3. Maximum thermal rating beyond which damage to the device may occur.

ELECTRICAL CHARACTERISTICS These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4.0 V, V_{CC} = 5.0 V nom, PWRON = V_{BAT} , Operating Mode, $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 μH, R_{LIM} = 0 Ω, CRDV_{CC} capacitor = 10 μF, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
BATTERY POWER SUPPLY SECTION						
Supply Voltage Range Normal operating range extended operating range (Note 4)		V_{BAT}	2.2 1.8	– –	6.0 6.6	V
MC33560 Standby Quiescent Current PWRON = GND, CRDCON = GND, ASYCLKIN = GND, V_{BAT} = 6.0 V, All Other Logic Inputs and Outputs Open		I_{oBAT}	–	–	30	μA
DC Operating Current $-I_{CC}$ = 10 mA; V_{CC} = 5.0 V, V_{BAT} = 6.0 V		I_{BATop}	–	–	12.5	mA
V_{BAT} Undervoltage Detection: Upper Threshold Lower Threshold Hysteresis		–	 – – –	 1.6 1.4 0.2	 – – –	V
V_{CC} = 5.0 V NOMINAL POWER SUPPLY SECTION						
Output Voltage	2.2 V ≤ V_{BAT} ≤ 6.0 V 1.0 mA ≤ $-I_{CC}$ ≤ 25 mA 3.0 V ≤ V_{BAT} ≤ 6.0 V 1.0 mA ≤ $-I_{CC}$ ≤ 60 mA	V_{CC}	 4.75 4.60	 5.0 5.0	 5.25 5.40	V
Card V_{CC} Undervoltage Detection: Upper Threshold Lower Threshold Switching Hysteresis	(RDYMOD Output) (See Table 4)	 V_{T5H} V_{T5L} V_{HYS5}	 4.2 120	 4.5 180	 V_{CC} − 0.14 	 V mV
Peak Output Current	V_{CC} = 4.0 V, Internally Limited (RDYMOD = L)	$-I_{CClim}$	80	–	–	mA
Current limit time−out	V_{CC} = 4.0 V	t_d	–	160	–	ms
Startup Current	V_{CC} = 2.0 V; 0°C to +85°C −40°C to 0°C	$-I_{CCst}$	80 50	– –	– –	mA
Low Side Switch Saturation Voltage	I_L = 50 mA, Pin 22	V_{sat22}	–	100	160	mV
Rectifier on Saturation Voltage	I_L = 50 mA, Pin 22 to Pin 13	V_{Fsat22}	–	400	520	mV
Converter Switching Frequency	T_A = 25°C	f_{sw}	–	120	–	kHz
Shutdown Current (Card access deactivated)	PWRON = GND, V_{CC} = 2.0 V	I_{SD}	80	–	–	mA
V_{CC} = 3.0 V NOMINAL POWER SUPPLY SECTION (V_{BAT} = 2.5 V, $-I_{CC}$ = 5.0 mA)						
Output Voltage	2.2 V ≤ V_{BAT} ≤ 6.0 V 1.0 mA ≤ $-I_{CC}$ ≤ 10 mA 2.5 V ≤ V_{BAT} ≤ 6.0 V 1.0 mA ≤ $-I_{CC}$ ≤ 50 mA	V_{CC}	 2.75 2.60	 3.0 3.0	 3.25 3.40	V
Card V_{CC} Undervoltage Detection: Upper Threshold Lower Threshold Switching Hysteresis	(RDYMOD Output) (See Table 4)	 V_{T3H} V_{T3L} V_{HYS3}	 2.4 80	 2.7 110	 V_{CC} − 0.1 	 V mV
Startup Current Shutdown Current (Card access deactivated)	V_{CC} = 2.0 V PWRON = GND, V_{CC} = 2.0 V	$-I_{CCst}$ I_{SD}	50 50	– –	– –	mA

4. See Figures 2 and 3.
5. The transistors T1 on lines IO, C4 and C8 (see Figure 24) have a max R_{dson} of 250 Ω.
6. Pin loading = 30 pF, except INVOUT = 15 pF.
7. As the clock buffer is optimized for low power consumption and hence not symmetrical, clock signal duty cycle is guaranteed for divide by 2 and divide by 4 ratio.
8. In either direction.

ELECTRICAL CHARACTERISTICS (continued) These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4.0 V, V_{CC} = 5.0 V nom, PWRON = V_{BAT} , Operating Mode, $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 μH, R_{LIM} = 0 Ω, CRDV_{CC} capacitor = 10 μF, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
APPLICATION INTERFACE DC SECTION (V_{BAT} = 5.0 V)						
Input High Threshold Voltage (increasing)	Pins 2, 4, 5, 6, 10, 17	V_{IH}	0.55*V_{BAT}	−	0.65*V_{BAT}	V
Input Low Threshold Voltage (decreasing)	Pins 2, 5, 6, 10 Pin 17 Pin 4	V_{IL}	0.3*V_{BAT} 0.2*V_{BAT} 0.3*V_{BAT}	− − −	0.45*V_{BAT} 0.40*V_{BAT} 0.5*V_{BAT}	V
Switching Hysteresis	Pins 2, 4, 5, 6, 10, 17	V_{HYST}	0.06*V_{BAT}	−	0.3*V_{BAT}	V
Threshold Voltage	Pin 9 Pin 18	V_{TH}	0.5*V_{BAT} 0.4*V_{BAT}	− −	0.6*V_{BAT} 0.6*V_{BAT}	V
Pulldown resistance	V_{IN} = V_{BAT} − 1.0 V, Pins 2, 6, 7, 10	R_{down}	120	240	500	kΩ
Pullup resistance	V_{IN} = 0.5 V, Pin 3, 4, 5	R_{up}	120	240	500	kΩ
Output High Voltage	I_{OH} = −2.5 μA, Pin 3, Pin 4 for $\overline{CS}$ = H I_{OH} = −50 μA, pins 7, 20,21 I_{OH} = −0.2 mA, Pin 8 Pin 4 (in Output Mode)	V_{OH}	V_{BAT} − 1	−	−	V
Output Low Voltage	I_{OL} = 1.0 mA, Pins 7, 20, 21 I_{OL} = 0.2 mA, Pins 3, 4, 8	V_{OL}	−	−	0.4	V
Input Leakage Current	V_{IN} = 2.5 V, $\overline{CS}$ = H, Pins 9, 17, 18, 20, 21	$\pm I_{leak}$	−	−	2.0	μA
CARD INTERFACE DC SECTION (V_{BAT} = 5.0 V)						
Output High Voltage	I_{OH} = −20 μA, Pins 11, 16, 19 I_{OL} = 0.2 mA, Pins 14, 15	V_{OH}	V_{CC} − 0.9	−	−	V
Output Low Voltage	I_{OL} = 1.0 mA, Pins 11, 16, 19 I_{OL} = 0.2 mA, Pins 14, 15	V_{OL}	−	−	0.4	V
I/O Pullup Resistance, Operating Mode, $\overline{CS}$ =L , PWRON = H	V_{OL} = 0.5 V, Pins 11, 16, 19	−	−	18	−	kΩ
Card pins security voltage (Card access deactivated)	PWRON = GND, Iin = 10 mA, Pins 11, 14, 15, 16, 19	$V_{security}$	−	−	2.0	V
DIGITAL DYNAMIC SECTION (V_{BAT} = 5.0 V, Normal Operating Mode) (Note 6)						
Input Clock Frequency	Pin 9, Duty Cycle = 50%	f_{asyclk}	−	−	20	MHz
Card Clock Frequency	Pin 15	f_{crdclk}	−	−	20	MHz
Card Clock Duty Cycle (Note 7)	Pin 15, 50% to 50% V_{CC}, f_{io} = 16 MHz	r_{clk}	45	−	55	%
Card Clock Rise and Fall Time	Pin 15, 10% ↔ 90% V_{CC}	t_{rclk}, t_{fclk}	−	−	10	ns
I/O Data Transfer Frequency	Pin [7, 11], [21, 16], [20, 19] (Note 8)	f_{io}	−	1.0	−	MHz
I/O Duty Cycle	Pin [7, 11], [21, 16], [20, 19] (Note 8) 50% to 50% V_{CC}	r_{io}	45	−	55	%
I/O Rise and Fall Time	Pin [7, 11], [21, 16], [20, 19] (Note 8) 10% ↔ 90% V_{CC}	t_{rio}, t_{fio}	−	−	150	ns
I/O Transfer Time	Pin [7, 11], [21, 16], [20, 19] (Note 8) 50% to 50% V_{CC}, L → H, H → L	t_{tr}	−	−	100	ns
Card Signal Sequence Interval	Pins 11, 14, 15, 16, 19 V_{CC} Powerup / Powerdown	t_{dseq}	−	0.2	1.0	μs

4. See Figures 2 and 3.
5. The transistors T1 on lines IO, C4 and C8 (see Figure 24) have a max R_{dson} of 250 Ω.
6. Pin loading = 30 pF, except INVOUT = 15 pF.
7. As the clock buffer is optimized for low power consumption and hence not symmetrical, clock signal duty cycle is guaranteed for divide by 2 and divide by 4 ratio.
8. In either direction.

ELECTRICAL CHARACTERISTICS (continued) These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4.0 V, V_{CC} = 5.0 V nom, PWRON = V_{BAT} , Operating Mode, $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 μH, R_{LIM} = 0 Ω, $CRDV_{CC}$ capacitor = 10 μF, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
DIGITAL DYNAMIC SECTION (V_{BAT} = 5.0 V, Normal Operating Mode) (Note 6)						
Card Detection Filter Time: Card Insertion Card Extraction		 t_{fltin} t_{fltout}	 50 50	 – –	 150 150	 μs μs
Internal Reset Delay	$\overline{RES}$, V_{CC} Powerup / Powerdown	t_{dres}	–	20	–	μs
Ready Delay Time	Pin 4	t_{drdy}	–	–	2.0	μs
PWRON low Pulse Width	$\overline{CS}$ = L, Pin 2	t_{won}	2.0	–	–	μs
DIGITAL DYNAMIC SECTION (V_{BAT} = 5.0 V, programming mode) (Note 6)						
Data Setup Time RDYMOD, PWRON, RESET, IO	Pins 2, 4, 6, 7	t_{smod}	1.0	–	–	μs
Data Hold Time RDYMOD, PWRON, RESET, IO	Pins 2, 4, 6, 7	t_{hmod}	1.0	–	–	μs
$\overline{CS}$ low Pulse Width	Pin 5	t_{wcs}	2.0	–	–	μs

4. See Figures 2 and 3.
5. The transistors T1 on lines IO, C4 and C8 (see Figure 24) have a max R_{dson} of 250 Ω.
6. Pin loading = 30 pF, except INVOUT = 15 pF.
7. As the clock buffer is optimized for low power consumption and hence not symmetrical, clock signal duty cycle is guaranteed for divide by 2 and divide by 4 ratio.
8. In either direction.

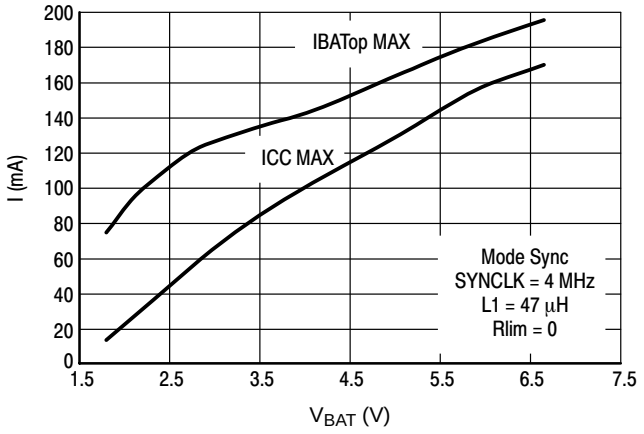


Figure 2. Maximum Battery and Card Supply Current vs. V_{BAT} (V_{CC} = 5.0 V)

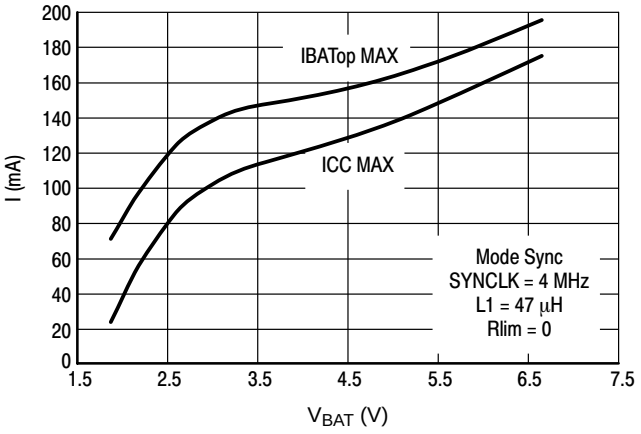


Figure 3. Maximum Battery and Card Supply Current vs. V_{BAT} (V_{CC} = 3.0 V)

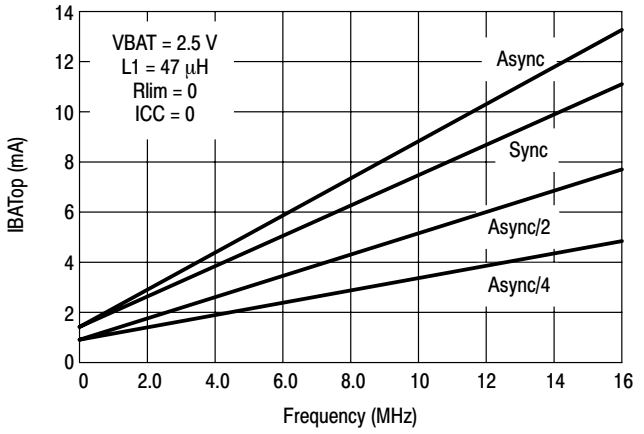


Figure 4. Battery Current vs. Input Clock Frequency (I_{CC} = 0, V_{BAT} = 4.0 V)

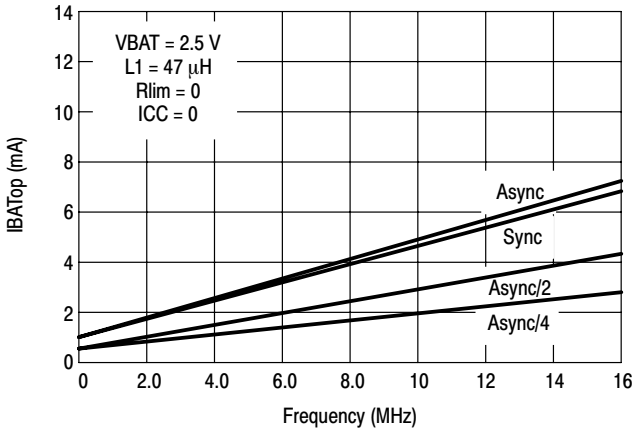


Figure 5. Battery Current vs. Input Clock Frequency (I_{CC} = 0, V_{BAT} = 2.5 V)

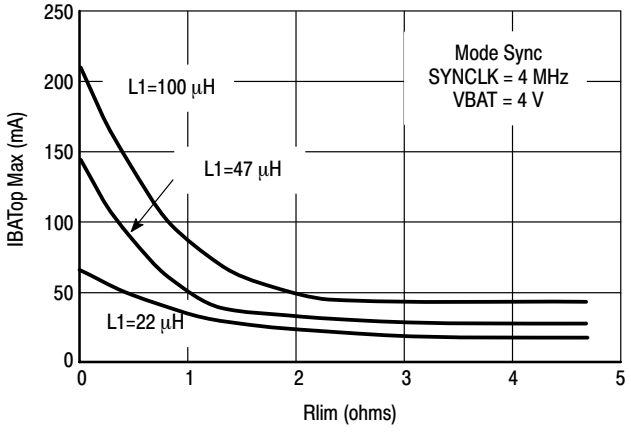


Figure 6. Maximum Battery Current vs. R_{LIM} (V_{CC} = 5.0 V, V_{BAT} = 4.0 V)

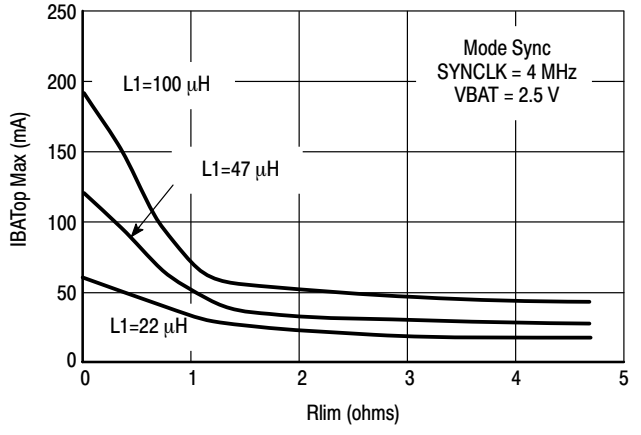


Figure 7. Maximum Battery Current vs. R_{LIM} (V_{CC} = 3.0 V, V_{BAT} = 2.5 V)

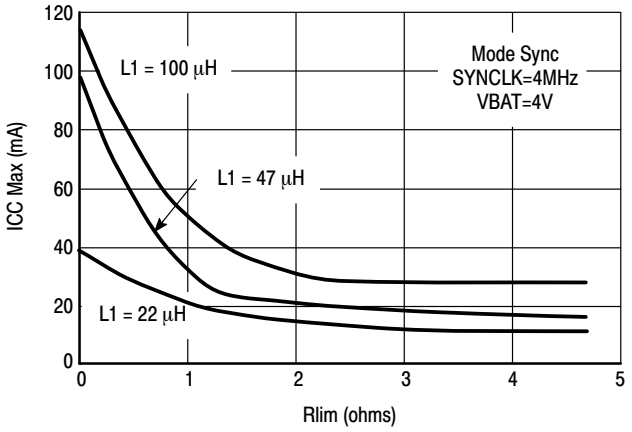


Figure 8. Maximum Card Supply Current vs. R_{LIM} (V_{CC} = 5.0 V, V_{BAT} = 4.0 V)

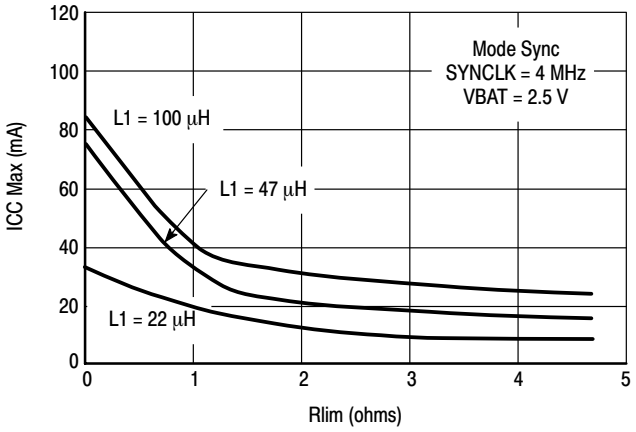


Figure 9. Maximum Card Supply Current vs. R_{LIM} (V_{CC} = 3.0 V, V_{BAT} = 2.5 V)

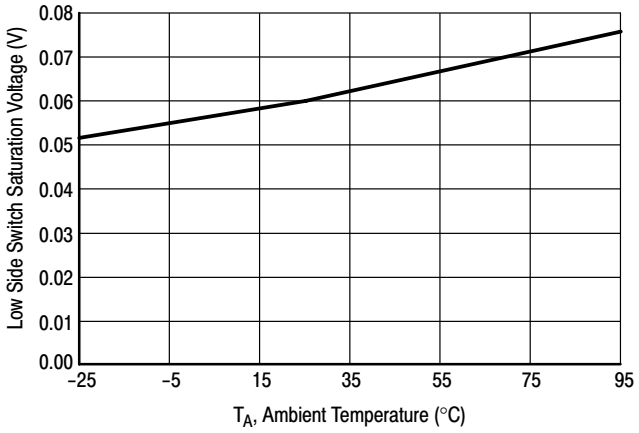


Figure 10. Low Side Switch Saturation Voltage (I_L = 50 mA) vs. Temperature

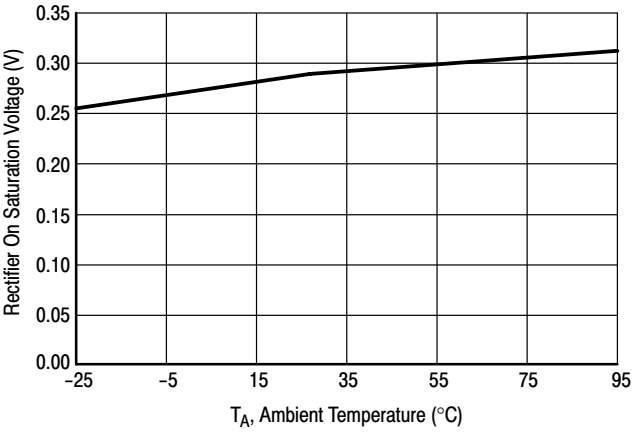


Figure 11. Rectifier On Saturation Voltage (I_L = 50 mA) vs. Temperature

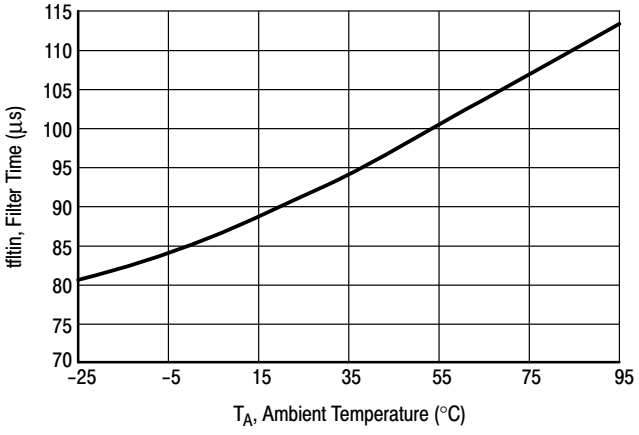


Figure 12. Card Detection (Insertion) Filter Time vs. Temperature

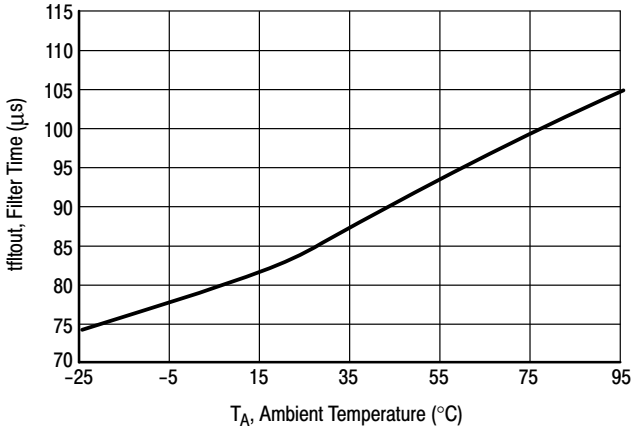


Figure 13. Card Detection (Extraction) Filter Time vs. Temperature

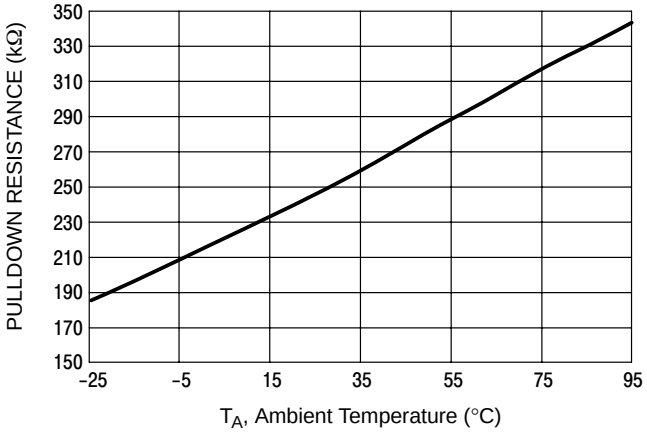


Figure 14. Pulldown Resistance vs. Temperature

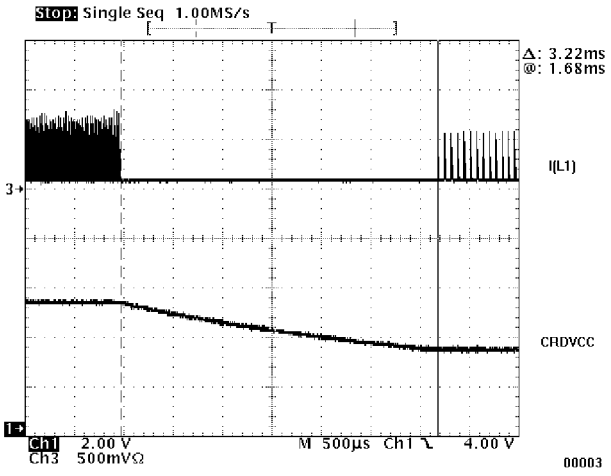


Figure 15. Transition from 5.0 V to 3.0 V Card Supply

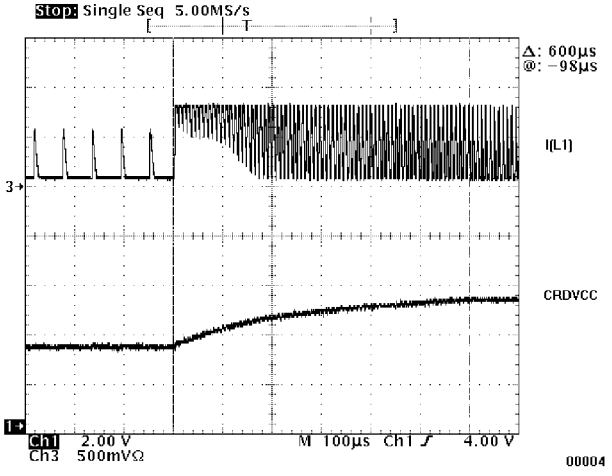


Figure 16. Transition from 3.0 V to 5.0 V Card Supply

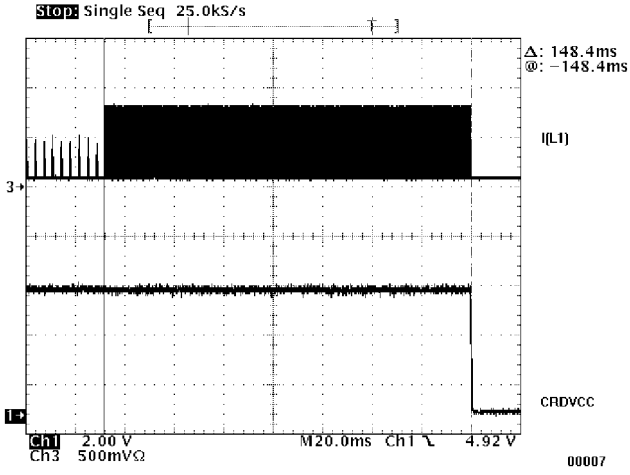


Figure 17. Overcurrent Shutoff (t_d = 160 ms)

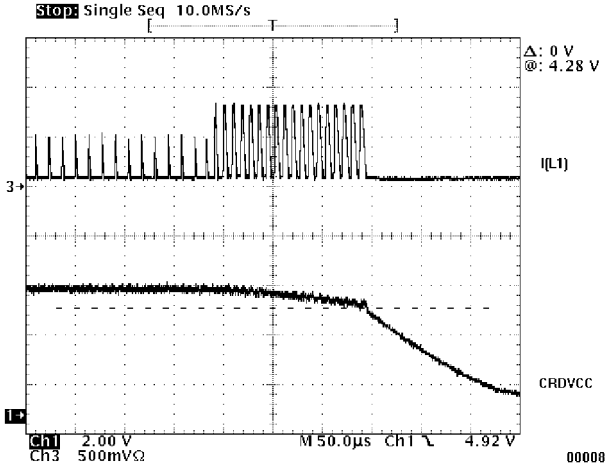


Figure 18. Undervoltage Shutoff (V_{T5L} = 4.6 V)

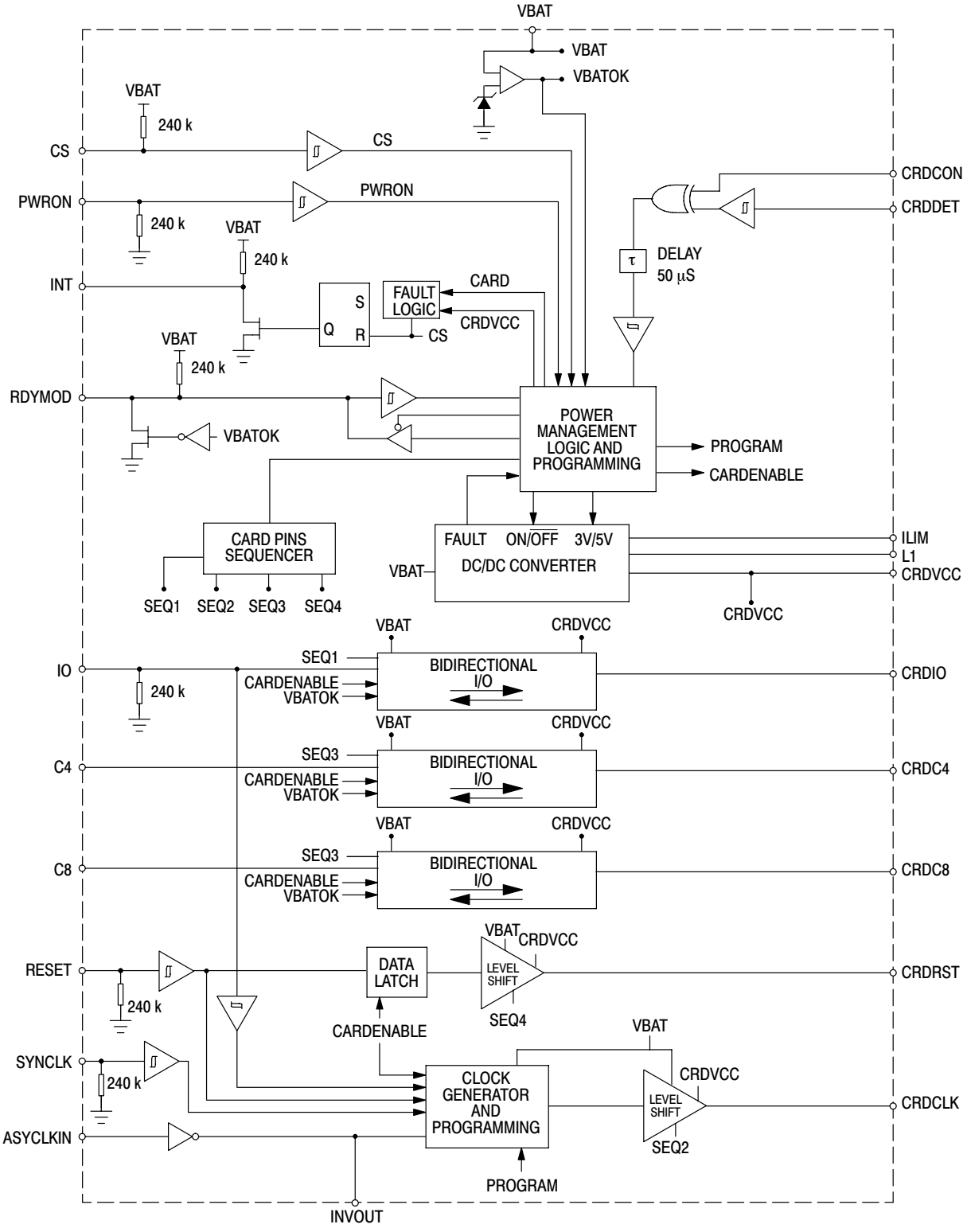


Figure 19. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Name/Function
CONTROLLER INTERFACE			
2	PWRON	INPUT Pulldown	This pin is used to start operation of the internal DC−DC converter. In programming mode, this pin is used to set the “Output Voltage” switch. (See Table 2).
3	INT	OUTPUT Pullup	This open collector pin indicates a change in the card presence circuit status. When a card is inserted or extracted, the pin goes to logic level “0”. The signal is reset to logic level “1” upon the rising edge of $\overline{CS}$ or upon the rising edge of PWRON. In the case of a multislot application, two or more $\overline{INT}$ outputs are connected together and the microcontroller has to poll all the MC33560s to identify which slot was detected.
4	RDYMOD	I/O and Pullup	This bidirectional pin has tri−state output and Schmitt trigger input. * When RDYMOD is forced to 0, the MC33560 can be set to programming mode by a negative transition on $\overline{CS}$. * When RDYMOD is connected to a high impedance, the MC33560 is in normal operating mode, and RDYMOD is in output mode (See Tables 2 and 4): − With $\overline{CS}$ = L and PWRON=H, RDYMOD indicates the status of the DC−DC converter. − With $\overline{CS}$ = L and PWRON=L, RDYMOD indicates the status of the card detector.
5	CS	INPUT Pullup	This is the MC33560 chip select signal. Pins 2, 6, 7, 10, 20, 21 are disabled when $\overline{CS}$ = H. When RDYMOD = L, the MC33560 enters programming mode upon the falling edge of $\overline{CS}$. (Figure 20)
6	RESET	INPUT Pulldown	The signal present at this input pin is translated to Pin 14 (the card reset signal) when $\overline{CS}$ = L. The signal on this pin is latched when $\overline{CS}$ = H. This pin is also used in programming mode. (See Table 2)
7	I/O	I/O	This pin connects to the Serial I/O port of a microcontroller. A bi−directional level translator adapts the serial I/O signal between the smartcard and the microcontroller. The level translator is enabled when $\overline{CS}$ = L. The signal on thispin is latched when $\overline{CS}$=H. This pin is also used in programming mode. (See Table 2)
8	INVOUT	CLK OUTPUT	The ASYCLKIN (Pin 9) signal is buffered and inverted to generate the output signal INVOUT. This output is used for multislot applications, where the ASYCLKIN inputs and INVOUT outputs are daisy−chained. (See the multislot application example in Figure 31)
9	ASYCLKIN	CLK INPUT high impedance	This pin can be connected to the microcontroller master clock or any clock signal for asynchronous cards. The signal is fed to the internal clock selector circuit, and is translated to CRDCLK at the same frequency, or divided by 2 or 4, depending on programming. (See Table 3)
10	SYNCLK	CLK INPUT Pulldown	This function is used for communication with synchronous cards, and the pin is generally connected to the controller serial interface clock signal. The signal is fed to the internal clock selector circuit, and is translated to CRDCLK upon appropriate programming of the MC33560 (See Table 3). When selected at programming, the signal on this pin is latched when $\overline{CS}$ = H.
20	C8	I/O	General purpose input/output. It has the same behavior as I/O, except for programming. It can be connected to a bidirectional port of the microcontroller. The level translator is enabled when CS = L, and the signal is latched whenCS = H. (Compare with Pin 19)
21	C4	I/O	General purpose input/output. It has the same behavior as I/O, except for programming. It can be connected to a bidirectional port of the microcontroller. The level translator is enabled when $\overline{CS}$ = L, and the signal is latched when $\overline{CS}$ = H. (Compare with Pin 16)
CARD INTERFACE			
11	CRDIO	I/O	This pin connects to the serial I/O pin of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the microcontroller. (Compare with Pin 7)
14	CRDRST	OUTPUT	This pin connects to the RESET pin of the card connector. A level translator adapts the RESET signal driven by the microcontroller. (Compare with Pin 6)
15	CRDCLK	OUTPUT	This pin connects to the CLK pin of the card connector. The CRDCLK signal is the output of the clock selector circuit.The clock selection is programmed using Pins 2, 6 and 7 with RDYMOD forced to “0”.
16	CRDC4	I/O	General purpose input/output. It has the same behavior as CRDIO. It can be connected to the C4 pin of the card connector.
17	CRDDET	INPUT high impedance	This pin connects to the card detection switch of the card connector. Card detection phase is determined with Pin 18. This pin needs an external pullup or pulldown resistor to operate properly.
18	CRDCON	INPUT high impedance	This pin connects to PGND or V_{BAT}, or possibly to an output port of the microcontroller. With this pin set to a logic “0”, the presence of a card is signalled with a logic “1” on Pin 17. With this pin set to a logic “1”, the presence of a card is signalled with a logic “0” on Pin 17.

Table 1. PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Name/Function
CARD INTERFACE			
19	CRDC8	I/O	General purpose input/output. It has the same behavior as CRDIO. It can be connected to the C8 pin of the card connector.
CURRENT LIMIT AND THERMAL PROTECTION			
1	PGND	POWER	This pin is the return path for the current flowing into Pin 22 (L1). It must be connected to CRDGND using appropriate grounding techniques.
12	CRDGND	POWER	This pin is the signal ground. It must be connected to the ground pin of the card connector. It is the reference level for all analog and digital signals.
13	$CRDV_{CC}$	POWER	This pin connects to the V_{CC} pin of the card connector. It is the reference level for a logic “1” of Pins 11, 14, 15, 16 and 19.
22	L1	POWER	This pin connects to an external inductance for the DC−DC converter. Please refer to the description of the DC−DC converter functional block.
23	V_{BAT}	POWER	This pin is connected to the supply voltage. Logic level “1” of Pins 2 to 10, 17, 18, 20 and 21 is referenced to V_{BAT}. Operation of the MC33560 is inhibited when V_{BAT} is lower than the minimum value.
24	ILIM	POWER	This pin can be connected to the PGND pin, or to a resistor connected to PGND, or left open, depending on the peak coil current needed to supply the card.

PROGRAMMING AND STATUS FUNCTIONS

The MC33560 features a programming interface and a status interface. Figure 20 shows how to enter and exit programming mode; Table 2 shows which pins are used to access the various functions.

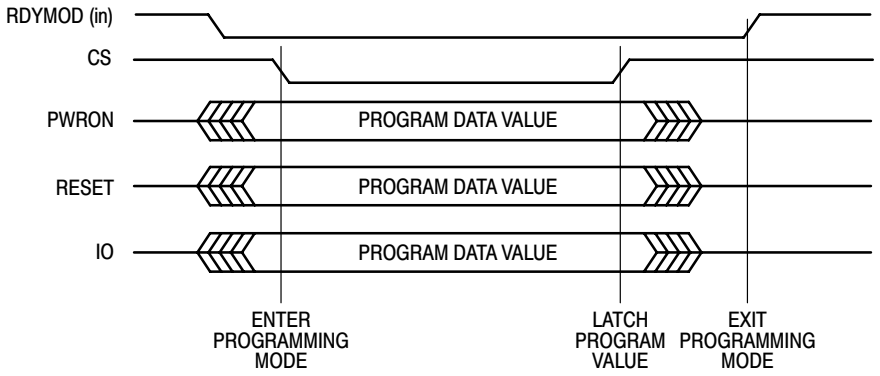


Figure 20. MC33560 Programming Sequence

Table 2. PIN USE FOR PROGRAMMING AND STATUS FUNCTIONS

	Programs $CRDV_{CC}$ TO 3 V/5 V	Select V_{CC} ON/OFF	Select Clock Input	Program ASYCLKIN Divide Ratio	Poll Card Status	Poll $CRDV_{CC}$ Status
RDYMOD (In/Out)	Force to 0	READ	Force to 0	Force to 0	READ	READ
$\overline{CS}$ (In)	rising edge	0	rising edge	rising edge	0	0
PWRON	0/1	0/1	Programs $CRDV_{CC}$	Programs $CRDV_{CC}$	0 or Hi−z	1
RESET(In)	Programs CLK Input/Divide Ratio	NOT USED	0/1	0/1	NOT USED	NOT USED
I/O(In)	Programs CLK Input/Divide Ratio	NOT USED	0/1	0/1	NOT USED	NOT USED

CARD V_{CC} AND CARD CLOCK PROGRAMMING

The $CRDV_{CC}$ and ASYCLK programming options allow the system clock frequency to be matched to the card clock frequency and to select 3.0 V or 5.0 V $CRDV_{CC}$ supply. Table 3 shows the values of **PWRON**, **RESET** and **I/O** for the possible options. The default power reset condition is state 4 (synchronous clock and $CRDV_{CC}$ =5.0 V). All states are latched for each output variable in programming mode at the positive transition of $\overline{\textbf{CS}}$ (Figure 20).

Table 3. CARD V_{CC} AND CARD CLOCK TRUTH TABLE

STATE#	PWRON	RESET	I/O	$CRDV_{CC}$	CRDCLK
0	L	L	L	3 V	SYNCLK
1	L	L	H	3 V	ASYCLKIN/4
2	L	H	H	3 V	ASYCLKIN/2
3	L	H	L	3 V	ASYCLKIN
4	H	L	L	5 V	SYNCLK
5	H	L	H	5 V	ASYCLKIN/4
6	H	H	H	5 V	ASYCLKIN/2
7	H	H	L	5V	ASYCLKIN

NOTE: Card clock integrity is maintained during all frequency commutations (no spikes).
State 4 is the default state at power on.

DC−DC CONVERTER AND CARD DETECTOR STATUS

The MC33560 status can be polled when $\overline{\textbf{CS}}$ **= L**. Please consult Table 2 for a description of input and output signals.The significance of the status message is described in Table 4.

Table 4. RDYMOD STATUS MESSAGES

PWRON (Input)	RDYMOD (Output)	Message
LOW	LOW	No card
LOW	HIGH	Card present
HIGH	LOW	DC−DC converter overload
HIGH	HIGH	DC−DC converter OK

DETAILED OPERATING DESCRIPTION

INTRODUCTION

The MC33560 Smartcard interface IC has been designed to provide all necessary functions for safe data transfers between a microcontroller and a smartcard or memory card.

A card detector scans for the presence of a card and generates a debounced wake−up signal to the microcontroller.

Communication and control signal levels are translated between the digital interface and the card interface by the voltage level translator, and the card clock is matched to the system clock frequency by the programmable card clock generator. The power management unit enables the DC−DC converter for card power supply, supervises the powerup/down sequence of the card's I/O and signal lines, and keeps the power consumption very low in standby mode.

All card interface pins have adequate ESD protection, and fault monitoring (V_{BATlow}, V_{CClow}, I_{CClim}) guarantees hazard free card reader operation.

Several MC33560s can be operated in parallel, using the same control and data bus, through the use of the chip select signal CS.

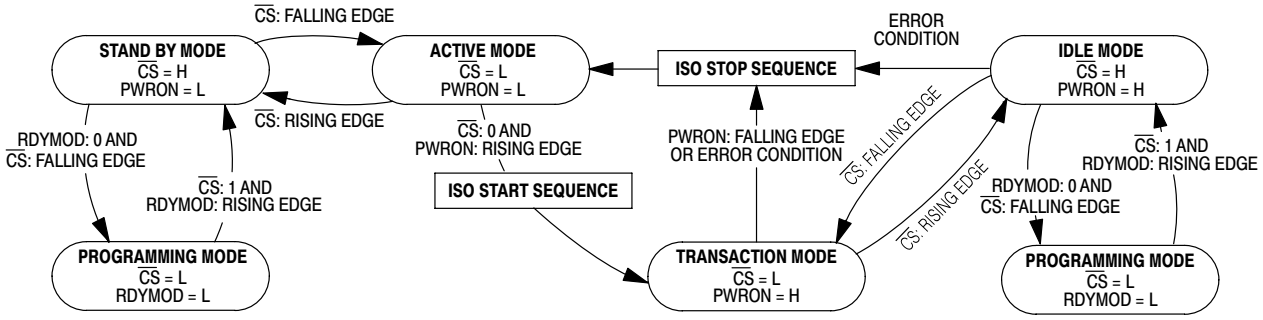


Figure 21. MC33560 Operating Modes

OPERATING MODES

The MC33560 has five operating modes:

- Standby
- Programming
- Active
- Transaction
- Idle

The transitions between these different states are shown in Figure 21 above.

STANDBY MODE

Standby mode allows the MC33560 to detect card insertion and monitor the power supply while keeping the power consumption at a minimum. It is obtained with **$\overline{CS}$ = H** and **PWRON = L**.

When the MC33560 detects a card, **$\overline{INT}$** is asserted low to wake up the Microcontroller.

PROGRAMMING MODE

The programming mode allows the user to configure the card V_{CC} and the card clock signal for his specific application. The card supply, $CRDV_{CC}$, can be programmed to 3 V or 5 V, and the card clock signal can be defined to be either synchronous, or asynchronous divided by 1, 2 or 4.

Programming mode is obtained with **RDYMOD = L** followed by a negative transition on **$\overline{CS}$**. The programming options are shown in Table 3. Programmed values are latched on a positive transition of **$\overline{CS}$** with **RDYMOD = L**.

ACTIVE MODE

In active mode, the MC33560 is selected, the **RDYMOD** pin becomes an output, and the MC33560 status can be polled. Power is not applied to the card.

The microcontroller polls the MC33560 by asserting **$\overline{CS}$ = L** and reading the **RDYMOD** pin.

If a card is present, the microcontroller starts the DC−DC converter by asserting **PWRON=H**. This starts the automatic power on sequence: when $CRDV_{CC}$ reaches the undervoltage level (V_{T5H} or V_{T3H}, depending on programming), the card sequencer validates **CRDIO**, **CRDRST**, **CRDCLK**, **CRDC4**, **CRDC8** pins according to the ISO7816−3 sequence (Figure 26). The MC33560 is now in transaction mode, and the system is ready for data exchange via the three I/O lines and the **RESET** line.

TRANSACTION MODE

In transaction mode, the MC33560 maintains power and the selected clock signal applied to the card, and the levels of the **I/O**, **RESET**, **C4** and **C8** signals between the microcontroller and the card are translated depending on the supply voltages V_{BAT} and V_{CC}.

The DC−DC converter status can be monitored on the **RDYMOD** pin.

IDLE MODE

Idle mode is used when maintaining a card powered up without communicating with it. When an asynchronous clock is used, the selected clock signal is applied to the card.

POWERDOWN OPERATION

Powerdown can be initiated by the controlling microprocessor, by stopping the DC−DC converter with **PWRON = L** while **$\overline{CS}$ = L**, or by the MC33560 itself when an error condition has been detected ($CRDV_{CC}$ undervoltage, overcurrent longer than 160 ms typ., overtemperature, “hot” card extraction). The communication session is terminated in a given sequence defined in ISO7816−3.

The MC33560 then goes into active mode, in which its status can be polled.

Standby mode is reached by deselecting the MC33560 (**$\overline{CS}$ = H**).

FUNCTIONAL BLOCKS

CARD DETECTOR

This block monitors the card contact **CRDDET** (during insertion and extraction), filters the incoming waveform and generates an interrupt signal **$\overline{INT}$** after each change. In order to identify which coupler activated the **$\overline{INT}$** line (multicoupler application) the microcontroller scans both circuits via **$\overline{CS}$** and reads the **RDYMOD** pin.

The programming input **CRDCON** tells the level detector which type of mechanical contact is implemented (normally open or normally closed). Special care is taken to hold the current consumption very low on this part of the circuit which is continuously powered by the **V_{BAT}** supply.

The **CRDDET** pin has high impedance input, and an external resistor must be connected to pullup or pulldown, depending on **CRDCON**. This resistor is chosen according to the maximum leakage current of the card connector and the PCB.

The card detector has an internal 50 μs debouncing delay. The micro controller has to insert an additional delay (in the ms range) to allow the card contacts to stabilize in the card connector before setting **PWRON = H**.

When the card detector circuit detects a card extraction, it activates the powerdown sequence and stops the converter, regardless of the **PWRON** signal. The 50 μs delay of the debouncer is enough to ensure that all card signals have reached a safe value before communication with the card takes place.

CARD STATUS

The controlling microprocessor is informed of the MC33560 status by interrupt and by polling. When a card is extracted or inserted, the $\overline{\textbf{INT}}$ line is asserted low. The interrupt is cleared upon the rising edge of $\overline{\textbf{CS}}$ or upon the rising edge of **PWRON** ($\overline{\textbf{INT}}$ line set to high state).

The microprocessor can poll the status at any time by reading the **RDYMOD** pin with proper **PWRON** setting (see Tables 2 and 4).

Since $\overline{\textbf{INT}}$ and **RDYMOD** have a high value pullup resistor (240 kΩ typical), their rise time can be as long as 10 μs if parasitic capacitance is high and no other pullup circuitry is connected.

POWER MANAGER

The task of the power manager is to activate only those circuit functions which are needed for a determined operating mode in order to minimize power consumption (Figure 19).

In standby mode (**PWRON = L**) the power manager keeps only the “card present” detector alive. All card interface pins are forced to ground potential.

In the event of a powerup request from the microcontroller (**PWRON L** to **H** transition, $\overline{\textbf{CS}}$ **= L**) the power manager starts the DC−DC converter. As soon as the $\textbf{CRDV}_{\textbf{CC}}$ supply reaches the operating voltage range, the circuit activates the card signals in the following sequence:

$CRDV_{CC}$, CRDIO, CRDCLK, CRDC4/C8, CRDRST

At the end of the transaction (**PWRON** reset to **L**, $\overline{\textbf{CS}}$ **= L**) or forced card extraction, the $\textbf{CRDV}_{\textbf{CC}}$ supply powers down and the card signal deactivation sequence takes place:

CRDRST, CRDC4/C8, CRDCLK, CRDIO, $CRDV_{CC}$

When $\overline{\textbf{CS}}$ **= L**, the bi−directional signal lines (**I/O**, **C4** and **C8**) are put into high impedance state to avoid signal collision with the microcontroller in transmission mode.

BATTERY UNDERVOLTAGE DETECTOR

The task of this block is to monitor the supply voltage, and to allow operation of the DC−DC converter only with valid voltage (typically 1.5 V). The comparator has been designed to have stability better than 20 mV in the temperature range.

DC−DC CONVERTER

Upon request from the power manager, the DC−DC converter generates the $\textbf{CRDV}_{\textbf{CC}}$ supply for the smartcard. The output voltage is programmable for 3.0 V or 5.0 V (see Table 3) to guarantee full cross compatibility of the reader for 5.0 V and 3.0 V smartcards. The wide voltage supply range, 1.8 V < V_{BAT} < 6.6 V, accommodates a broad range of coupler applications with different battery configurations (single cell or multiple cells, serial or parallel connections).

The $\textbf{CRDV}_{\textbf{CC}}$ is current−limited and short−circuit−proof. To avoid excessive battery loading during a card short−circuit, a current integration function forces the powerdown sequence (Figure 28). To retry the session, the microprocessor works through the power on sequence as defined in the power manager section.

DC−DC CONVERTER OPERATING PRINCIPLES

The DC−DC converter architecture used in the MC33560 allows step−up and step−down voltage conversion to be done. The unique regulation architecture permits an automatic transition from step−up to step−down, and from zero to full load, without affecting the output characteristics.

DC−DC Converter Description: The converter architecture is very similar to the boost architecture, with an active rectifier in place of the diode. The switching transistor is connected to ground through a resistor network in order to adjust the maximum peak current (Figure 22). A transistor connected to the converter output ($\textbf{CRDV}_{\textbf{CC}}$) forces this pin to a low voltage when the converter is not operating. This prevents erratic voltage supply to the smartcard when not in use.

The MC33560 has a built in oscillator; the DC−DC converter requires only one inductor and the output filtering capacitor to operate.

Stepup Operation: When the card supply voltage is lower than the battery voltage, the converter operates like a boost converter; the active rectifier behavior is similar to that of a diode.

Stepdown Operation: When the card supply voltage is higher than the battery voltage, the rectifier control circuit puts the power rectifying transistor in conduction when the L_1 voltage reaches $V_{BAT} + V_{FSAT22}$. The voltage across the rectifying transistor is higher than in step−up operation. The efficiency is lower, and similar to a linear regulator.

Fault Detection: The DC−DC converter has several features that help to avoid electrical overstress of the MC33560 and of the smartcard, and help to ensure that data transmission with the smartcard occurs only when its supply voltage is within predetermined limits. These functions are:

- Overtemperature Detection,
- Current Limitation, and
- Card Supply Undervoltage Detection.

The level at which current will be limited is defined by the maximum card supply current programmed with the external components L1 and RLIM.

The undervoltage detection levels for 3.0 V and 5.0 V card supply are preset internally to the MC33560.

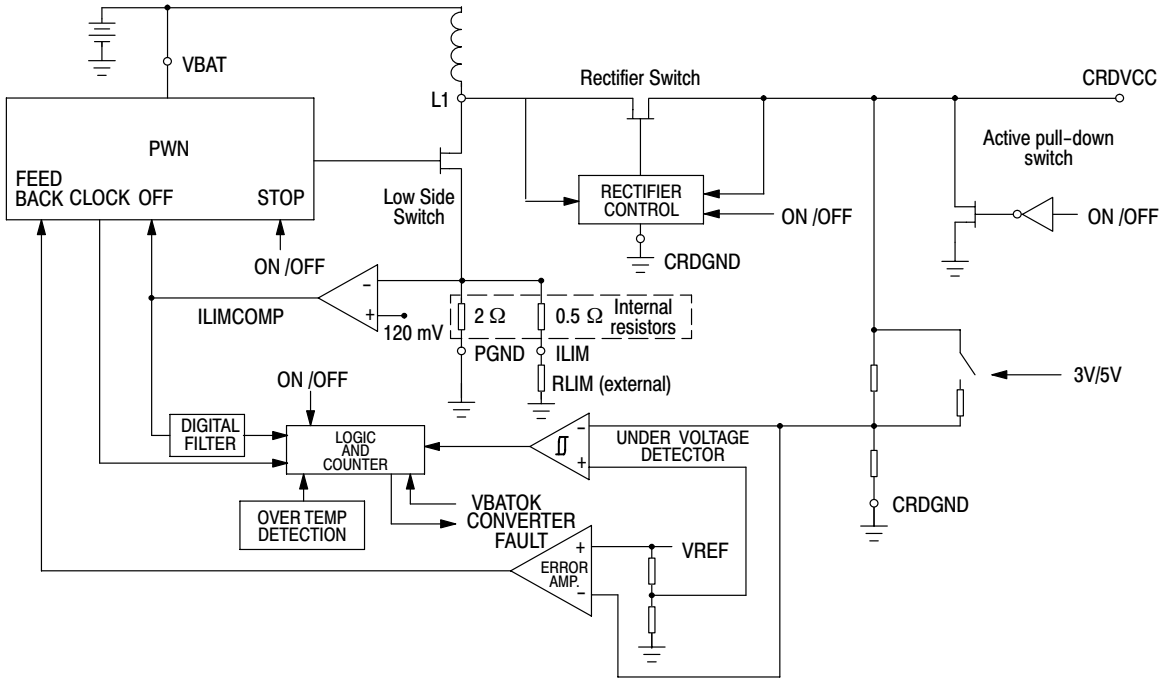


Figure 22. DC−DC Converter Functional Block

The overcurrent and undervoltage protection features are complementary, and will shut the circuit off either if the overcurrent is high enough to bring the $CRDV_{CC}$ output below the preset threshold, either after 160 ms (typ.)

In addition, the DC−DC converter will be allowed to start only if the battery supply voltage is high enough to allow normal operation (1.8 V).

The undervoltage comparator has a hysteresis and a delay of typically 20 ms to ensure stable operation. The current detector is a comparator associated with two resistors: one 2.0 Ω attached to **PGND** and usually connected to analog ground, and a 0.5 Ω attached to **ILIM**, usually connected to ground through an external resistor to adjust the maximum peak current. The voltage developed across this resistor network is then compared to a 120 mV (typical) reference voltage, and the comparator output performs a cycle−by−cycle peak current limitation by switching off the low side transistor when the voltage exceeds 120 mV.

The internal **ILIMCOMP** signal is monitored to stop the converter if current limitation is continuously detected during 160 ms (typical). This allows normal operation with high filtering capacitance and low peak current, even at converter startup. As a result, a short circuit to ground on the card connector or a continuous overcurrent is reported by **RDYMOD** 160 ms (typical) after powerup.

Unexpected Card Extraction: The MC33560 detects card extraction and runs a powerdown sequence if card power is still on when extraction occurs. An active pulldown switch clamps $CRDV_{CC}$ to GND within 150 μs (max) after extraction is detected. The external capacitors will then be discharged. With typical capacitor values of 10 μF and 47 nF as indicated in the application schematic, the time needed to discharge $CRDV_{CC}$ to a voltage below 0.4 V can be estimated to less than 750 μs. The total time aftercard extraction detection until $CRDV_{CC}$ reaches 0.4 V is then estimated to 900 μs (maximum). All smartcard connector contacts will be deactivated before $CRDV_{CC}$ deactivation. This ensures that no electrical damage will be caused to the smartcard under abnormal extraction conditions.

3.0 V/5.0 V Programming: It is possible to set the card supply voltage to 3.0 V or 5.0 V at any time, before DC−DC converter start, or during converter operation. When switching from 3.0 V to 5.0 V, a 160 ms (typical) delay blanks the undervoltage fault detection to allow filter capacitor charging.

PWM: The free−running integrated oscillator has two working modes:

Variable on−state and fixed frequency (typically 120 KHz) for average to heavy loads.

Variable on−state and variable frequency for light loads.

The frequency can be as low as a few kHz if no load is connected to **$CRDV_{CC}$**.

The charging current of the timing capacitor is related to the V_{BAT} supply voltage, to allow better line regulation, and to increase stability.

Filtering Capacitor: A high value allows efficient filtering of card current spikes. Low values allow low startup charging current. Care must be taken not to combine low capacitor value with high current limiting, as this can generate high ripple. Usual values range from 4.7 μF to 47 μF, depending on current limiting.

Selecting the External Components L1 and RLIM: The choice of inductor L1 and resistor R4 is made by using Figure 8 (5.0 V card) and/or Figure 9 (3.0 V card) on page 8:

First, determine the maximum current that the application requires to supply to the card (ICCmax, on the y−axis)

Then, select one curve that crosses the selected ICC_{max} level. The curve is associated with an inductance value (22 μH, 47 μH, or 100 μH).

Finally, use the intersection of the curve and the ICCmax level to find the R_{lim} value on the x−axis.

Good starting values are : L1 = 47 μH; R_{lim} = 0.5 Ω

Note also that, for a high inductance value (100 μH), the filtering capacitor is generally charged before inductance current reaches current limitation, while for alow inductance value, the current limitation is activated after a few converter cycles.

Battery Requirements: Having determined the L_1 and R_{lim} values, the maximum current drawn from the battery supply is shown by the curves in Figures 6 and 7.

When the application is powered by a single 3.0 V battery, special care has to be taken to extend its lifetime. When lithium batteries approach the end−of−life, their internal resistance increases, while voltage decreases. This phenomenon can prevent the startup of the DC−DC converter if the current limiting is set too high, because of the filtering capacitor charging current.

CLOCK GENERATOR

The primary purpose of the clock generator module is to match the smartcard operating frequency to the system frequency. The source frequency can be provided to **ASYCLKIN** by the microcontroller itself or from an external oscillator circuit.

In programming mode (**RDYMOD=L** and $\overline{\textbf{CS}}$ asserted low) the three input variables **PWRON**, **I/O** and **RESET** are used to configure the two output variables $\textbf{CRDV}_{\textbf{CC}}$ and **CRDCLK** as described in Table 3. This circuit setup is latched during the positive transition of $\overline{\textbf{CS}}$.

Furthermore, in asynchronous mode the system clock frequency **ASYCLKIN** can be divided by a factor of 1, 2 or 4. The circuit controls the frequency commutation to guarantee that the card clock signal remains free from spikes and glitches. In addition, this circuit ensures that **CRDCLK** signal pulses will not be shorter than the shortest and/or longer than the longest of the clock signals present before and after programming changes.

The **INVOUT** output is provided to drive other circuits without additional load to the microprocessor quartz oscillator. It can also be used to build a local RC oscillator. This driver has been optimized for low consumption; it has no hysteresis, and input levels are not symmetrical. If the **ASYCLKIN** pin is connected to a sine wave, the duty cycle will not always be 50% at **INVOUT**.

CLOCK GENERATOR OPERATING PRINCIPLES

Synchronous Clock: This clock is used mainly for memory cards. It can also be used for asynchronous (microprocessor) cards, allowing the use of two different clock sources. The status of **SYNCLK** is latched at **CRDCLK** when $\overline{\textbf{CS}}$ goes high, so that data (the **I/O** pin) and clock are always consistent at the card connector, whatever the $\overline{\textbf{CS}}$ status is. When using the synchronous clock, the clock output becomes active only when the MC33560 is selected with $\overline{\textbf{CS}}$.

Asynchronous Clock: This clock is used mainly for microprocessor cards. When applied, the clock output remains active even when the MC33560 is not selected with $\overline{\textbf{CS}}$, in order to keep the microprocessor running and avoid an unwanted reset. The **ASYCLKIN** signal is buffered at the **INVOUT** pin, so that several MC33560 systems can use the same clock with one load only.

Depending on programming, the frequency is fed directly, or divided by 2 or by 4 to the **CRDCLK** pin. If the duty cycle of the applied clock signal is not exactly symmetrical, it is recommended that the clock signal be divided by two or four to guarantee 50% duty cycle.

Clock Signal Synchronization and Consistency (Figure 29). The clock divider includes synchronization logic that controls the switch from synchronous clock to asynchronous (and vice−versa), from any division ratio to any other ratio, during $\overline{\textbf{CS}}$ changes and at powerup. The synchronization logic guarantees that each clock cycle on the **CRDCLK** pin is finished before changing clock selection (and has always the adequate duration), regardless of the moment the programming is changed.

At powerup, when **ASYCLKIN** is selected, the clock signal at the **CRDCLK** pin has an entire length, according to the selected divide ratio, whatever the **ASYCLKIN** signal is versus the internal sequencer timing.

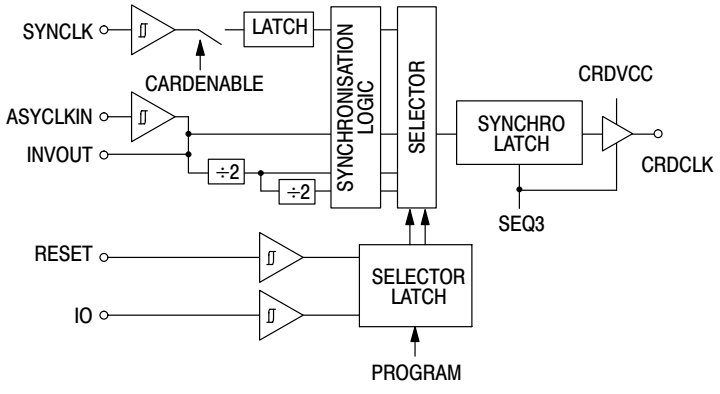


Figure 23. Clock Generator Functional Block

BIDIRECTIONAL LEVEL TRANSLATOR

This module (used on **I/O/CRDIO**, **C4/CRDC4**, **C8/CRDC8**, Figure 24) adapts the signal voltage levels of the I/O and control lines between the micro controller (supplied by V_{BAT}) and the smartcard (supplied by $CRDV_{CC}$)

When $\overline{\textbf{CS}}$ is low, with $\textbf{CRDV}_{\textbf{CC}}$ on, and start sequencing completed, this module is transparent for the data, and acts as if the card was directly connected to the reader microcontroller. The core of the level shifter circuit defined for the bidirectional **CRDIO**, **CRDC4** and **CRDC8** lines consists of a NMOS switch which can be driven to the logic low state from either side (microcontroller or card). If both sides work in transmission mode with opposite phase, then signal collision on the line is not avoidable. In this case, the peak current is limited to a safe value for the integrated circuit and the smartcard.

During high−to−low transitions, the NMOS transistor impedance (T1 = 250 Ω maximum) is low enough to charge parasitic capacitance, and have a high enough dv/dt. On low to high transition, the NMOS transistor is not active above a certain voltage, and an acceleration circuit is activated to ensure a high dv/dt.

When the chip is disabled ($\overline{\textbf{CS}}$ = **H**) with the voltage supply $\textbf{CRDV}_{\textbf{CC}}$ still active, the **I/O**, **C4** and **C8** lines keep their last logic state.

When the converter is off, a transistor forces the **CRDIO**, **CRDC4** and **CRDC8** lines to a low state, thus preventing any unwanted voltage level to be applied to the data lines when the card is not in use.

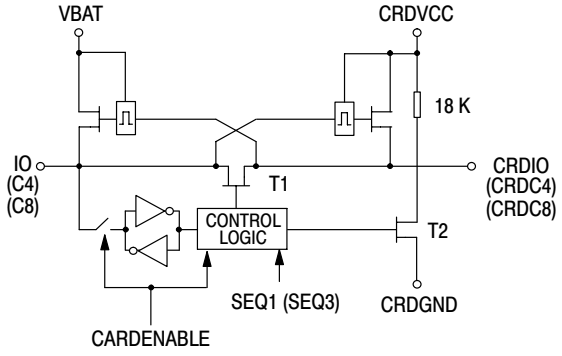


Figure 24. Bidirectional Translator Functional Block

SECURITY FEATURES

The MC33560 has a number of unique security functions to guarantee that no electrical damage will be caused to the smartcard:

- Battery supply minimum voltage threshold
- Card supply undervoltage and overcurrent detection with automatic shutdown
- Card pin overvoltage clamp to $CRDV_{CC}$
- Card presence detector for “clean” and fast shutdown
- Consistent card signal sequencing at startup and powerdown, according to ISO7816, even on error conditions
- Consistent clock signal, even when division ratio or synchronization clock signal are changed “on the fly” during a card session (Figure 29)
- Active pulldown on all card pins, including $\textbf{CRDV}_{\textbf{CC}}$, when not in normal operating mode.

A current limiting function and an overtemperature detector are limiting power dissipation.

ESD PROTECTION

Due to the nature of smartcards, the card interface pins must absorb high Electro Static Discharge (ESD) energy during card insertion. In addition, the control circuits attached to these pins must safely withstand short circuits and voltage transients during forced card extraction.

Therefore, the MC33560 features enhanced ESD protection, current limitation and short circuit protection on all smartcard interface pins, including **C4** and **C8**.

PARALLEL OPERATION

For applications where two or more MC33560 are used, the digital control and data bus lines are common to all MC33560. Only the chip select signal, $\overline{\textbf{CS}}$, requires a separate line for each interface.

While deselected, all communication pins except **CRDCLK** will keep their logical state on the card side, and will go to high impedance mode on the microprocessor side.

Figure 31 shows a typical application of a dual card reader. This arrangement was chosen only to illustrate the parallel operation of two card interfaces in the same module. The discrete capacitor components are necessary to provide low impedance on the supply lines $\textbf{V}_{\textbf{BAT}}$ and $\textbf{CRDV}_{\textbf{CC}}$ and to suppress the high frequency noise due to the DC−DC converter. The load resistors are external in order to adapt the sense current of the “card present” switches.

MINIMUM POWER CONSUMPTION CONSIDERATIONS

All analog blocks except the V_{BAT} comparator and the card presence detector are disabled in standby mode ($\overline{\textbf{CS}}$ = **H**: DC−DC converter stopped).

In order to maintain standby current at a minimum value, all pins with pullup resistance (**$\overline{\text{CS}}$**, **$\overline{\text{INT}}$**, **RDYMOD**) have to be kept in the high state or left open, and pins with pulldown resistance (**RESET**, **SYNCLK**, **PWRON**) have to be kept in the low state or left open. **ASYCLKIN** should not be connected to an active clock signal during standby to avoid dynamic currents. This is valid also for **SYNCLK**, except that it can be left open.

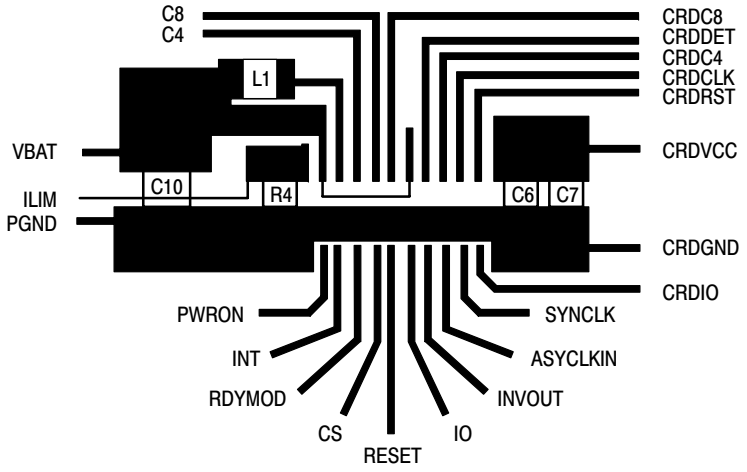


Figure 25. Example of Single Sided PCB Layout for MC33560

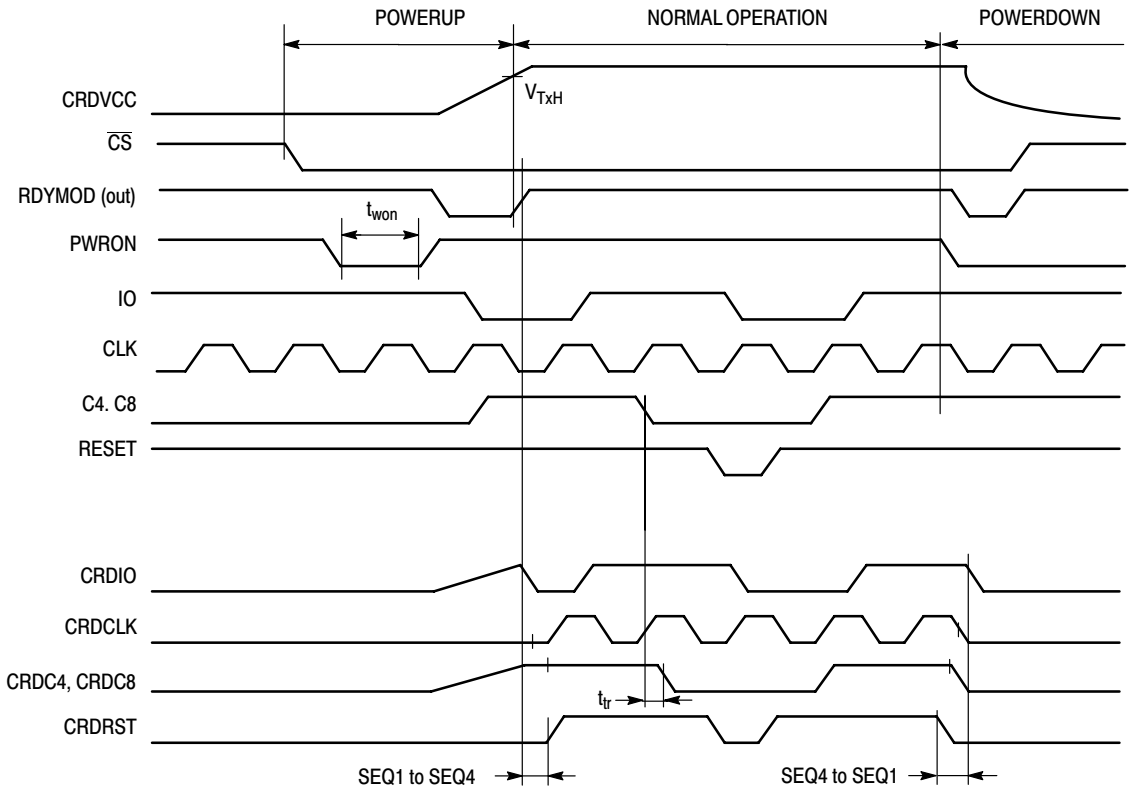


Figure 26. Card Signal Sequence During V_{CC} Powerup/Down

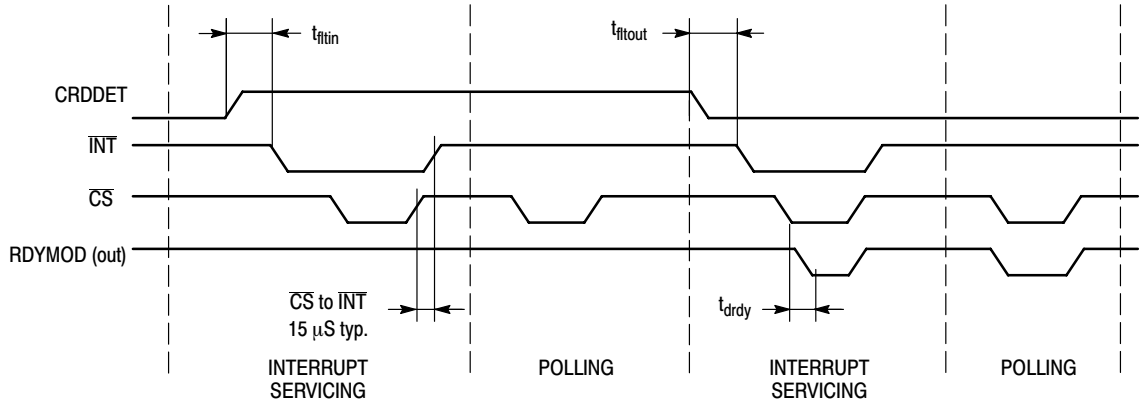


Figure 27. Interrupt Servicing and Polling

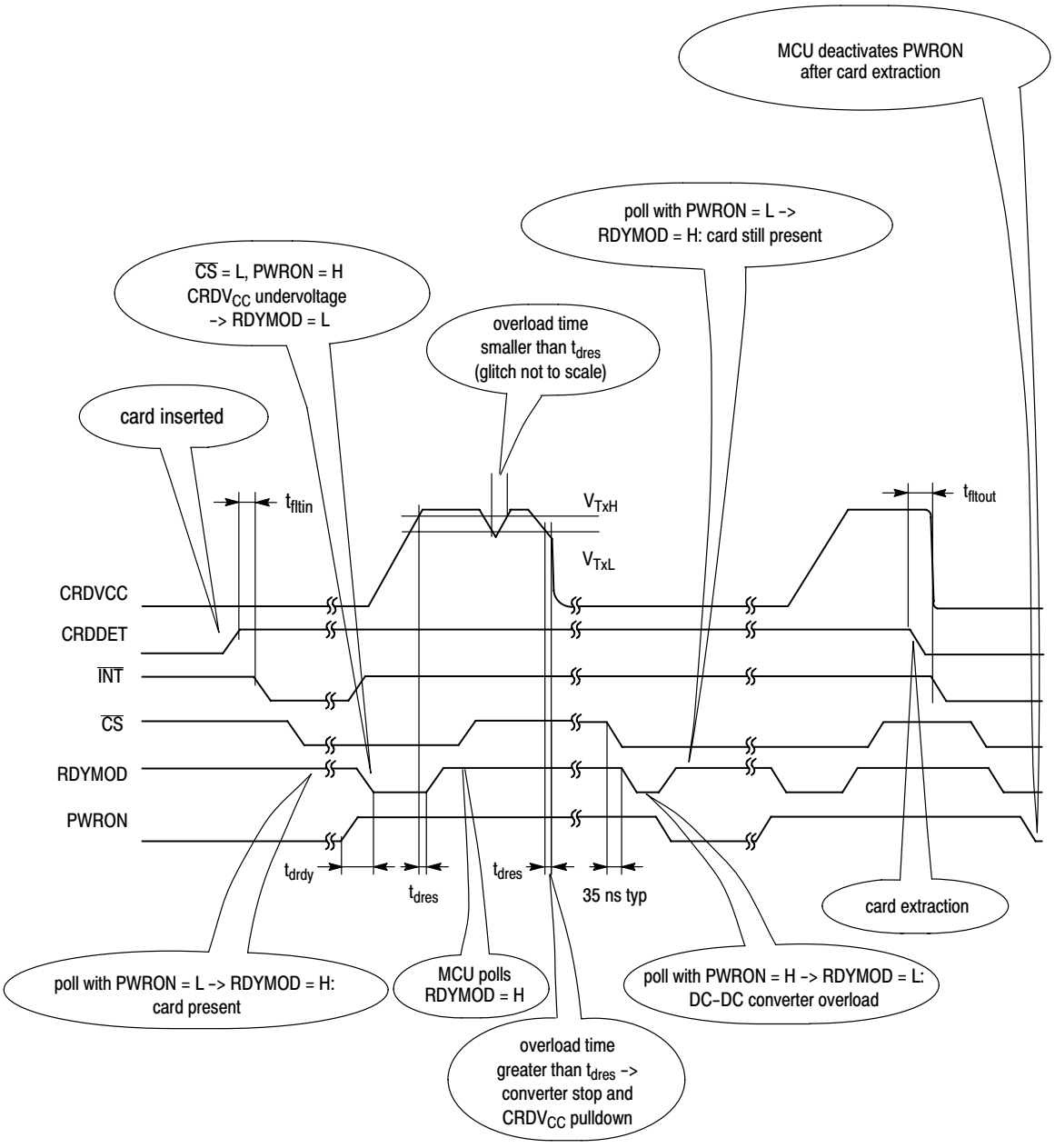


Figure 28. Card Signal Sequence During V_{CC} Overload and Unexpected Card Extraction

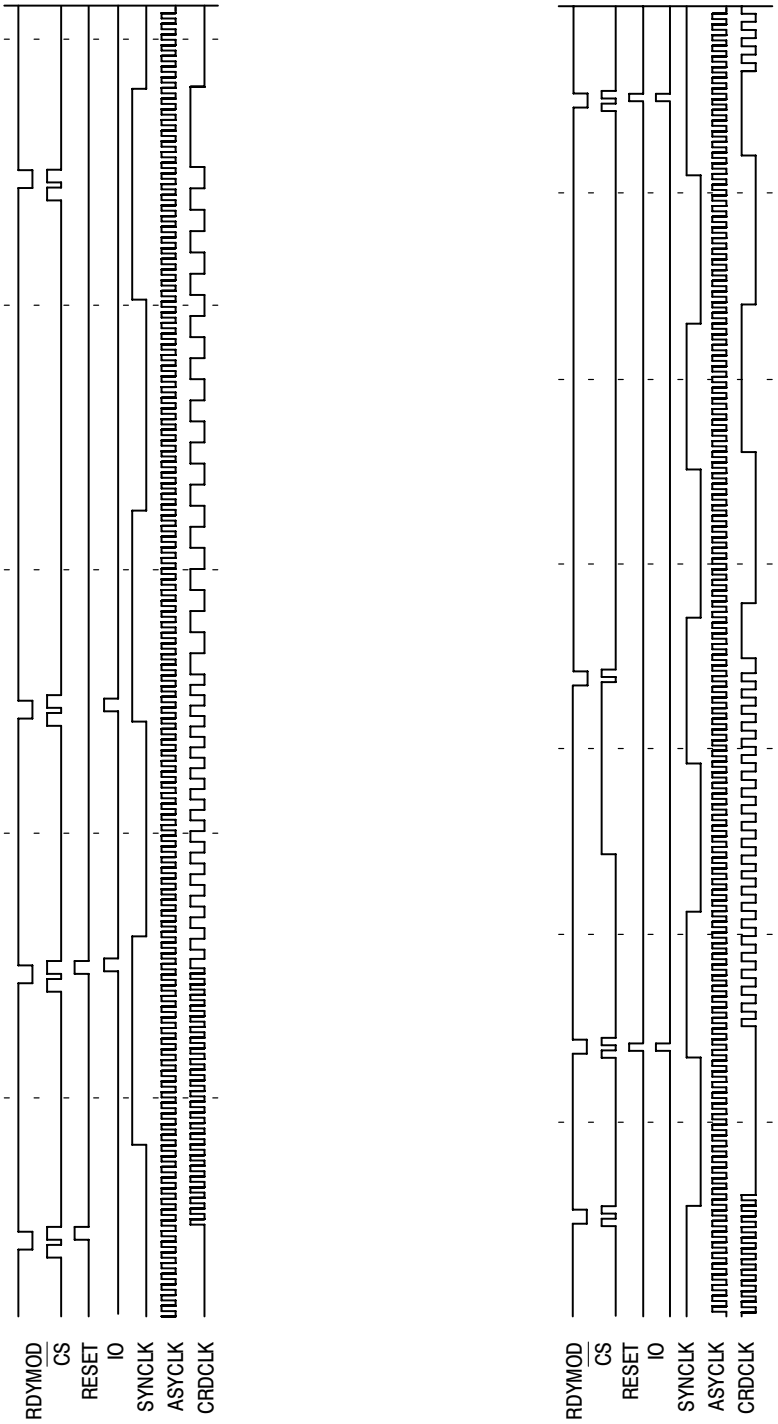


Figure 29. “On−the−Fly” Card Clock Selection Examples

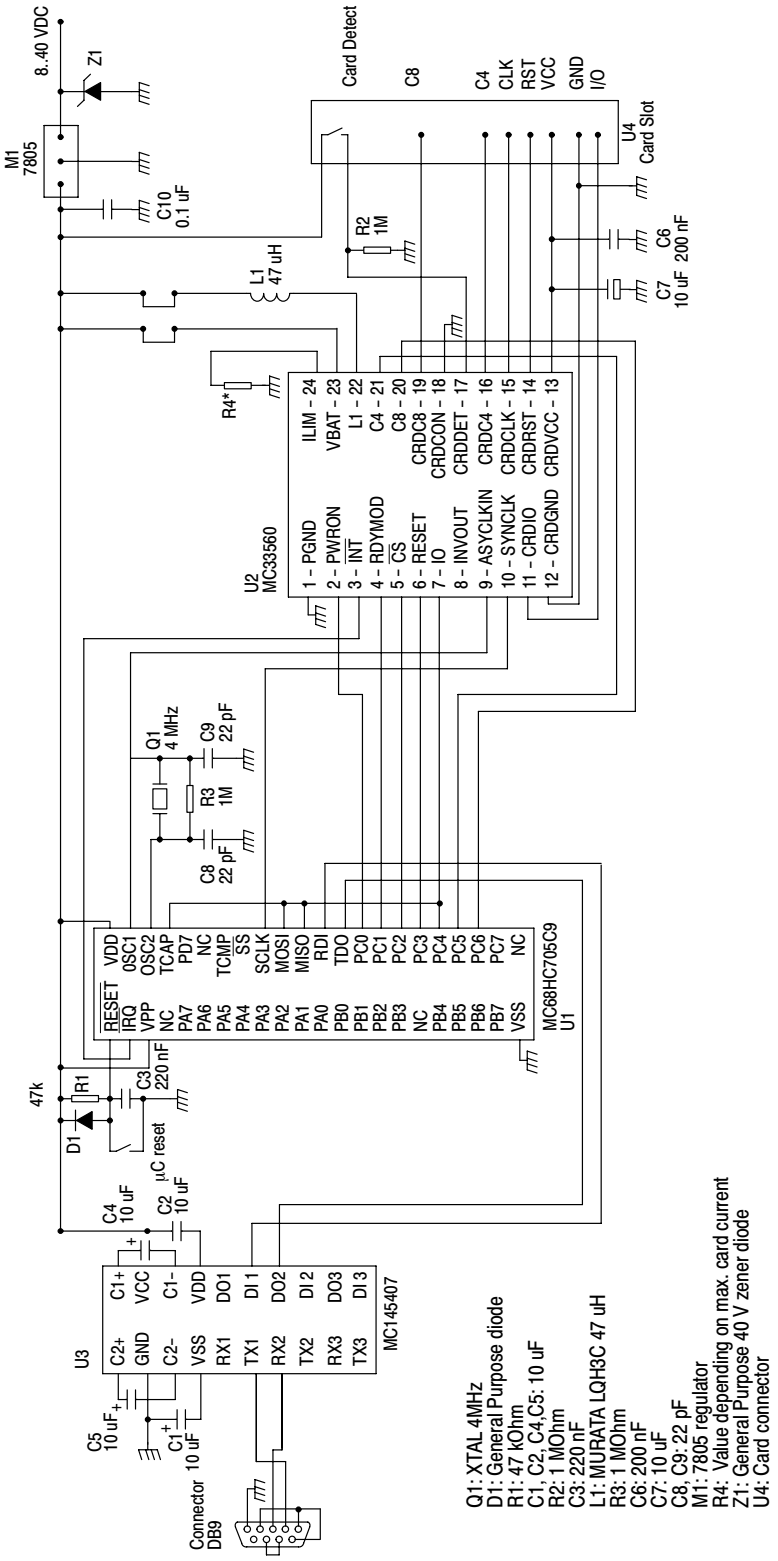


Figure 30. Card Reader/Writer Application

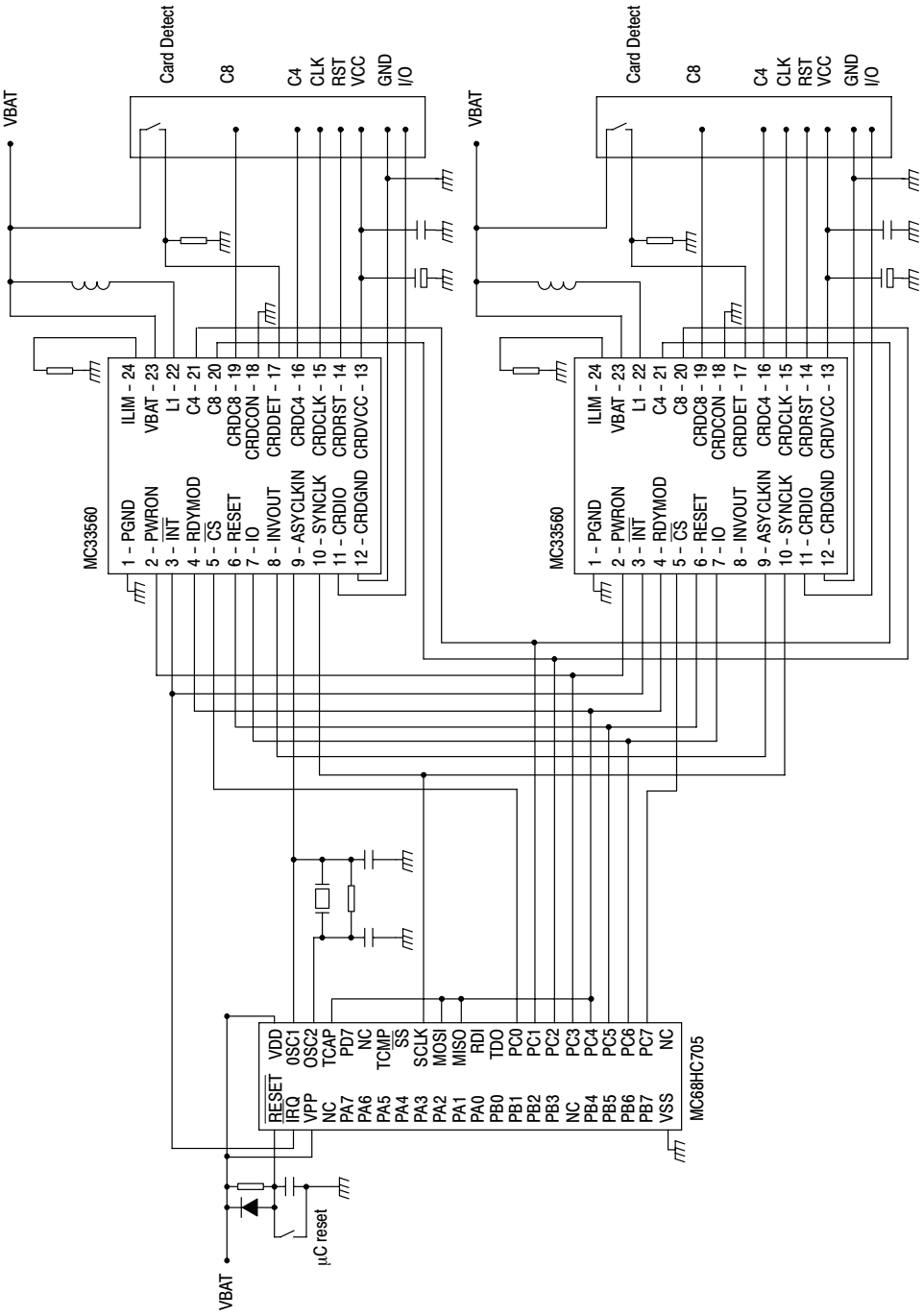


Figure 31. Multi Slot Card Reader/Writer Application

ORDERING INFORMATION

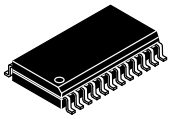
Device	Package	Shipping†
MC33560DTB	TSSOP−24	62 Units / Rail
MC33560DTBR2	TSSOP−24	2500 / Tape & Reel
MC33560DTBR2G	TSSOP−24 (Pb−Free)	2500 / Tape & Reel
MC33560DW	SO−24	30 Units / Rail
MC33560DWR2	SO−24	1000 / Tape & Reel
MC33560DWR2G	SO−24 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

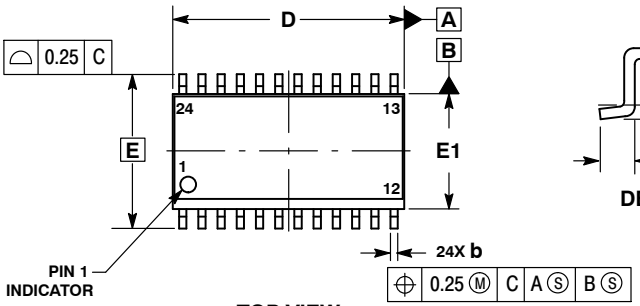
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

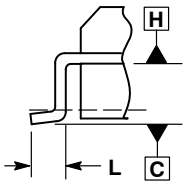
SOIC−24 WB
CASE 751E−04
ISSUE F

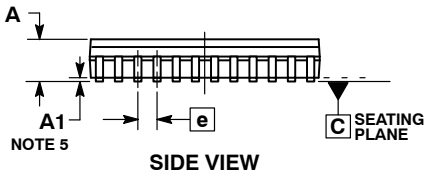
DATE 03 JUL 2012

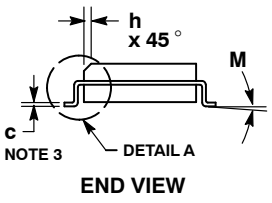


SCALE 1:1





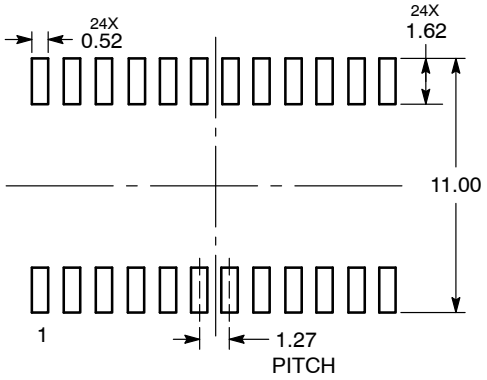




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
b	0.35	0.49
c	0.23	0.32
D	15.25	15.54
E	10.30 BSC	
E1	7.40	7.60
e	1.27 BSC	
h	0.25	0.75
L	0.41	0.90
M	0 °	8 °

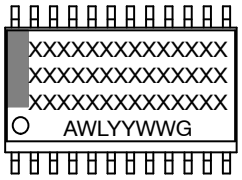
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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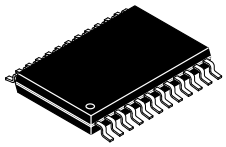
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

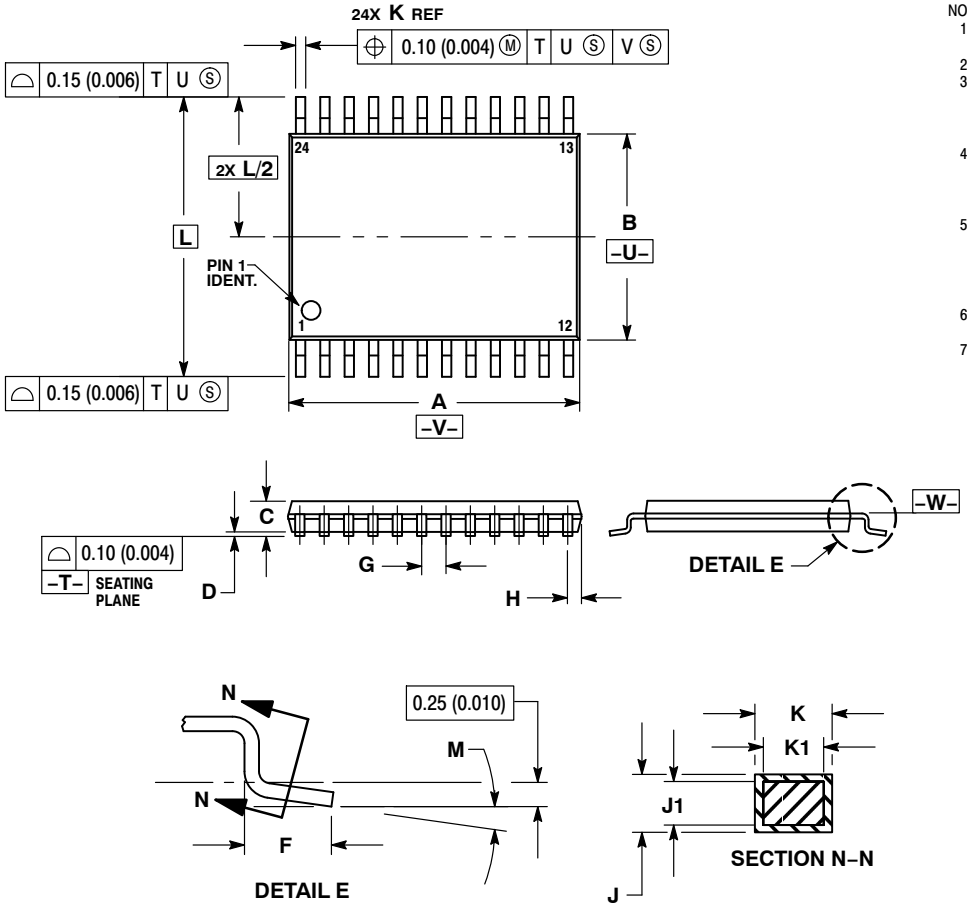
ON Semiconductor®

TSSOP24 WB
CASE 948K
ISSUE O

DATE 17 FEB 2000



SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	5.50	5.70	0.216	0.224
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	7.60 BSC		0.299 BSC	
M	0 °	8 °	0 °	8 °

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