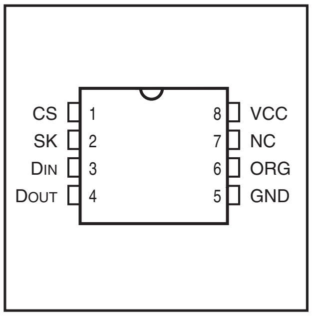
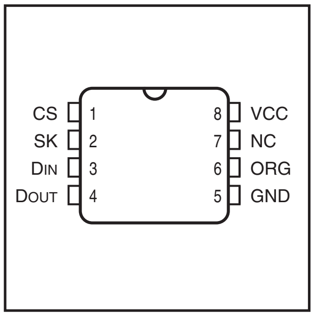
PIN CONFIGURATIONS

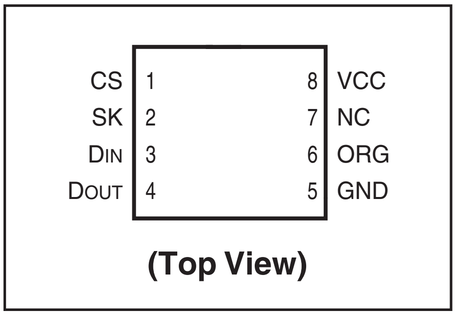
8-Pin DIP, 8-Pin TSSOP



8-Pin JEDEC SOIC "GR"



8-pad DFN



PIN DESCRIPTIONS

CS	Chip Select
SK	Serial Data Clock
DIN	Serial Data Input
DOUT	Serial Data Output
ORG	Organization Select
NC	Not Connected
Vcc	Power
GND	Ground

Applications

The IS93C46D is very popular in many applications which require low-power, low-density storage. Applications using this device include industrial controls, networking, and numerous other consumer electronics.

Endurance and Data Retention

The IS93C46D is designed for applications requiring up to 1M programming cycles (WRITE, WRALL, ERASE and ERAL). It provides 40 years of secure data retention without power after the execution of 1M programming cycles.

Device Operations

The IS93C46D is controlled by a set of instructions which are clocked-in serially on the Din pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the Din value must be stable at either LOW or HIGH. Each instruction begins with a start bit of the logical "1" or HIGH. Following this are the opcode (2 bits), address field (6 or 7 bits), and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock-speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

Read (READ)

The READ instruction is the only instruction that outputs serial data on the DOUT pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a serial shift register. (Please note that one logical "0" bit precedes the actual 8 or 16-bit output data string.) The output on DOUT changes during the low-to-high transitions of SK (see Figure 3).

Low Voltage Read

The IS93C46D has been designed to ensure that data read operations are reliable in low voltage environments. They provide accurate operation with Vcc as low as 1.8V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the IS93C46D has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When Vcc is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until Vcc is removed. (See Figure 4.) (Note: Chip select must remain LOW until Vcc reaches its operational value.)

Write (WRITE)

The WRITE instruction includes 8 or 16 bits of data to be written into the specified register. After the last data bit has been applied to DIN, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN).

If CS is brought HIGH, after a minimum wait of 200 ns (5V operation) after the falling edge of CS (tCS) DOUT will indicate the READY/$\overline{\text{BUSY}}$ status of the chip. Logical “0” means programming is still in progress; logical “1” means the selected register has been written, and the part is ready for another instruction (see Figure 5). The READY/$\overline{\text{BUSY}}$ status will not be available if: a) The CS input goes HIGH after the end of the self-timed programming cycle, tWP; or b) Simultaneously CS is HIGH, Din is HIGH, and SK goes HIGH, which clears the status flag.

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (tCS), the DOUT pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip (see Figure 6). Vcc is required to be above 4.5V for WRALL to function properly.

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

Erase Register (ERASE)

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of tCS, will cause DOUT to indicate the READ/$\overline{\text{BUSY}}$ status of the chip: a logical “0” indicates programming is still in progress; a logical “1” indicates the erase cycle is complete and the part is ready for another instruction (see Figure 8).

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical “1” (see Figure 9). Vcc is required to be above 4.5V for ERAL to function properly.

INSTRUCTION SET - IS93C46D (1Kb)

			8-bit Organization (ORG = GND)		16-bit Organization (ORG = Vcc)	
Instruction(2)	**Start Bit**	**OP Code**	**Address (1)**	**Input Data**	**Address (1)**	**Input Data**
READ	1	10	(A6-A0)	—	(A5-A0)	—
WEN (Write Enable)	1	00	11xxxxx	—	11xxxx	—
WRITE	1	01	(A6-A0)	(D7-D0)	(A5-A0)	(D15-D0)
WRALL (Write All Registers)	1	00	01xxxxx	(D7-D0)	01xxxx	(D15-D0)
WDS (Write Disable)	1	00	00xxxxx	—	00xxxx	—
ERASE	1	11	(A6-A0)	—	(A5-A0)	—
ERAL (Erase All Registers)	1	00	10xxxxx	—	10xxxx	—

Notes:

1. x = Don't care bit.
2. If the number of bits clocked-in does not match the number corresponding to a selected command, all extra trailing bits are ignored, and WRITE, WRALL, ERASE, ERAL are also ignored, and READ, WEN, WDS are accepted.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	–0.5 to +6.5	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	1.8V to 5.5V
Automotive	–40°C to +125°C	2.5V to 5.5V

Note: ISSI offers Industrial grade for Commercial applications (0°C to +70°C)

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C for Industrial and –40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	1.8V to 2.7V	—	0.2	V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.1mA	2.7V to 5.5V	—	0.4	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	1.8V to 2.7V	V_{CC} – 0.2	—	V
V_{OH1}	Output HIGH Voltage	I_{OH} = –400 µA	2.7V to 5.5V	2.4	—	V
V_{IH}	Input HIGH Voltage		1.8V to 2.7V 2.7V to 5.5V	0.7xV_{CC} 2.0	V_{CC}+1 V_{CC}+1	V
V_{IL}	Input LOW Voltage		1.8V to 2.7V 2.7V to 5.5V	–0.3 –0.3	0.2xV_{CC} 0.8	V
I_{LI}	Input Leakage	V_{IN} = 0V to V_{CC} (CS, SK, D_{IN}, ORG)		0	2.5	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to V_{CC}, CS = 0V		0	2.5	µA

Notes:

Automotive grade devices in this table are tested with Vcc = 2.5V to 5.5V and 4.5V to 5.5V. An operation with Vcc <2.5V is not specified.

POWER SUPPLY CHARACTERISTICS

T_A = –40°C to +85°C for Industrial, –40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	Vcc	Min.	Typ.	Max.	Unit
$I_{CC}1$	Vcc Read Supply Current	CS = V_{IH}, SK = 1 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels	1.8V 2.5V 5.0V	— — —	0.1 0.2 0.5	1 1 2	mA mA mA
$I_{CC}2$	Vcc Write Supply Current	CS = V_{IH}, SK = 1 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels	1.8V 2.5V 5.0V	— — —	0.5 1 2	1 2 3	mA mA mA
$I_{SB}1$	Standby Current	CS = GND, SK = GND ORG = Vcc or Floating (x16) D_{IN} = Vcc or GND	1.8V 2.5V 5.0V	— — —	0.1 0.1 0.2	1 2 4	µA µA µA
$I_{SB}2$	Standby Current	CS = GND, SK = GND ORG = GND (x8) D_{IN} = Vcc or GND	1.8V 2.5V 5.0V	— — —	6 6 10	10 10 15	µA µA µA

AC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C for Industrial

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
t_{SK}	SK Clock Frequency		1.8V ≤ Vcc < 2.5V	0	1	Mhz
			2.5V ≤ Vcc < 4.5V	0	2	Mhz
			4.5V ≤ Vcc ≤ 5.5V	0	3	Mhz
t_{SKH}	SK HIGH Time		1.8V ≤ Vcc < 2.5V	250	—	ns
			2.5V ≤ Vcc < 4.5V	200	—	ns
			4.5V ≤ Vcc ≤ 5.5V	200	—	ns
t_{SKL}	SK LOW Time		1.8V ≤ Vcc < 2.5V	250	—	ns
			2.5V ≤ Vcc < 4.5V	200	—	ns
			4.5V ≤ Vcc ≤ 5.5V	100	—	ns
t_{CS}	Minimum CS LOW Time		1.8V ≤ Vcc < 2.5V	250	—	ns
			2.5V ≤ Vcc < 4.5V	200	—	ns
			4.5V ≤ Vcc ≤ 5.5V	200	—	ns
t_{CSS}	CS Setup Time	Relative to SK	1.8V ≤ Vcc < 2.5V	200	—	ns
			2.5V ≤ Vcc < 4.5V	100	—	ns
			4.5V ≤ Vcc ≤ 5.5V	50	—	ns
t_{DIS}	Din Setup Time	Relative to SK	1.8V ≤ Vcc < 2.5V	100	—	ns
			2.5V ≤ Vcc < 4.5V	50	—	ns
			4.5V ≤ Vcc ≤ 5.5V	50	—	ns
t_{CSH}	CS Hold Time	Relative to SK	1.8V ≤ Vcc < 2.5V	0	—	ns
			2.5V ≤ Vcc < 4.5V	0	—	ns
			4.5V ≤ Vcc ≤ 5.5V	0	—	ns
t_{DIH}	Din Hold Time	Relative to SK	1.8V ≤ Vcc < 2.5V	50	—	ns
			2.5V ≤ Vcc < 4.5V	50	—	ns
			4.5V ≤ Vcc ≤ 5.5V	50	—	ns
t_{PD1}	Output Delay to “1”	AC Test	1.8V ≤ Vcc < 2.5V	—	400	ns
			2.5V ≤ Vcc < 4.5V	—	200	ns
			4.5V ≤ Vcc ≤ 5.5V	—	100	ns
t_{PD0}	Output Delay to “0”	AC Test	1.8V ≤ Vcc < 2.5V	—	400	ns
			2.5V ≤ Vcc < 4.5V	—	200	ns
			4.5V ≤ Vcc ≤ 5.5V	—	100	ns
t_{SV}	CS to Status Valid	AC Test	1.8V ≤ Vcc < 2.5V	—	400	ns
			2.5V ≤ Vcc < 4.5V	—	200	ns
			4.5V ≤ Vcc ≤ 5.5V	—	200	ns
t_{DF}	CS to Dout in 3-state	AC Test, CS=VIL	1.8V ≤ Vcc < 2.5V	—	100	ns
			2.5V ≤ Vcc < 4.5V	—	100	ns
			4.5V ≤ Vcc ≤ 5.5V	—	100	ns
t_{WP}	Write Cycle Time		1.8V ≤ Vcc < 2.5V	—	10	ms
			2.5V ≤ Vcc < 4.5V	—	5	ms
			4.5V ≤ Vcc ≤ 5.5V	—	5	ms

Notes:

1. C_L = 100pF

AC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +125°C for Automotive

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
f_{SK}	SK Clock Frequency		2.5V ≤ Vcc < 4.5V	0	2	Mhz
			4.5V ≤ Vcc ≤ 5.5V	0	3	Mhz
t_{SKH}	SK HIGH Time		2.5V ≤ Vcc < 4.5V	200	—	ns
			4.5V ≤ Vcc ≤ 5.5V	200	—	ns
t_{SKL}	SK LOW Time		2.5V ≤ Vcc < 4.5V	200	—	ns
			4.5V ≤ Vcc ≤ 5.5V	100	—	ns
t_{CS}	Minimum CS LOW Time		2.5V ≤ Vcc < 4.5V	200	—	ns
			4.5V ≤ Vcc ≤ 5.5V	200	—	ns
t_{CSS}	CS Setup Time	Relative to SK	2.5V ≤ Vcc < 4.5V	100	—	ns
			4.5V ≤ Vcc ≤ 5.5V	50	—	ns
t_{DIS}	Din Setup Time	Relative to SK	2.5V ≤ Vcc < 4.5V	50	—	ns
			4.5V ≤ Vcc ≤ 5.5V	50	—	ns
t_{CSH}	CS Hold Time	Relative to SK	2.5V ≤ Vcc < 4.5V	0	—	ns
			4.5V ≤ Vcc ≤ 5.5V	0	—	ns
t_{DIH}	Din Hold Time	Relative to SK	2.5V ≤ Vcc < 4.5V	50	—	ns
			4.5V ≤ Vcc ≤ 5.5V	50	—	ns
t_{PD1}	Output Delay to “1”	AC Test	2.5V ≤ Vcc < 4.5V	—	200	ns
			4.5V ≤ Vcc ≤ 5.5V	—	100	ns
t_{PD0}	Output Delay to “0”	AC Test	2.5V ≤ Vcc < 4.5V	—	200	ns
			4.5V ≤ Vcc ≤ 5.5V	—	100	ns
t_{SV}	CS to Status Valid	AC Test	2.5V ≤ Vcc < 4.5V	—	200	ns
			4.5V ≤ Vcc ≤ 5.5V	—	200	ns
t_{DF}	CS to Dout in 3-state	AC Test, CS=VIL	2.5V ≤ Vcc < 4.5V	—	100	ns
			4.5V ≤ Vcc ≤ 5.5V	—	100	ns
t_{WP}	Write Cycle Time		2.5V ≤ Vcc < 4.5V	—	5	ms
			4.5V ≤ Vcc ≤ 5.5V	—	5	ms

Notes:

1. C_L = 100pF

AC WAVEFORMS

FIGURE 2. SYNCHRONOUS DATA TIMING

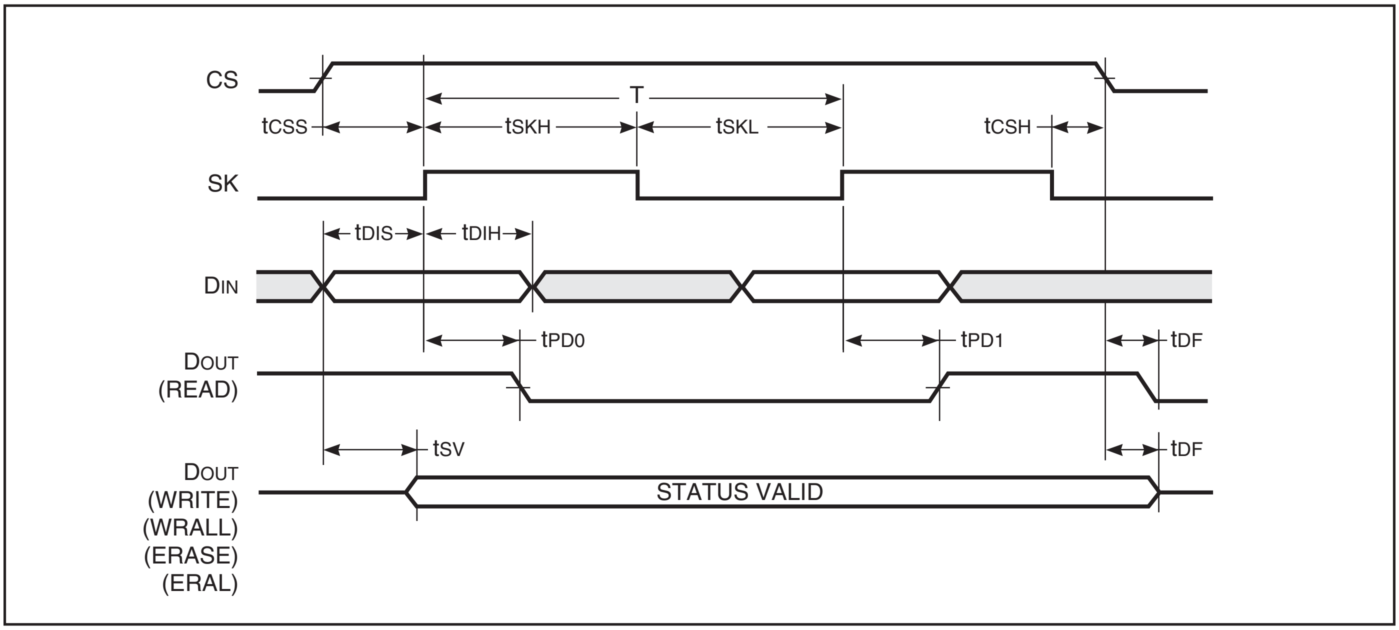
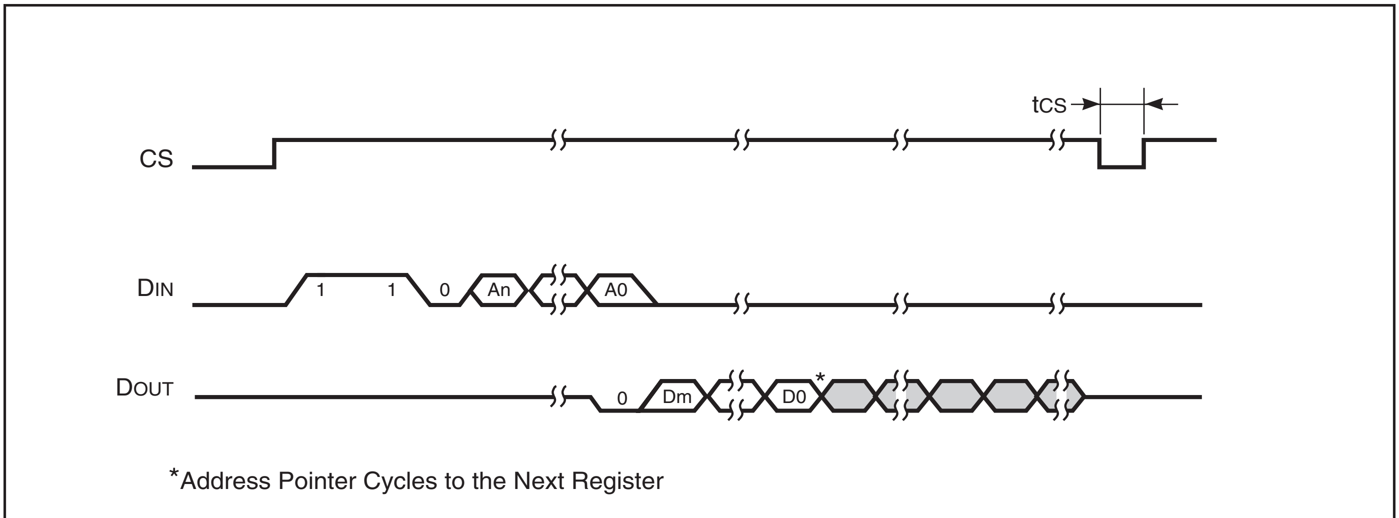


FIGURE 3. READ CYCLE TIMING



*Address Pointer Cycles to the Next Register

Notes:
To determine address bits An-A0 and data bits Dm-Do, see Instruction Set for the specific device.

AC WAVEFORMS

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

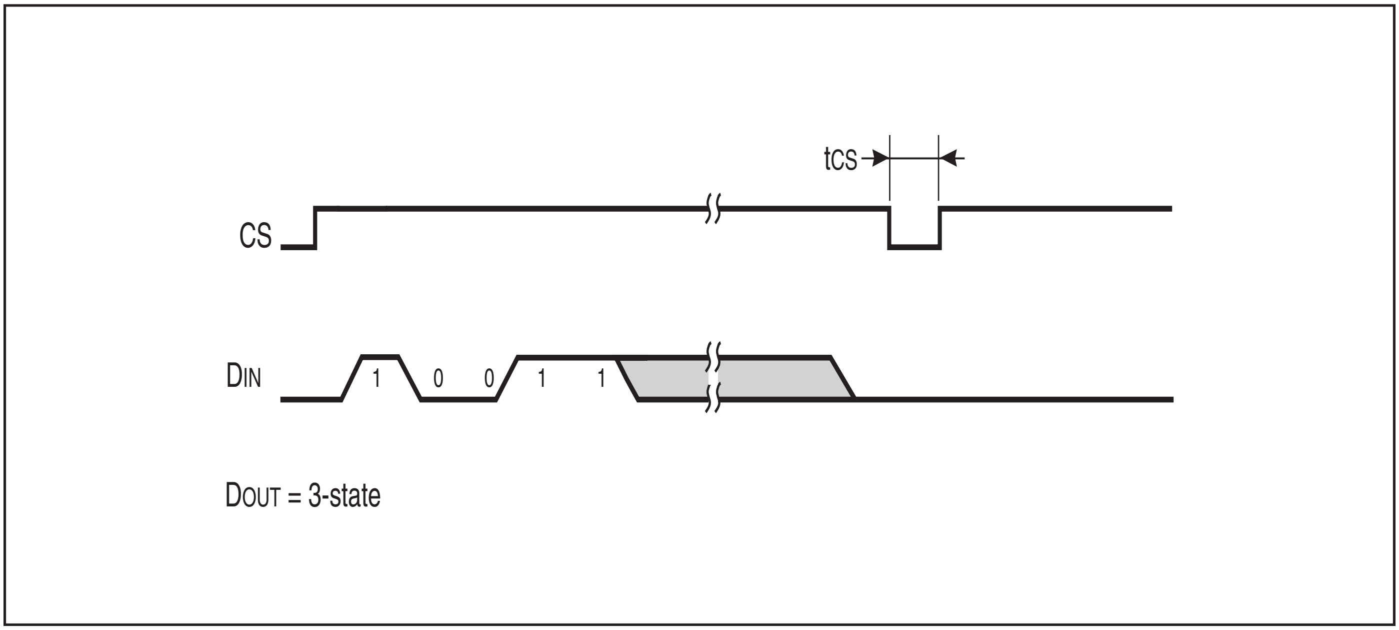
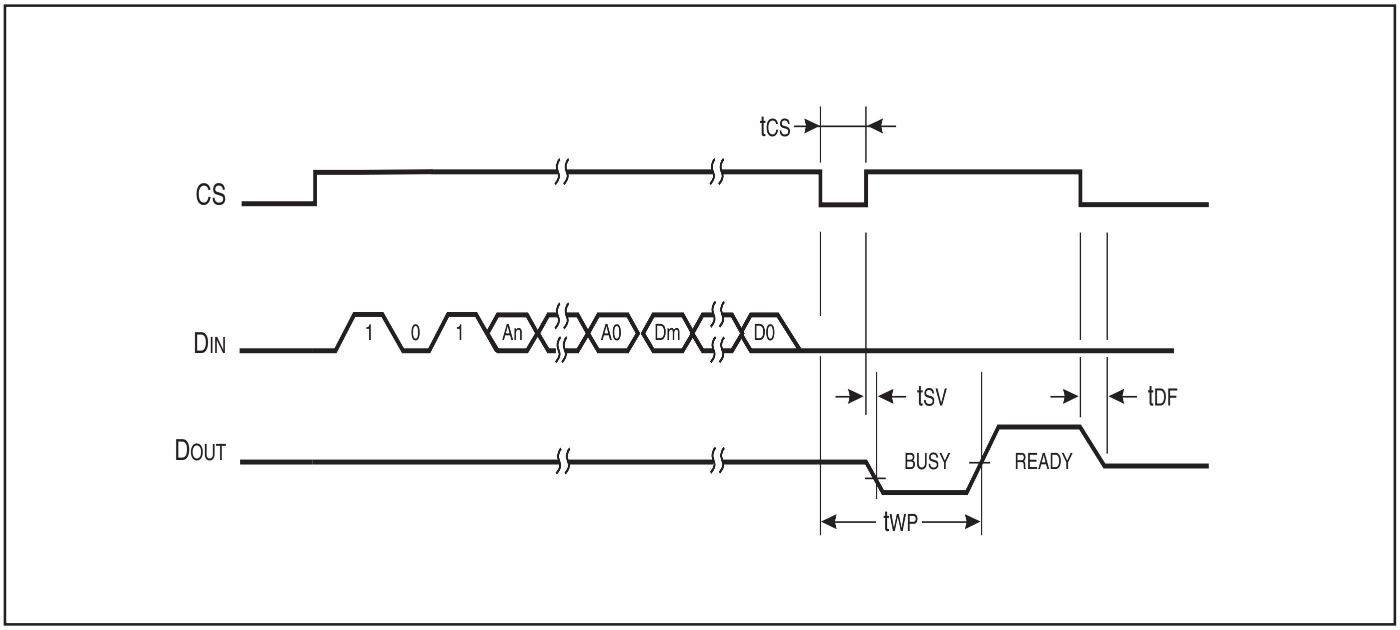


FIGURE 5. WRITE (WRITE) CYCLE TIMING

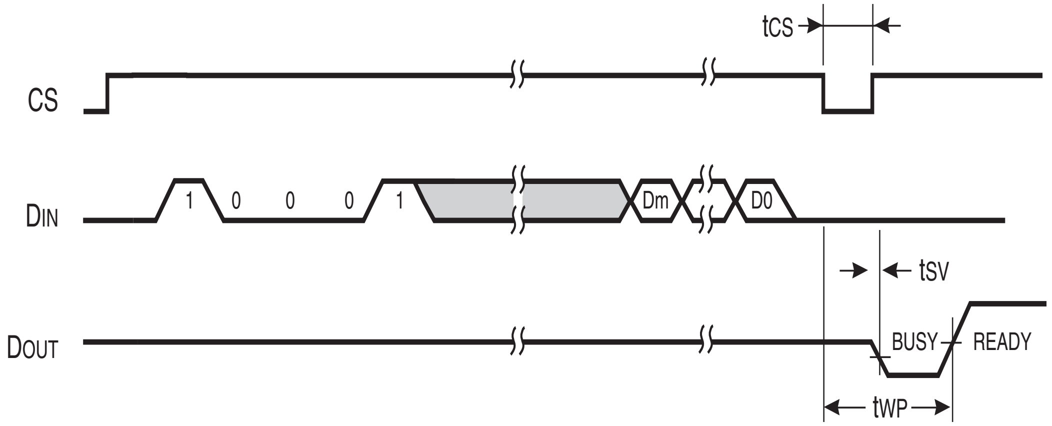


Notes:

1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in $\overline{\text{BUSY}}$ status (DOUT indicates $\overline{\text{BUSY}}$ status) then attempting to perform another instruction could cause device malfunction.
2. To determine address bits A_n-A_0 and data bits D_m-D_0, see Instruction Set for the specific device.

AC WAVEFORMS

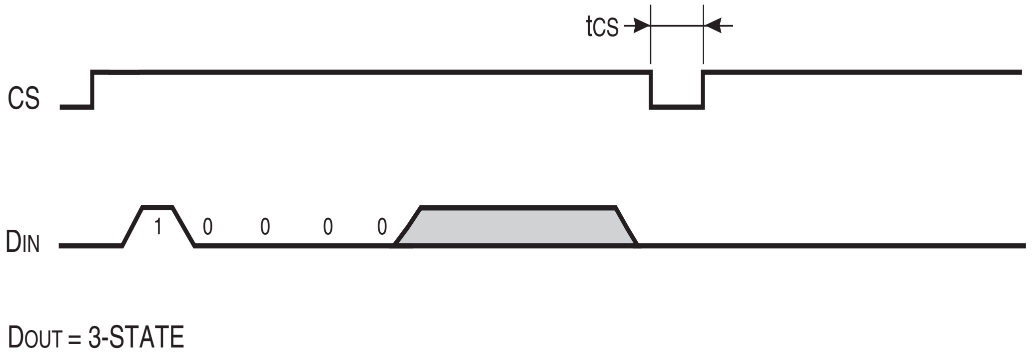
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



Notes:

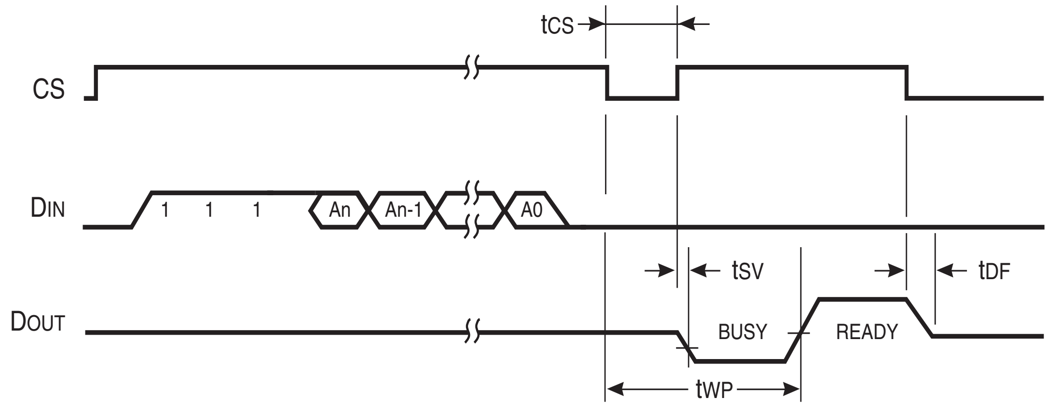
1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in $\overline{\text{BUSY}}$ status (DOUT indicates $\overline{\text{BUSY}}$ status) then attempting to perform another instruction could cause device malfunction.
2. To determine data bits Dm-D0, see Instruction Set for the appropriate device.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



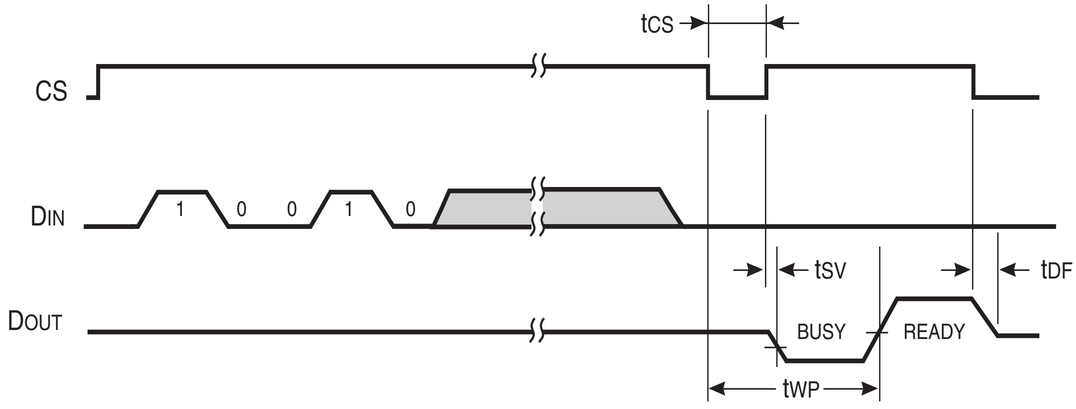
AC WAVEFORMS

FIGURE 8. ERASE (REGISTER ERASE) CYCLE TIMING



Notes:
To determine data bits An - A0, see Instruction Set for the appropriate device.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING



Note for Figures 8 and 9:

After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **$\overline{\text{BUSY}}$** status (DOUT indicates **$\overline{\text{BUSY}}$** status) then attempting to perform another instruction could cause device malfunction.

ORDERING INFORMATION

Industrial Range: -40ºC to +85ºC

Voltage Range	Order Part No.	Package
1.8V to 5.5V	IS93C46D-2PI	300-mil Plastic DIP
	IS93C46D-2GRI	SOIC JEDEC
	IS93C46D-2ZI	169-mil TSSOP

ORDERING INFORMATION

Industrial Range: -40ºC to +85ºC, Lead-free

Voltage Range	Order Part No.	Package
1.8V to 5.5V	IS93C46D-2PLI	300-mil Plastic DIP
	IS93C46D-2DLI	DFN
	IS93C46D-2GRLI	SOIC JEDEC
	IS93C46D-2ZLI	169-mil TSSOP

ORDERING INFORMATION

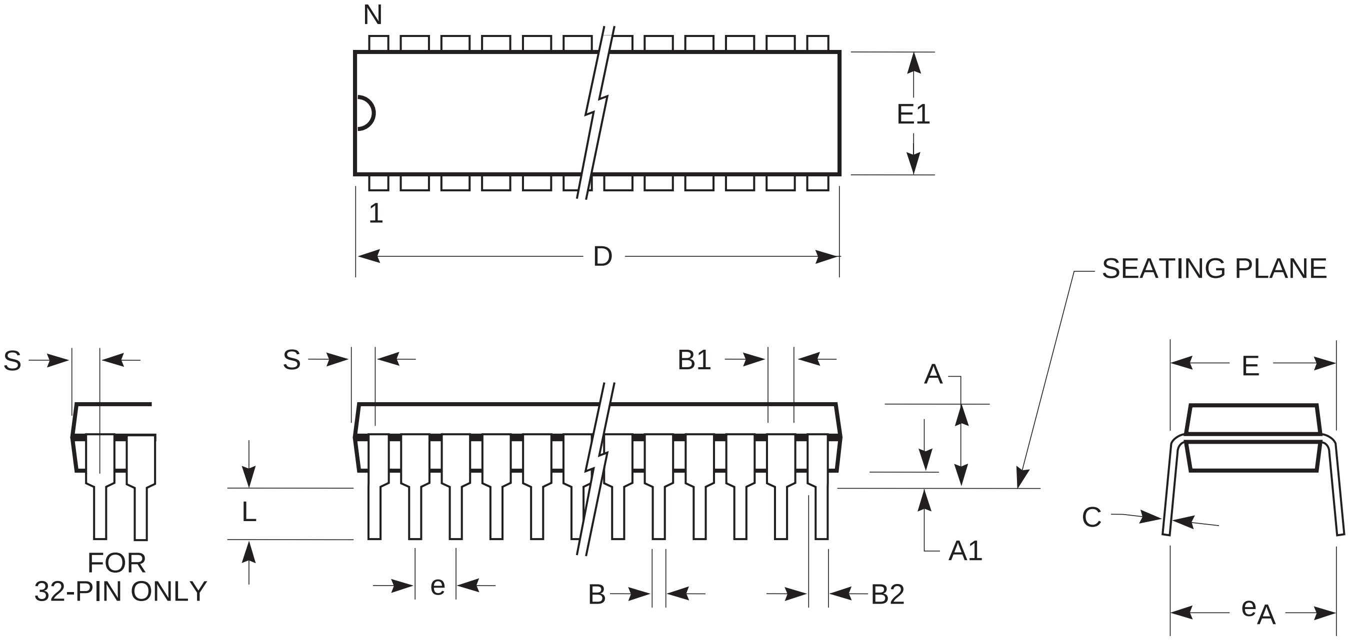
Automotive Range: -40ºC to +125ºC, Lead-free

Voltage Range	Order Part No.	Package
2.5V to 5.5V	IS93C46D-3PLA3	300-mil Plastic DIP
	IS93C46D-3GRLA3	SOIC JEDEC

PACKAGING INFORMATION

ISSI®

300-mil Plastic DIP
Package Code: N,P



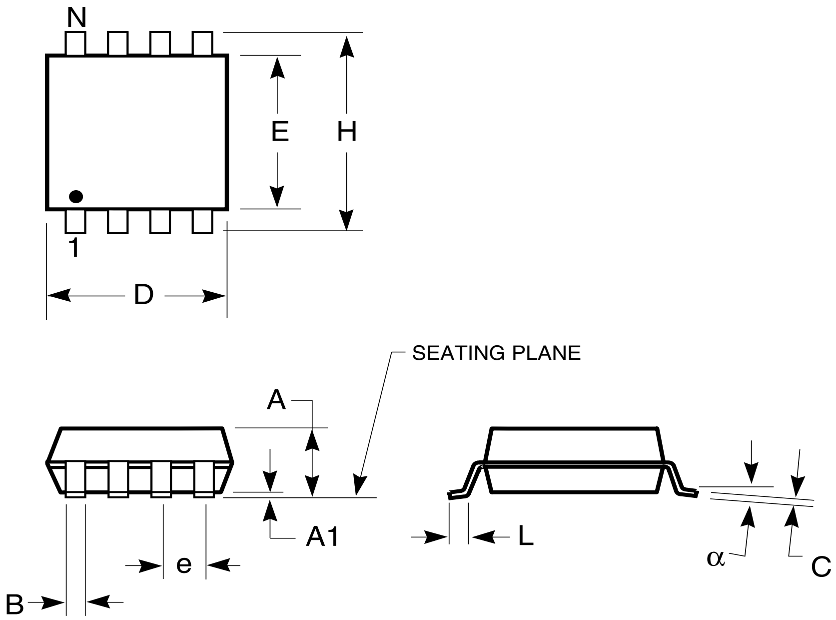
	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
N0. Leads	**8**			
A	3.68	4.57	0.145	0.180
A1	0.38	—	0.015	—
B	0.36	0.56	0.014	0.022
B1	1.14	1.52	0.045	0.060
B2	0.81	1.17	0.032	0.046
C	0.20	0.33	0.008	0.013
D	9.12	9.53	0.359	0.375
E	7.62	8.26	0.300	0.325
E1	6.20	6.60	0.244	0.260
e_A	8.13	9.65	0.320	0.380
e	2.54 BSC		0.100 BSC	
L	3.18	—	0.125	—
S	0.64	0.762	0.025	0.030

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

150-mil Plastic SOP
Package Code: G, GR

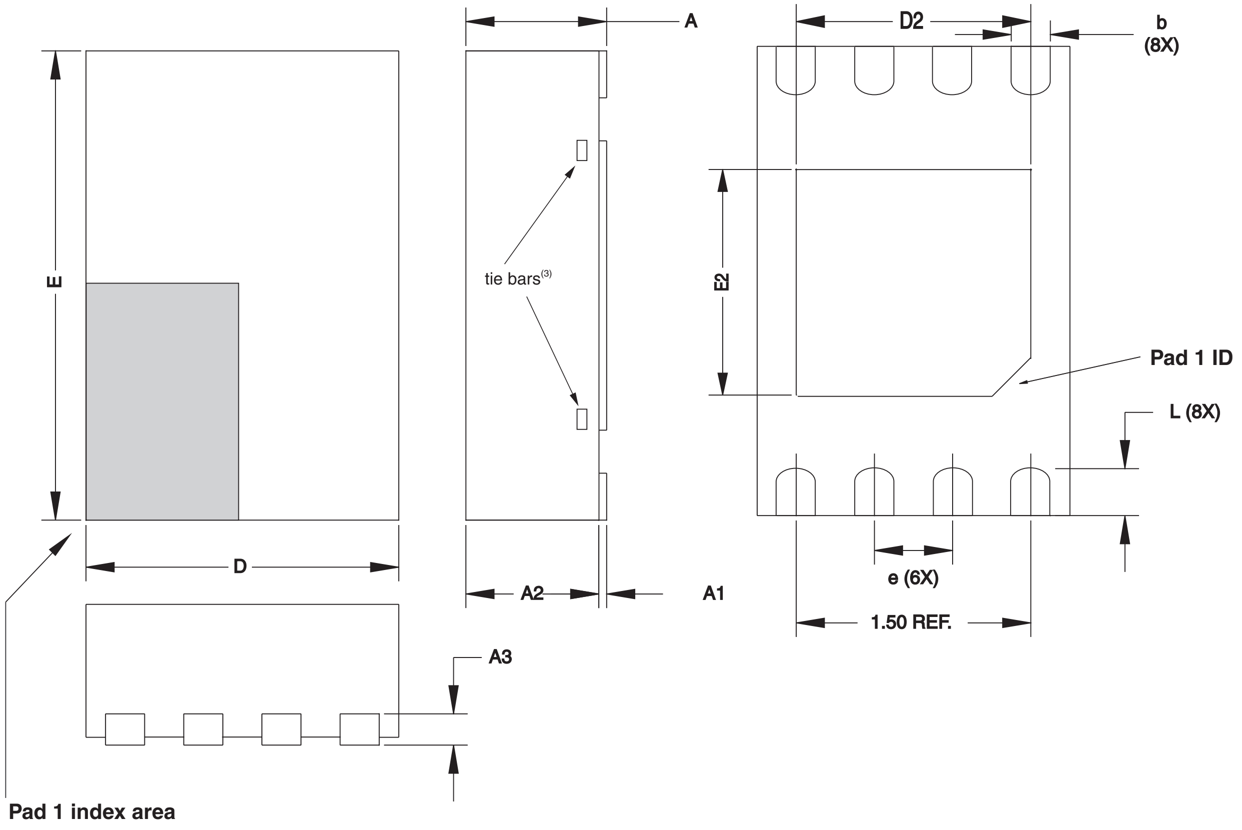


150-mil Plastic SOP (G, GR)				
Symbol	**Min**	**Max**	**Min**	**Max**
Ref. Std.	Inches		mm	
No. Leads	8		8	
A	—	0.068	—	1.73
A1	0.004	0.009	0.1	0.23
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.189	0.197	4.8	5
E	0.150	0.157	3.81	3.99
H	0.228	0.245	5.79	6.22
e	0.050 BSC		1.27 BSC	
L	0.020	0.035	0.51	0.89

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Dual Flat No-Lead
Package Code: D (8-pad)



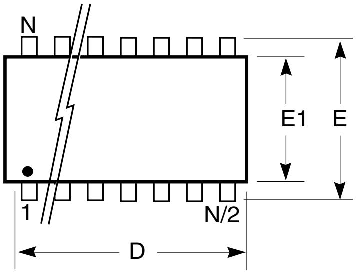
DFN

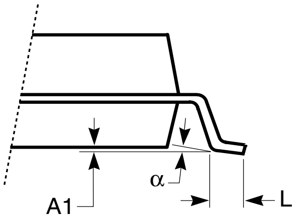
	MILLIMETERS		
Sym.	**Min.**	**Nom.**	**Max.**
N0. Pad		**8**	
D		2.00 BSC	
E		3.00 BSC	
D2	1.50	—	1.75
E2	1.60	—	1.90
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2	—	—	0.75
A3		0.20 REF	
L	0.30	0.40	0.50
e		0.50 BSC	
b	0.18	0.25	0.30

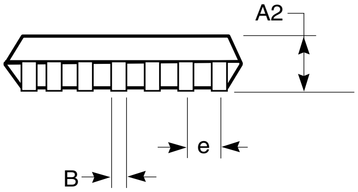
Notes:
1. Refer to JEDEC Drawing MO-229.
2. This is the metallized terminal and is measured between 0.18 mm and 0.30 mm from the terminal tip. The terminal may have a straight end instead of rounded.
3. Package may have exposed tie bars, ending flush with package edge.

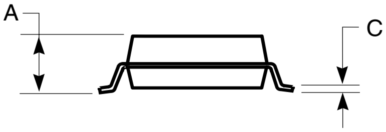
PACKAGING INFORMATION

Thin Shrink Small Outline TSSOP
Package Code: Z (8 pin, 14 pin)









TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	8			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E1	4.30	4.50	0.169	0.177
E	6.40 BSC		0.252 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
α	—	8°	—	8°

TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	14			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.193	0.201
E1	4.30	4.50	0.170	0.177
E	6.40 BSC		0.252 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.0177	0.0295
α	—	8°	—	8°