Ordering Information

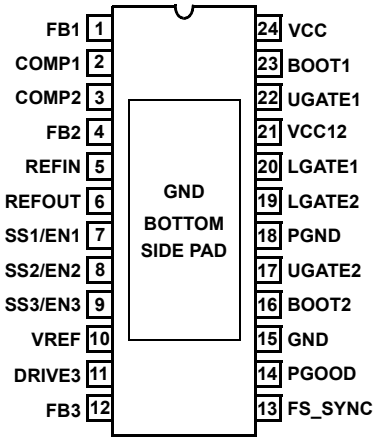
PART NUMBER	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6534CV	ISL6534CV	0 to 70	24 Ld EPTSSOP (exposed pad)	M24.173B
ISL6534CVZ (See Note)	ISL6534CVZ	0 to 70	24 Ld EPTSSOP (exposed pad) (Pb-free)	M24.173B
ISL6534CR	ISL6534CR	0 to 70	32 Ld 5x5 QFN	L32.5x5
ISL6534CRZ (See Note)	ISL6534CRZ	0 to 70	32 Ld 5x5 QFN (Pb-free)	L32.5x5
ISL6534EVAL2	EVAL board			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

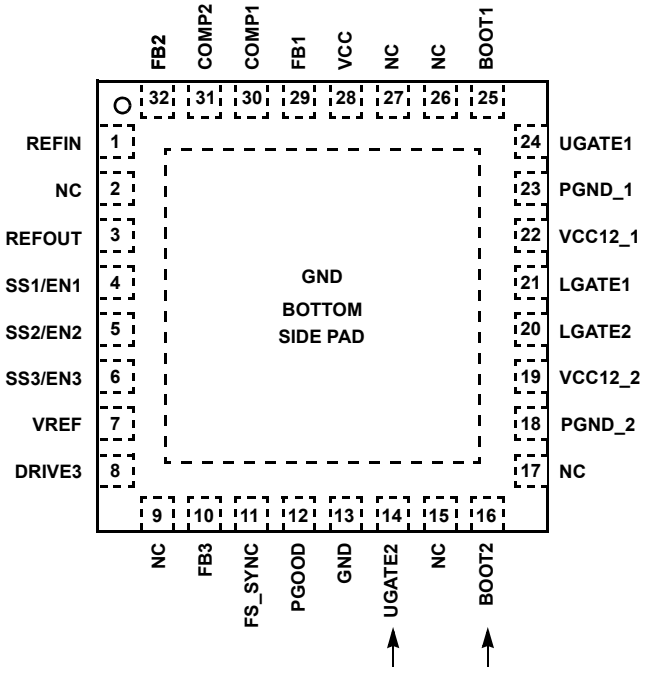
Add “-T” suffix for tape and reel.

Pinouts

24 LD EPTSSOP
TOP VIEW



32 LD 5x5 QFN
TOP VIEW



NOTES:

1. BOOT2 and UGATE2 are different order in QFN.
2. NC is No Connect

Block Diagram

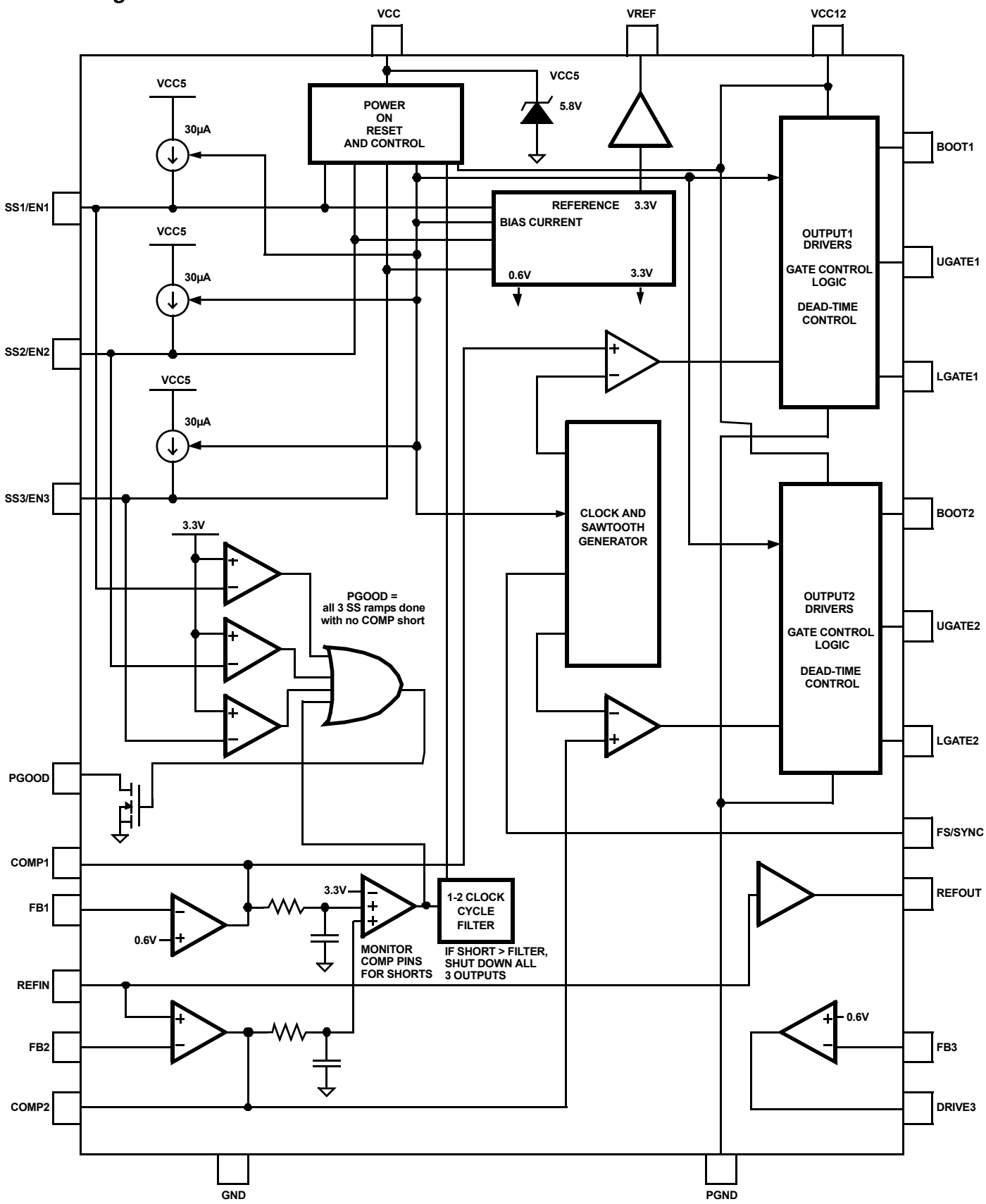
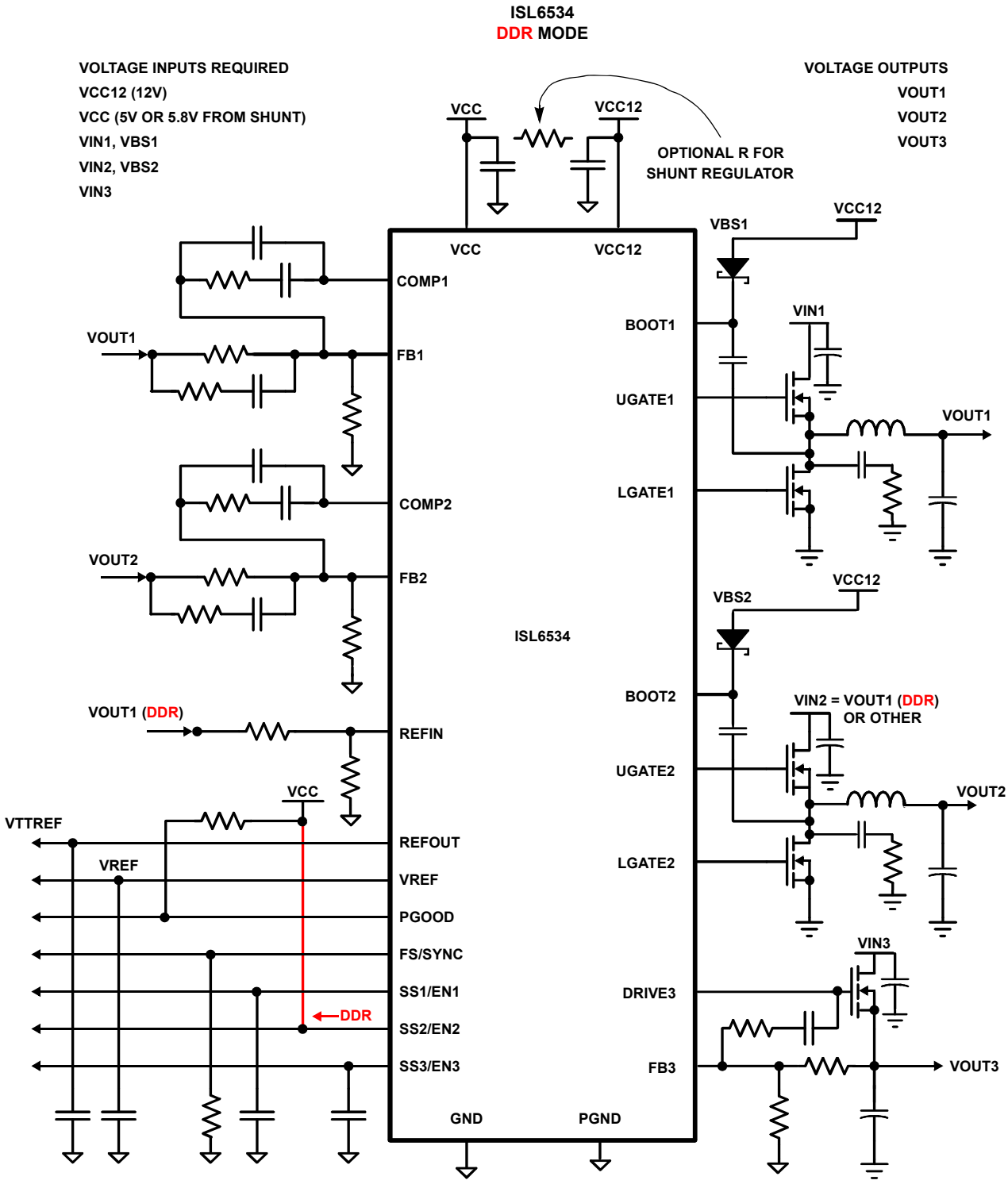


FIGURE 1. BLOCK DIAGRAM

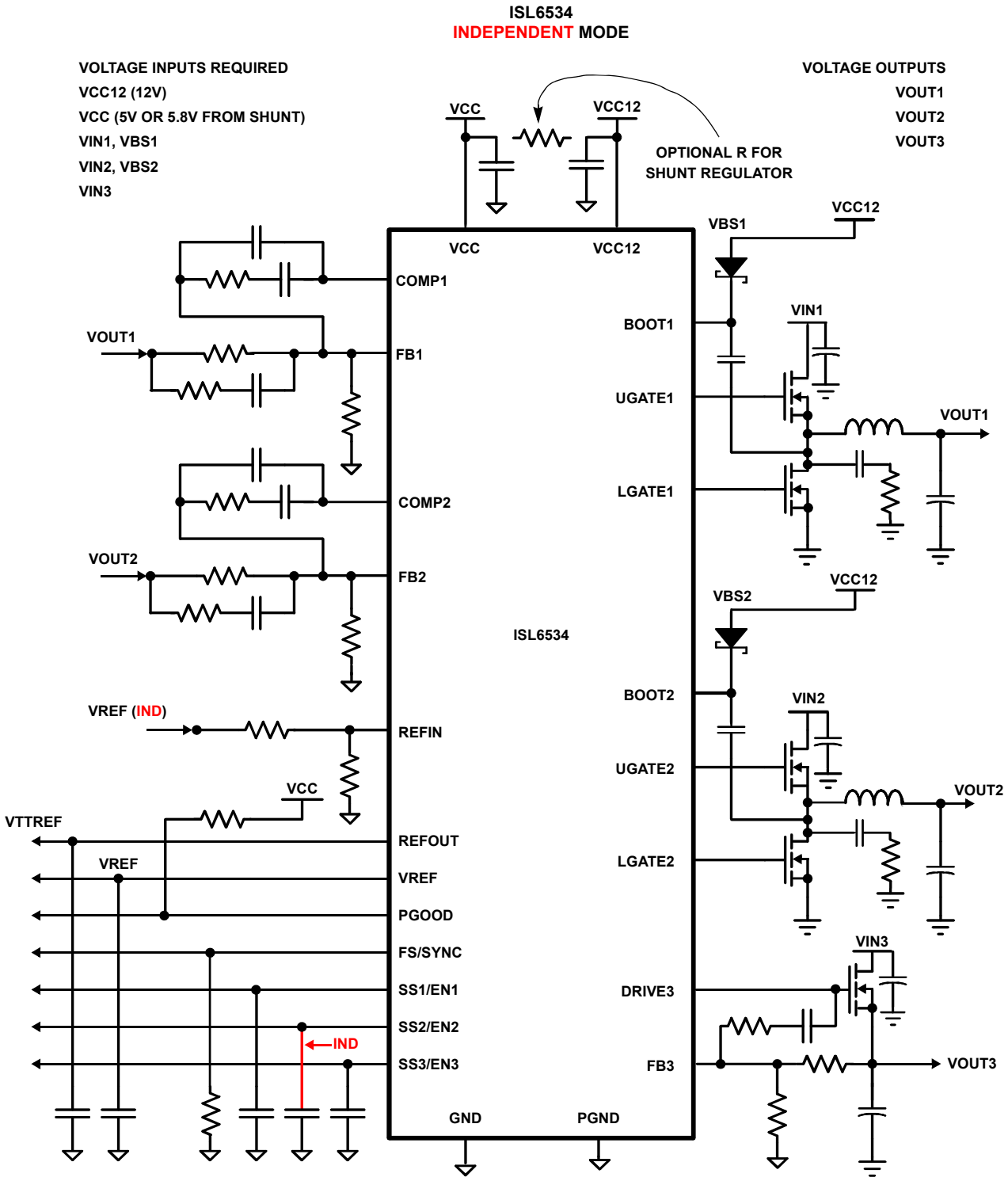
Typical Application, DDRAM Controller



NOTE: Not all components are necessary in all applications.

FIGURE 2. TYPICAL APPLICATION, DDRAM CONTROLLER

Typical Application, Independent Mode



NOTE: Not all components are necessary in all applications.

FIGURE 3. TYPICAL APPLICATION, INDEPENDENT MODE

Absolute Maximum Ratings

Supply Voltage (VCC12) . . . . . GND - 0.3V to 14.0V
Supply Voltage (VCC, separate supply). . . . . GND - 0.3V to 5.5V
Supply Voltage (VCC, shunt regulator) . . . . . GND - 0.3V to 6.0V
UGATE1, UGATE2, BOOT1, BOOT2 . . . . . GND - 0.3V to 36V
LGATE1, LGATE2, DRIVE3. . . . . GND - 0.3V to VCC12
FS_SYNC (through 10k resistor) . . . . . GND - 0.3V to 12V
REFIN, REFOUT, PGOOD, VREF. . . . . GND - 0.3V to VCC
FB1, COMP1, FB2, COMP2, FB3 . . . . . GND - 0.3V to VCC
SS1/EN1, SS2/EN2, SS3/EN3. . . . . GND - 0.3V to VCC
PGND. . . . . GND - 0.3V to GND + 0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 1500V
Machine Model (Per EIAJ ED-4701 Method C-111). 100V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . . 1000V

Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TSSOP Package	37	4
QFN Package	32	4

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range. . . . . 0°C to 70°C
VCC12 Supply Voltage Range (Typical) . . . . . 12V ±1.2V
VCC Supply Voltage Range (Typical) . . . . . 5V ±0.25V
VCC Shunt Regulator Voltage Range (Typical). . . . . 5.8V ±0.2V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, V_{CC12} = 12V, T_A = 0°C to 70°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY POWER					
Input Supply Current (Quiescent)	VCC; outputs disabled		4		mA
	VCC12; outputs disabled		6		mA
Input Supply Current (Dynamic)	VCC12; UGATEs, LGATEs CL = 1nF, 300kHz		50		mA
	VCC; UGATEs, LGATEs CL = 1nF, 300kHz		7		mA
Shunt Regulator Output Voltage	40mA current; ~equivalent to 150Ω resistor VCC to 12V	5.6	5.8	6.0	V
Shunt Regulator Current	150Ω resistor VCC to 12V		40		mA
Power-On Reset Threshold	VCC rising	4.15	4.23	4.5	V
	VCC falling	3.8	4.0	4.15	V
	VCC12 rising		7.8		V
	VCC12 falling		7.3		V
SYSTEM ACCURACY					
Output 1 (measured at FB1)	VCC = 4.75 to 5.25V; T_A = 0°C to 70°C; (Note 5)	0.5997	0.6070	0.6142	V
Output 3 (measured at FB3)	VCC = 4.75 to 5.25V; T_A = 0°C to 70°C; (Note 5)	0.6027	0.6100	0.6173	V
Output 1 (measured at FB1)	VCC = ~5.8V (@ 20mA shunt current); T_A = 0°C to 70°C; (Note 5)	0.6027	0.6100	0.6173	V
Output 3 (measured at FB3)	VCC = ~5.8V (@ 20mA shunt current); T_A = 0°C to 70°C; (Note 5)	0.6057	0.6130	0.6203	V
Min Output Voltage (VOUT1, VOUT2)	(Note 9)		0.6		V
Max Output Voltage (VOUT1, VOUT2)	(Note 9)		6.0		V
OSCILLATOR					
Accuracy		-20		20	%
Frequency	FS_SYNC pin to GND	240	300	360	kHz
Adjustment Range	FS_SYNC pin: resistor to GND; (see Figure 12 for curves)	300		1000	kHz
Sawtooth Amplitude	(Note 7)		2.1		V
Duty-Cycle Range		0		87.5	%

Electrical Specifications Operating Conditions: V_{CC} = 5V, V_{CC12} = 12V, T_A = 0°C to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER (OUT1 and OUT2)					
Open-Loop Gain	RL = 10kΩ to ground; (Note 7)		85		dB
Open-Loop Bandwidth	CL = 100pF, RL = 10kΩ to ground; (Note 7)		15		MHz
Slew Rate	CL = 100pF, RL = 10kΩ to ground; (Note 7)		4		V/µs
EA Offset	COMP1/2 to FB1/2; compare to internal VREF/REFIN; (Note 7)		2		mV
Maximum Output Voltage	V_{CC} = 5V; RL = 10kΩ to ground; (may trip short-circuit)	3.6	4.1		V
Output High Source Current	COMP1/2		-8		mA
Output Low Sink Current	COMP1/2		6		mA
PROTECTION AND MONITOR					
Undervoltage Threshold (COMP1 and COMP2)	Causes PGOOD to go low; if there for a filter time, Implies the COMP pin(s) is out -of-range, and shuts down IC		3.3		V
UV Filter Time	Based on internal oscillator clock frequency (nominal 300kHz = 3.3µs clock period)		1-2		clock pulses
PGOOD Low Voltage	IPGOOD = 2mA		0.1	0.3	V
LINEAR REGULATOR (OUT3)					
Min Output Voltage	(As determined by resistor divider into FB3); (Note 8)		0.6		V
Max Output Voltage	(As determined by resistor divider into FB3); (Note 8)		3.3		V
EA Offset	DRIVE3 to FB3; compare to internal VREF; (Note 7)		2		mV
DRIVE3 High Output Voltage			9		V
DRIVE3 High Output Source Current			0.4		mA
DRIVE3 Low Output Sink Current			0.4		mA
VREF					
Output Voltage	VCC = 4.75 to 5.25V; T_A = 0°C to 70°C; (Note 5) 1.1µF max capacitance	3.244	3.307	3.370	V
Output Voltage	VCC = ~5.8V (@ 20mA shunt current); T_A = 0°C to 70°C; (Note 5)	3.285	3.335	3.385	V
Source Current				2.0	mA
REFIN					
Input Offset Voltage		-2.5		+2.5	mV
Common Mode Input Range	VCC can be external or internal shunt regulator voltage	0.6		VCC-1.8	V
REFOUT (VTTREF)					
Min Output Voltage	Determined by REFIN voltage		0.6		V
Max Output Voltage	Determined by REFIN voltage		3.3		V
Offset Voltage	REFIN = 3.3V	-10		+10	mV
Source Current		0.2		20	mA
Sink Current				0.48	mA
Min Output Capacitance	External		0.4		µF
Max Output Capacitance	External		2.2		µF
Output High Voltage Minimum	To select 0 degree phase; (see Table 1)		4.7	VCC	V

Electrical Specifications Operating Conditions: V_{CC} = 5V, V_{CC12} = 12V, T_A = 0°C to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/SOFT-START (SS/EN 1, 2, 3)					
Enable Threshold	EN Rising		1.05		V
	EN falling		0.95		V
Noise Immunity (noise de-glitch)	(Note 7)		6		µs
Soft-Start Current	I_{SS}		-30		µA
Soft-Start High Voltage	End of ramp		3.3V		V
Output High Voltage	To select DDR mode; (see Table 1)		4.7	VCC	V
FS/SYNC PLL					
Min Frequency Range of Lock-In			300		kHz
Max Frequency Range of Lock-In			1000		kHz
Maximum High Voltage	Use a 10k series resistor (from LG pin of another IC, for example)		12		V
BOOT PINS (BOOT1, 2)					
High Voltage	Maximum DC Voltage with respect to GND; also depends upon VIN, Phase, VOUT, and threshold of NFET; ringing should not exceed max rating of BOOT (36V)		27		V
GATE DRIVERS					
Output Voltage	UGATE1, UGATE2; DC maximum voltage		27		V
Output Voltage	LGATE1, LGATE2; DC maximum voltage = VCC12		13.2		V
Upper Driver Source Resistance	UGATE1, UGATE2 = 3V; BOOT = 12V; I_{GATE} = 100mA		2		Ω
Lower Driver Source Resistance	LGATE1, LGATE2 = 3V; I_{GATE} = 100mA		2		Ω
Upper Driver Sink Resistance	UGATE1, UGATE2 = 3V; BOOT = 12V; I_{GATE} = 100mA		2.8		Ω
Lower Driver Sink Resistance	LGATE1, LGATE2 = 3V; I_{GATE} = 100mA		2.8		Ω
GATE DRIVERS SWITCHING TIME					
UGATE Rise Time	10% - 90%; 2nF Load; BOOT = 12V		17		ns
UGATE Fall Time	90% - 10%; 2nF Load; BOOT = 12V		17		ns
UGATE Rise Time	10% - 90%; 2nF Load; BOOT = 24V		27		ns
UGATE Fall Time	90% - 10%; 2nF Load; BOOT = 24V		25		ns
LGATE Rise Time	10% - 90%; 2nF Load		17		ns
LGATE Fall Time	90% - 10%; 2nF Load		17		ns

NOTES:

5. Operating range is: 12V ±10%; 5V ±5% for no shunt regulator; 12V ±10%; VCC5 = ~5.8V (approximate shunt voltage at a shunt current of 20mA). The accuracy specs are slightly different for the two cases.
6. Thermal comments.
7. Design guidance only; not production tested.
8. The maximum output voltage of VOUT3 can go higher than 3.3V, with the proper precautions. These include making sure: the input voltage is higher than the desired output, with sufficient current available; the DRIVE3 voltage can go high enough to drive the FET, with an acceptable V_{GS} for the load current desired; the FET is chosen and mounted to handle the power dissipation at full load.
9. The maximum output voltage of VOUT1 and VOUT2 is determined by the following factors: the VIN (usually 12V or less; take into account its min and max variation as well); the maximum duty cycle (with a perfect 12V input, that limits the output to 10.5V); the bootstrap voltage used; the FETs chosen. Since the upper FET will be on most of the time, it must be sized accordingly. The output capacitors also need to be rated for the higher voltage.

Pin Description

VCC

This power pin supplies bias to the control functions. It can be connected to a nominal 5V (±5%) supply, or it can function as a shunt regulator (nominal 5.8V), with an external pull-up resistor (nominally 150Ω to 12V).

GND

This pin is the signal ground for the IC. The metal thermal pad under both packages is connected to the GND potential (through the IC substrate; the pad does NOT substitute for the GND pin connection). But the GND pin and the metal pad should be connected together on the board, and tied to a good GND plane (both for electrical and thermal conduction). The thermal pad on both packages limits metal interconnect traces underneath the package.

VCC12 (QFN: VCC12_1, VCC12_2)

This power pin (nominal 12V) supplies the output gate drivers, as well as some other control functions.

The QFN package has two power pins; one for each switcher. They are electrically connected internally, but allow for separate decoupling caps to better isolate the switching noise, if necessary. Even if they share one capacitor, they should both be connected externally, for lower resistance.

PGND (QFN: PGND_1, PGND_2)

This pin is the Power GND for the gate drive circuits. It is not directly tied to GND inside the IC; it should be tied to GND on the board.

The QFN package has two Power GNDs; one local to each switcher; both should be connected externally to the GND plane on the board.

SS1/EN1, SS2/EN2, SS3/EN3

These analog input pins have two functions. A 30µA current source charges an external capacitor (to GND), to provide a soft-start timing ramp; their respective Output voltage will follow the ramp voltage as it powers up. The 2nd function is Enable; when the input is left open (with the soft-start cap), the respective output will be Enabled after the ramp reaches the 1V level. If the input is pulled to a low logic level, the output will be disabled.

SS2/EN2 also has a special mode function; see Table 1. Tying it to VCC (5V) selects the DDR mode (where both OUT1 and OUT2 share the SS1 ramp); otherwise it will be in the Independent mode.

COMP1, COMP2

These analog output pins are used to externally compensate the error amplifiers for their respective regulators.

FB1, FB2, FB3

These analog input pins are used to set their respective regulator output voltages. A resistor divider from the output to GND is compared to a reference voltage (0.6V for OUT1 and OUT3; REFIN pin for OUT2). The compensation components also connect to these pins.

UGATE1, UGATE2

These output pins provide the gate drive for the upper MOSFETs of OUT1 and OUT2 respectively; the voltage comes from its bootstrap pin, typically 12V (minus the diode drop) above the VCC12 pin.

LGATE1, LGATE2

These output pins provide the gate drive for the lower MOSFETs of OUT1 and OUT2 respectively; the voltage comes from VCC12.

BOOT1, BOOT2

These pins feed the bootstrap voltage (externally generated with a diode and a capacitor) to the upper MOSFETs, through the UGATE pins. Either BOOT pin can be connected directly to a power supply instead (but only if the VIN voltage of the regulator is sufficiently lower than that supply, such that the FETs have enough gate-source voltage).

REFIN

This analog input is used as the reference voltage for OUT2 (the error amplifier compares it to the feedback resistor divider at FB2). This voltage is also fed into a buffer, which is output on the REFOUT pin. Note from the Electrical Specifications Table that there is a common-mode limit for this input; in particular, if an external 5V supply is used for VCC, then the 3.3V from VREF should not be used directly; it should be divided down to avoid running out of headroom.

REFOUT (VTT Buffer)

This analog output provides a buffered version of the REFIN input, to be used by other IC's in the system. In the DDR mode, where VTT is generated from VDDQ, this output can be used as a VTT Buffer.

In addition, it can be used to select the phase relationship, but it disables the buffer in that case (see Table 1). Tying it to VCC (5V) selects 0 degrees phase (in either mode); leaving it open (where it can also be used as a reference output) selects 90 degrees phase (in DDR mode) and 180 degrees phase (in Independent Mode). A capacitor to GND is recommended for stability (see Application Considerations).

VREF

This analog output pin is a 3.3V nominal reference, which can be used by this IC (or others) as a voltage reference. A capacitor to GND is recommended for stability (see Application Considerations).

DRIVE3

This pin drives the gate of an external N-Channel MOSFET, for OUT3, which is a linear regulator.

PGOOD

This digital output is an open-drain pull-down device. When power is first applied to the IC, the output is pulled low, for power “Not Good”. After all 3 soft-start pins complete their ramp up with no faults (no short detected on switchers) the power is considered “Good”, and the output pin is high-impedance (to be pulled up to a logic high level with an external pull-up resistor). See the PGOOD section under Functional Description for more details.

FS/SYNC

This input allows the user to adjust the internal oscillator used for the PWM outputs; a pull-down resistor will speed up the oscillator; use a 0Ω resistor (or a trace) to GND to get the default 300kHz. In addition, a digital clock signal can be fed into this input, in order to SYNC its clock with the external one; this allows the clock edges to line up in a way that won’t interfere with each other.

Functional Description

Overview

There are two single-phase synchronous buck converters, and one linear regulator. Except for a common clock, the two PWM regulators are independent. Refer to Figures 2 and 3 for a quick discussion of the circuit. The right side of the diagram shows the 3 output stages with their components; each switcher has an upper and lower FET, input capacitor, bootstrap diode and capacitor, an LC output filter, and an optional snubber.

The 3rd regulator (OUT3) is a linear, with an external NFET, input and output capacitor. The output voltage is divided to FB3, and compared to an internal 0.6V reference. An RC is used for compensation.

The left side of the diagrams show the various control and programming components. Each switcher has a compensation network for stability that includes the output resistor divider. VREF and REFOUT can be used as reference voltages. There are three SS/EN pins to set the soft-start ramp of each output, and a PGOOD output to signal when they are all done. The FS_SYNC pin allows options for the oscillator frequency. Each of these features will be described in more detail, either in the Functional Description or the Application Considerations.

The first regulator (OUT1) has an internal 0.6V reference. To set the output voltage level, connect a resistor divider between VOUT1 and FB1.

The second regulator (OUT2) requires an external reference connected to REFIN. For DDR memory applications (Figure 2), connect a divide-by-two resistor divider from VOUT1 to ground with the center point connected to REFIN. This causes VOUT2 to track VOUT1 at one-half its value. Connect VOUT2 to FB2 (through the compensation resistor). A buffered copy of REFIN is provided on REFOUT.

For Independent mode operation on OUT2 (Figure 3), a 3.3V reference is provided on VREF which can be used directly (if VCC is high enough), or divided down for REFIN. A resistor divider from VOUT2 to FB2 sets the output voltage.

Operational Modes

Table 1 shows how to select the various modes and phasing between the two switching regulators.

TABLE 1. MODE AND PHASE SELECTION

MODE	EN_SS2	REFOUT	PWM1/2	CH1/2
DDR	VCC	VCC	0 degree	EN1/SS1 enables CH1 and CH2
DDR	VCC	Open	90 degree	“
Independent	SS2 cap	VCC	0 degree	EN1/SS1 for CH1; EN2/SS2 for CH2
Independent	SS2 cap	Open	180 degree	“

DDR mode is chosen by connecting the SS2/EN2 pin to VCC (5V). In this mode, SS1/EN1 is used to enable and soft-start both OUT1 and OUT2 (a single 30µA current source is charging a single soft-start capacitor). In addition, VOUT1 (usually divided by 2) can be used as the REFIN for OUT2. VOUT1 is often used as VIN2 (especially when the VOUT2 current is low enough) although it is not necessary. And OUT2 does allow both sinking and sourcing of current for the DDR.

For Independent mode, SS2/EN2 is not connected to VCC. Instead it is connected to a soft-start capacitor to GND, similar to SS1/EN1. The capacitors will ramp each output independently, and each can be turned off by pulling its SS/EN pin to GND; releasing will start a new soft-start ramp. SS3/EN3 is also independent of the first two. As explained earlier, one capacitor can be shared by more than one SS/EN pin.

To select the Phase shift between Channel 1 and 2, the REFOUT pin is used. Tie it to the VCC pin to get 0 degrees in either mode (which means both switchers are in phase). In this case, the REFOUT pin is not available for use elsewhere; the buffer is disabled. Leave REFOUT open (driven to whatever voltage is supplied at REFIN) and it selects 90 degrees in the DDR mode, or 180 degrees in Independent mode; REFOUT can be used as a reference in this case. The advantage of Phase shift is to keep the switching current spikes from lining up to create even higher noise, or interaction between the channels; it also reduces the RMS current through the input capacitors, allowing fewer caps to be employed. However, depending on the VOUT to VIN ratios of both, there is no guarantee that opposite edges might not line up, depending on the duty cycles; so the user should check for that possibility.

Figure 4 shows the phases. The rising edge of LGATE1 (LG1) and LGATE2 (LG2) is fixed; the phase difference is relative to the rising edges. The falling edge of each is the

variable one (determined by the duty cycle). LG1 is shown with a pulse width shorter than LG2; this is just an arbitrary example, and it does not affect the rising edges.

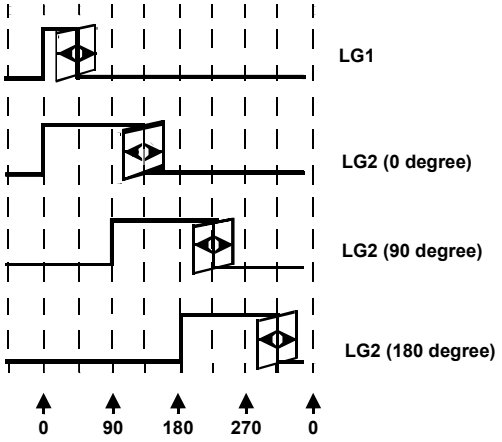


FIGURE 4. PHASE OF LG2 WITH RESPECT TO RISING EDGE OF LG1

Output Regulation

The basic PWM regulator voltage is usually set up as follows: FB and the internal reference are the two inputs to the error amplifier, which are forced to be equal. The output voltage is externally divided down to the FB pin, to equal the reference. In the ISL6534, VOUT1 uses an internal nominal 0.6V reference; VOUT2 uses an external REFIN pin for the reference. There are many variations of the above, especially when the modes (Independent or DDR) are also considered. Below are some of the cases that can be used, along with the advantages or disadvantages of each.

The following figures show the compensation circuit for VOUT1 and VOUT2; they include a full type-3 compensation network. Also shown is the resistor divider for REFIN. Several notes:

1. The labeling of the resistors may not match other diagrams; they should be used just for the equations included.
2. The VREF pin (nominal 3.3V) is assumed here (the VREF pin supplies a soft-start ramp that other external sources may not), but any other appropriate fixed voltage reference can be used as REFIN for OUT2.
3. One percent (or better) resistors are typically used for these resistor dividers; the overall system accuracy depends directly upon them. Exact ratios are not always possible, due to the limited values of standard resistors available; these errors must also be added to the tolerance.

VOUT1 (INDEPENDENT OR DDR MODE)

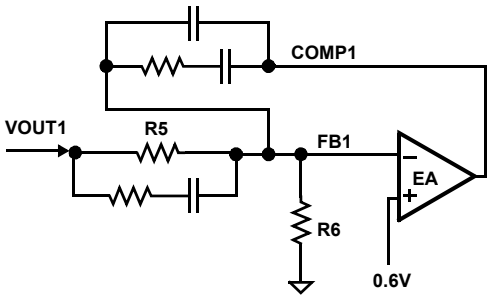


FIGURE 5. RESISTOR DIVIDER FOR VOUT1 (DDR OR INDEPENDENT MODE)

Figure 5 shows the resistors for VOUT1, and the equation below shows that R5 and R6 divide VOUT1 down to match the 0.6V internal reference. VOUT1 must be greater than 0.6V and 2 resistors are needed, and their accuracy directly affect the regulator tolerance.

$$FB1 = VOUT1 \cdot \frac{R6}{R5 + R6}$$

Use the following equation to choose the resistor values. R5 is part of the compensation network, and should be selected to be compatible; 1kΩ is a good starting value. Find FB1 from the Specification Table for the right condition, plug in the desired value for VOUT1, and solve for R6.

$$R6 = \frac{FB1 \cdot R5}{VOUT1 - FB1}$$

VOUT2 (INDEPENDENT MODE)

Figure 6 shows the resistors for VOUT2; it is similar to VOUT1 in that 2 resistors divide down VOUT2 to FB2; the difference is that a second resistor divider may be used to divide an external reference REF (such as VREF pin; see Specification Table for details) or some other voltage (such as VOUT1 for DDR mode).

Use the following equations; first decide what reference will be used (REF), and whether it will be divided down (to REFIN); choose a nominal value for R3 (such as 1kΩ) and solve for R4. Assume a value for R1 (part of the compensation calculation); 1kΩ is good starting value. Now that REFIN is determined, plug it in for FB2, plug in the desired VOUT2, and solve for R4.

$$R4 = \frac{REFIN \cdot R3}{REF - REFIN}$$

$$R2 = \frac{FB2 \cdot R1}{VOUT2 - FB2}$$

The same equations are used for following cases; some of them get simplified by removing one or both dividers.

Case 1 is the most general case (no restriction on VREF > or < VOUT2), and the most flexible. Both VREF and the output are divided down to the same arbitrary reference (in the 0.6V

to 3.3V range for best performance). The advantage is that if either the VREF or desired output voltage changes going forward, the only board change needed is the value of 1 or more resistors. The disadvantage is that since there are two resistor dividers, both of them add to the error budget of the regulator output. The total number of resistors used is 4.

Case 2 can be used when VOUT2 is less than VREF. R3 and R4 divide the reference to match VOUT2. It saves a resistor (R2); R1 (usually ~1kΩ) is still needed as part of the compensation, but it doesn't affect the accuracy of the output. Three resistors are needed; this is the most typical case.

Case 3 can be used only when VOUT2 is greater than VREF, which is brought directly into REFIN; then VOUT2 is divided down to match it. Only two resistors (R1, R2) are needed, and both affect the accuracy.

Case 4 can be used only if VREF = VOUT2; this case is the most accurate (since neither has a divider), and only uses one resistor (R1, as part of the compensation). Make sure REFIN has sufficient headroom to VCC.

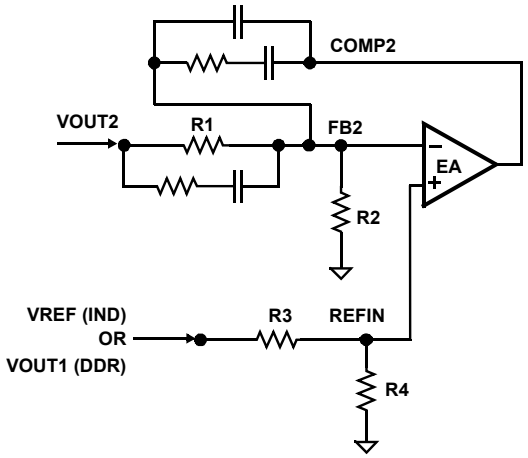


FIGURE 6. RESISTOR DIVIDERS FOR VOUT2 AND REFIN

VOUT2 (DDR MODE)

The main difference for DDR Mode is that rather than using a fixed external reference for REFIN, a reference based on VOUT1 (which is also called VDDQ for DDR) is used instead. See Figure 6. Use the same equations shown for the Independent mode; just substitute VOUT1 for REF.

Case 1 is again the most general case; Both VOUT1 and the VOUT2 output are divided down to the same arbitrary reference (in the 0.6V to 3.3V range for best performance). The trade-offs are the same as Case 1 for Independent mode described earlier.

Case 2 can be used when VOUT2 is less than VOUT1, which is the case for DDR (since VOUT2 = 1/2 VOUT1). It saves a resistor (R2); R1 is still needed as part of the compensation, but it doesn't affect the accuracy of the output. R3 and R4 divide the VOUT1 by 2 to match VOUT2. Three resistors are needed, two of which affect the accuracy. Since the DDR mode almost always uses the divide by two, no flexibility is lost here; just change the VOUT1 resistor divider to change the value of VDDQ, and VOUT2 will still track at 1/2 the value.

Cases 3 and 4 don't apply for DDR.

Soft-Start/Enable

Numerous combinations of independent and dependent start-up are possible by the various methods of connecting the three SS/EN pins; some combinations are shown in Figures 7 and 8. In Figure 7, the three regulators enable independently and rise at rates selected by their individual soft-start capacitors C_{SS1}, C_{SS2}, and C_{SS3}. In Figure 8, two diodes are used to connect to a single open-drain pull-down device (not shown); this allows one FET to disable both channels. When enabled, they will each rise at their own ramp rate. If they could use the same ramp rate, then both pins could share one capacitor and the one FET, and the diodes are not necessary. The 3rd channel is disabled and ramped independently.

Since the EN trip point is around 1V, some care should be taken to guarantee the diode drop and the FET in series with it will always be below it (including manufacturing tolerances, temperature extremes, etc.); schottky diodes, with their lower voltage drop, are preferred. Also, beware of diodes with high reverse leakage, especially at high temperatures. If the pull-down FET also has a pull-up resistor to 12V, for example (not recommended), then the SS/EN pin could be pulled too high, and interfere with normal operation; the voltage on the EN pins should not exceed VCC.

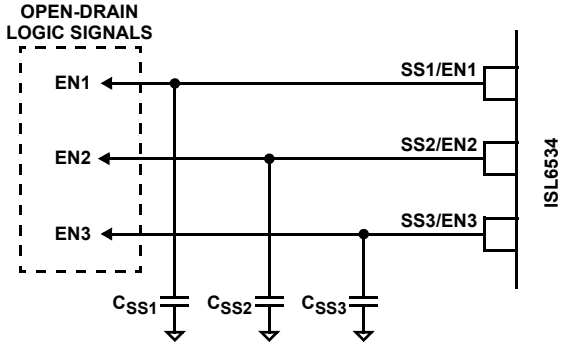


FIGURE 7. CONNECTIONS FOR INDEPENDENT ENABLE AND SOFT-START

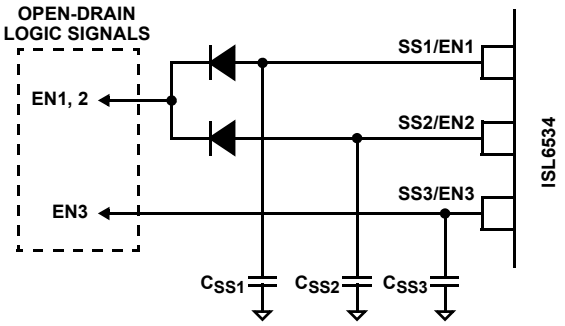


FIGURE 8. 1 AND 2 ENABLED TOGETHER BUT HAVE INDEPENDENT SOFT-STARTS. 3 IS FULLY INDEPENDENT.

The soft-start pins can share the same capacitor, to ramp them all at the same rate (but since there will be 3 times the current, the value of the capacitor needs to be approximately 3 times bigger, for the same ramp rate).

Note that each output rise does not start until its SS/EN voltage reaches ~1V; the output will then start to ramp up until the soft-start is > ~3.3V (ramp is done). PGOOD will not go active unless all three ramps are >3.3V (and no faults are detected).

Figure 9 shows the start-up waveform for VOUT1 at power up. In this example, the VCC voltage is generated from the internal shunt regulator. The ramp of the 12V is controlled by the external power supply; it can vary widely, depending upon the type and model used. The ramp of the shunt more or less follows the VCC12 until it reaches its regulation point at ~5.8V. Both VCC and VCC12 must be past their rising POR trip points before SS1 starts rising. The order doesn't matter, and may be different, especially when the VCC uses an independent supply. In most cases with the shunt regulator, the VCC12 POR is 2nd; when it hits ~8V, the SS1/EN1 ramp begins. When SS1/EN1 reaches ~1V, the output starts ramping up, and the ramp is complete when SS1/EN1 reaches ~3.3V.

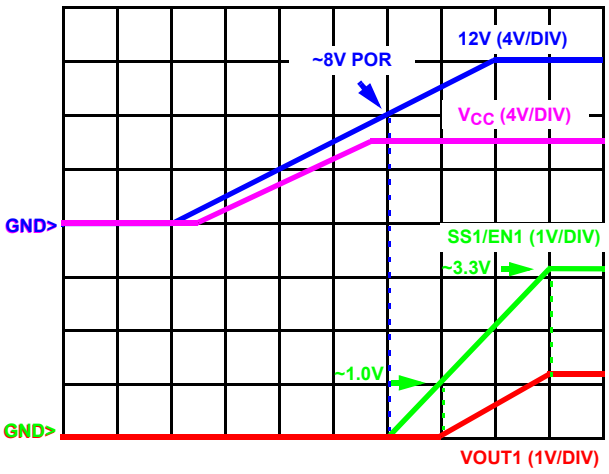


FIGURE 9. START-UP (12V, VCC, SS1/EN1, VOUT1)

Note that if VIN1 is tied to a supply other than either VCC or VCC12, then it MUST be up above the desired output voltage (or at least ramping there ahead of the output) before the SS1/EN1 reaches ~1V. If not, the short-circuit protection will trigger, and shut down all three outputs, requiring a POR on either VCC or VCC12 to restart. If either VCC or VCC12 is used as VIN, then the voltage levels should be sufficient, as long as the design can function at the POR levels, since both must hit their POR levels before starting up. So, for example, if the VCC12 supply was also used as VIN, then as long as the output could start up at VIN = ~8V (the VCC12 rising POR trip point) the start-up condition is satisfied.

PGOOD

The PGOOD open-drain pull-down device is on when power is first applied to the IC, forcing the pin to a logic low, for power "Not Good". After all 3 soft-start pins complete their ramp up with no faults (no short detected on either switcher), the power is considered "Good", and the output pin goes high-impedance (to be pulled up to a logic high level with an external pull-up resistor). Figure 10 shows an example, with a fast SS1 and VOUT1, a slower SS3 and VOUT3, and the PGOOD output. The PGOOD waits for the last of the SS signals (EN3/SS3 here) to reach their ramp-done trip point before it goes high.

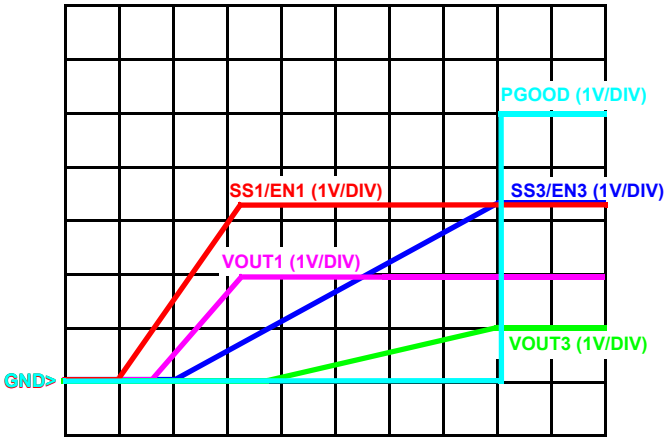


FIGURE 10. PGOOD OUTPUT

If any of the SS/EN pins is held low, PGOOD will not go high; thus, if one of the three outputs is not used, and the PGOOD function is desired, then that SS/EN should be allowed to charge high, and the other pins of the unused regulator should be tied so as not to cause a fault or shutdown. Options for OUT1 include: tying FB1 to COMP1, or tying FB1 to VCC, and leaving COMP1 open. VOUT2 is a little more difficult; Tie REFIN, FB2, COMP2 to GND; or tie FB2 to COMP2, and tie REFIN to a voltage well under 3V (to avoid the short-circuit shutdown). In all of these cases, leave the LGATE and UGATE pins open; tie BOOT pin to VCC12. See section "Linear (VOUT3) Component Selection" for considerations for disabling the linear output, while keeping PGOOD active.

Once the power is “Good”, PGOOD will pull low if any of the 3 SS/EN pins is pulled low. Also, if a short is detected on either switcher, then the PGOOD will pull low, for as long as the condition is there. If VOUT1 or VOUT2 has a short detected which stays there for 1-2 clock pulses, then all three regulators will shut down, and wait for a power-down and up cycle to reset (either VCC or VCC12 (or both) must power down and up). If the short-circuit is not there long enough to shut down, it may still cause PGOOD to go low momentarily. If this causes a system issue, a filter capacitor could be tried; it should be at least several nF to be effective.

Note that this is not a full-feature PGOOD; it is not directly monitoring if the VOUT1 or VOUT2 drops below a set UV level; it only checks for the simple short-circuit condition, via the COMP pins. And it is not monitoring VOUT3 at all. So it is a good indication that all three outputs have ramped up, but it is less useful as a monitor from that point on.

Since PGOOD is an open-drain pull-down device, it usually requires an external pull-up resistor; however, if the pin is not used, no resistor is necessary. A value in the range of 1kΩ to 10kΩ is typical.

POR

Both the VCC (5V) and VCC12 (12V) are monitored for Power-On-Reset, as shown in the Specification Table. The two POR outputs are logically gated together, such that both have to be above their rising trip points to enable the SS/EN ramps to start (if they are not held low) and then enable each output. Either POR output can go below its falling trip point to disable all outputs, and then back to restart the enable operation.

Shunt Regulator

The ISL6534 must have both a 12V (for VCC12) and a 5V power supply (for VCC); both must be above their respective POR rising trip points to enable the outputs to start switching. The shunt regulator (nominal 5.8V) was designed for those systems that do not have a 5V supply available; the range of the shunt (5.6V to 6.0V) was designed not to overlap the usual 4.75V to 5.25V range of typical power supplies. An external resistor between VCC12 and VCC is required; a typical value of 150Ω is the recommended starting value (it may change due to other factors, such as VCC12 voltage, VBS voltages, oscillator frequency, etc.). The dissipation of the resistor is approximately 1/4W; it needs to be sized accordingly. For example, 12V - 5.8V = 6.2V across the 150Ω resistor is 41mA; P = IV = 0.256W. Several low-power resistors in parallel can also be used. See Figure 11.

In either case, both VCC and VCC12 pins have small decoupling capacitors (typically 1.0 to 10.0µF); they should each be located near their pin, with a via to the GND plane.

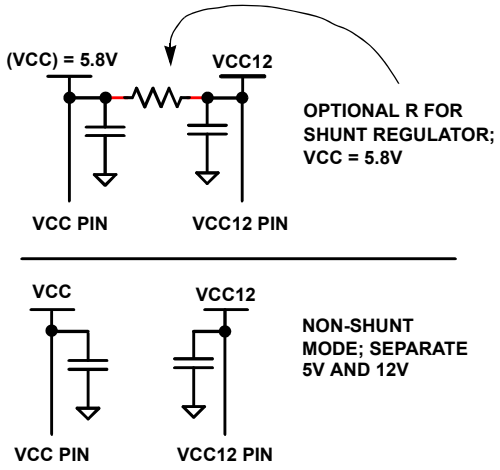


FIGURE 11. SHUNT REGULATOR AND DECOUPLING CAPACITORS FOR VCC AND VCC12 PINS

Short-Circuit Protection

There is no current sensing or $r_{DS(ON)}$ sensing or undervoltage sensing on the ISL6534. However, if either Channel 1 or 2 output is shorted while active, there is a simple detection on the error amp COMP output that implies either overcurrent or undervoltage; the PGOOD pin goes low immediately. If the condition persists for 1-2 internal clock cycles (3-6µs at 300kHz), then ALL 3 Outputs are latched off, requiring either a VCC or VCC12 POR to restart. The protection was not designed to work for the case of powering up an output into a short-circuit, and there are limitations on detecting applied shorts. Note that the linear regulator has no short-circuit protection.

See Application Considerations for more details.

Oscillator

The internal oscillator is nominally 300kHz (±20% tolerance) with no external components required (tie FS_SYNC pin to GND), as measured at either of the LG or UG pins. To run faster, a resistor from FS_SYNC pin to GND will speed up the frequency. See Figure 12 for a curve that shows the frequency versus resistor value. Since the curve is steep as it approaches 300kHz, operation in this area is not recommended if the exact frequency is important.

Since this pin has several functions muxed onto it, it is important that they do not interfere with each other. Thus, the circuit that looks for the resistor will shut off (and default to the 300kHz) if it doesn’t see a current in the expected range. There should not be any excessive capacitive loading on the pin either, and if a resistor is used, it should be located very close to the FS_SYNC pin, and its connection to GND should be near the IC GND, and away from the output stage power GND, to minimize jitter.

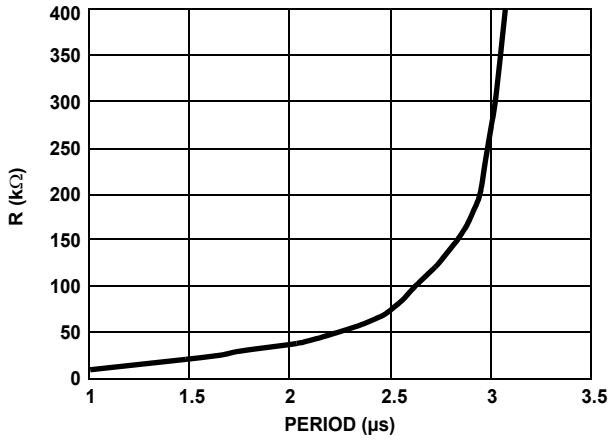


FIGURE 12. TYPICAL CLOCK PERIOD vs FS_SYNC RESISTOR TO GND

SYNC

With multiple switching regulators running on the same board at similar, but independent frequencies, there may be interference between them; a “beat” frequency can develop, based on the difference between the two frequencies. To avoid this situation, the ISL6534 has a synchronization circuit that will read an external frequency, and make the ISL6534 follow it. The typical circuit involves taking the LG (Lower Gate) signal from another regulator, going through a series 10kΩ resistor (to limit the current), and connecting to the FS_SYNC pin (with no other resistors attached). Within a few internal clock cycles, the ISL6534 will lock-in to the new frequency, and run normally as if it were programmed to run there. If the signal is lost for any reason, after a set number of clock cycles, the ISL6534 will go back to its default internal frequency. Note: Do not use the oscillator of another regulator directly, since the ISL6534 will scale it up by 4 to match its own internal oscillator; using the LGATE signal will allow the ISL6534 to match its LGATE to the same frequency. See Figure 13.

Note that the SYNC circuit expects to see a stable frequency, and can be fooled by variations. For example, if the gate signal used has both leading and falling edge modulation, that might cause some confusion. Skipping clock cycles completely may also be misinterpreted as a much longer period. The SYNC circuit was designed to work over a range of 300kHz to 1MHz.

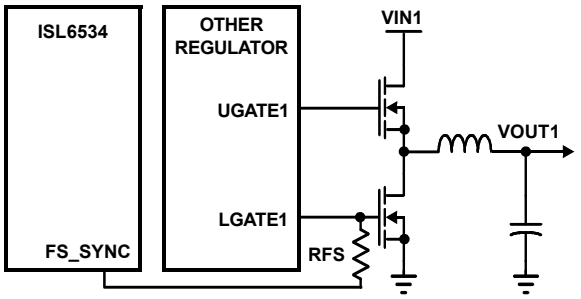


FIGURE 13. CONNECTION OF FS_SYNC TO THE LGATE OF ANOTHER SWITCHING REGULATOR

Application Considerations

Decoupling Capacitors

Both the VCC12 and VCC pins should have a decoupling ceramic capacitor (typical values are 1 - 10µF), located as near to the pin as possible, and with the GND connection as a via to a wide GND plane. A low-value resistor in series with the capacitor may help isolate the switching noise from the power supply from affecting the capacitor, especially if either pin is sharing a power supply with other noisy circuits (adding a resistor in series with the shunt regulator resistor gives no advantage).

SS_EN Capacitors

The basic formula for the soft-start is:

$$t = C \bullet \frac{dV}{I_{SS}}$$

where

t is the soft-start ramp time
C is the external capacitor to GND on the SS pin
dV is the voltage the ramp charges up to (nominal value is 3.3V)
I is the charging current (nominal 30µA).

Or:

time (in ms) = 110 * C (in µF).

Plugging in the known values, and adjusting units, time (in ms) = 110 * C (in µF). So, for example, a 0.1µF capacitor will give a ramp time of 11ms, and a 1.0µF capacitor will give a ramp time of 110ms, which is around the practical maximum value allowed, before noise and leakage and other factors start affecting the formula. Faster ramps are allowed, as long as the input supplies are capable of charging the output capacitors (and possibly the load currents, if present at power-up), without drooping too much (for example, if either the 5V or 12V supply is dragged down below its POR falling trip point, because of output loading, that might indicate that the output ramp is too fast (or perhaps bigger input capacitors are needed, or possibly other explanations as well).

The above formula determines how long the Soft-Start ramp time is. But since the outputs don't turn on until the SS/EN pin reaches ~1V, that means the actual time the output ramps is only ~70% of the total SS ramp. Figure 9 shows an example; SS1/EN1 ramps from 0 and 1V, before the VOUT1 ramp starts; but they both end at the same time. If the SS ramp was 3.3ms long, the output ramp would be about 2.3ms long.

Each of the three regulators can have its own independent ramp rate, as well as their own independent enable function (pulling one of the SS/EN pins below 1V nominal will shut down that output). Two or three pins can be tied together to share a common ramp and enable; but there are now two or three times the current charging a single cap, so the formula should be adjusted accordingly. If you need the same ramp rate, but separate enable functions, then don't share the capacitor; just use the same value capacitor on each, which will still allow independent enabling. If you need different ramp rates, but want to share a single enable signal, you will probably need to connect a separate pull-down FET to each pin, and just drive their gates from a common signal, or use diodes to isolate a single FET to multiple pins (as previously shown in Figures 7 and 8).

VREF/REFOUT Capacitors

The VREF output may require a small capacitor to GND to remain stable; 1.0µF is recommended. If the output is not used (for example, in DDR mode, where if VOUT1 is divided down for REFIN); it could be left open, but the additional noise and current draw may be objectionable. So even then, a capacitor is recommended.

The REFOUT output is similar; a 0.1µF capacitor is recommended.

Linear (VOUT3) Component Selection

Once the VIN3 and VOUT3 levels are defined, the NFET is chosen to handle the output load current and the power dissipation it creates. The power is determined by:

$$\text{Power} = (\text{VIN3} - \text{VOUT3}) \bullet \text{ILOAD}$$

Even if the FET is in a good thermal package (such as a D-PAK), the mounting of the FET will determine how much power dissipation is allowed. If simply placed on a pad on an FR4 board, the dissipation will be limited by the area of the pad; the more area, the lower the temperature will be. The recommendation is to use large plane areas, as well as thermal vias to the back of the board, plus additional area there, if possible. Even then, power dissipation is usually limited to 1W or so, which would give 1A (assuming a 1V drop from VIN3 to VOUT3).

It is not recommended to parallel two FETs in order to get higher current or to spread out the heat; the FETs would need to be well-matched in order to share the current equally without any additional circuitry. In addition, the DRIVE3 pin output was not sized to drive multiple FET gates; it may take longer to charge or discharge the gates during transients. Similar problems will occur if two FETs are placed in series; the currents will be equal, but the voltage across each will not match without additional circuitry. Acceptable solutions include adding a heat sink or airflow, finding or creating an input voltage closer to the output voltage, reducing the load current (or raising the output voltage), adding a 2nd complete linear output (and splitting the load between the two) or replacing the linear with a switcher.

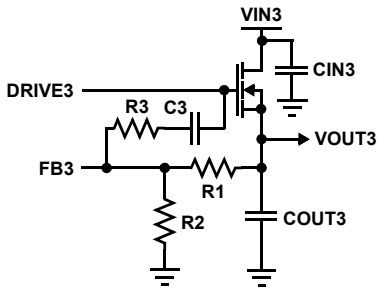


FIGURE 14. LINEAR (VOUT3) REGULATOR COMPONENT SELECTION

The output capacitor C_{OUT3} should be chosen for output filtering and transient response needs. However, the output capacitor also affects the stability of the regulator, so the choice is limited to a range of acceptable values, which include the capacitance and its ESR (Effective Series Resistance). See Figure 14.

The input capacitance C_{IN3} is chosen to keep the input supply from changing too much when the output current load changes; this is related to transient response.

The resistor ratio is chosen to divide the desired output voltage down to make the FB3 pin = 0.6V. First choose R1; 1kΩ is a good typical value. In the equation below, plug in the value of FB3 from the Specification Table, and the desired VOUT3 value, and solve for R2.

$$R2 = \frac{FB3 \cdot R1}{VOUT3 - FB3}$$

Compensation components R3 and C3 are chosen to make the output stable under the conditions being used. Choose the values to add a zero around 30kHz to cancel a pole. Values of 4.75K and 6800pF are a good starting point.

If the Linear output is not used, then tie DRIVE3 to FB3 to terminate them; no other components are needed. There are then several options for SS/EN3. If PGOOD is not being used, SS/EN3 can be tied to GND to disable the linear (and PGOOD). If you need PGOOD to be active for the switchers VOUT1 and VOUT2, then SS/EN3 can be left open for a very fast ramp, or it can be tied to tied to SS/EN1 or SS/EN2 (but remember that SS/EN3 adds charging current, so make the cap bigger). It is not recommended to tie SS/EN3 to VCC.

A possible side benefit of tying off the linear is gaining additional control over the PGOOD timing. Using one of the above methods, the PGOOD will become active after the 2nd switcher ramps up. But if you want to add a delay after that, one way to do it is to add a cap on SS/EN3, and make the ramp longer than the other two; then PGOOD would not become active until the longest one finishes, effectively creating a delay (from when SS/EN3 starts). Another option is to externally hold down SS/EN3, and then release it after a fixed delay, with or without an additional ramp delay. Externally switching SS/EN3 to GND can also make PGOOD go inactive, without having to shut down VOUT1 or VOUT2.

The maximum VOUT3 voltage allowed is determined by several factors: the power dissipation, as described earlier; the input voltage available, the DRIVE3 voltage, and the FET chosen. The voltage can't be any higher than the input voltage available; let's assume we use 12V. The DRIVE3 voltage is driven from the VCC12 rail; allowing for headroom, the typical maximum voltage is 9V (lower as VCC12 goes to its minimum). So the maximum output voltage will be a V_{GS} drop below the 9V (which includes the FET threshold voltage), at the maximum load current, as determined by the FET characteristics. So a practical value around 7-8V is possible.

This is a low drop-out linear regulator. For any input voltage below the maximum above, where the DRIVE3 voltage is not limited by the FET threshold voltage, the drop-out is determined mainly by the FET V_{DS} voltage drop. In other words, the maximum voltage drop across the FET at the maximum load current is what determines the Vin - Vout difference. This can be less than 0.1V for big FETs or relatively low max current ratings.

Connecting One Input from Another Output

Often, one of the 3 outputs generated is used as the input voltage to a 2nd (and perhaps 3rd); the general case includes inputs or outputs of other IC regulators as well. This can be done, with a few precautions in mind.

1. The first output must be designed and sized for its own load current, plus the expected input current of the other channels.
2. The sequencing of the outputs must be consistent. The first output cannot be disabled or have a much slower SS/EN ramp than the input channel, in order to take full advantage of the soft-start. If the VIN is not present when the 2nd regulator tries to start up, that can be interpreted as a short-circuit, and the whole IC could be shut down.
3. The output capacitor of the first is now also the input capacitor of the 2nd, so it needs to be chosen and sized for both conditions. For example, transients on the first output show up on the input of the 2nd; and input current transients on the 2nd can affect the output of the first. There may also be trade-offs of the placement of the various capacitors; some might be near the output FETs of the first, and some near the input FETs of the 2nd.
4. The linear regulator has no short-circuit protection. However, if VIN3 is connected to one of the switcher outputs, a short on the linear output may be detected; but it is subject to all the cautions mentioned in the SHORT-CIRCUIT PROTECTION section.

Feedback Compensation

The compensation required for VOUT1 and VOUT2 is similar to many other switching regulators, and the same tools can be used to determine their component values. VOUT1 and VOUT2 are similar with respect to the compensation; the only difference is their reference voltages (fixed ~0.6V versus REFIN, which does not directly affect the component values). The schematics show type-3 compensation, which is recommended for the general case; the simpler type-2 compensation is a subset. A simple rule of thumb is that when bulk capacitors are used on the outputs, the ESR is often high enough (10's - 100mΩ) to use type-2 compensation. But if only ceramic capacitors (ESR ~ 1's mΩ) or other low-ESR capacitors are used on the outputs, then most likely type-3 will be required. The reference designators in these figures match the equations given in this section, but may not match other figures in this data sheet. Each switcher output should be calculated separately.

CAUTIONS:

1. If two (or more) different kinds of output capacitors are used, their effective ESR and capacitor values cannot be easily combined into one for modeling. This can lead to stability problems, and in some cases can also cause unwanted shutdowns during start-up. But the use of different capacitor types for output filters is generally considered a good practice and can improve performance; the key is modeling them accurately.
2. There is a restriction on the size of capacitor C2 (see Figure 15; this is the single capacitor from COMP to FB); it is recommended that the capacitor C2 be kept to less than 500 pF. During start-up, with low voltages and limited slew rate, the smaller value will allow for adequate drive current capability. Some designs can and do work with higher values; there are other factors that can affect the performance; this recommendation just minimizes the chances of a start-up problem.
3. If the compensation is not properly matched with the rest of the circuit, it is possible that noise coupled from the output can affect the COMP pin, such that it can exceed the voltage and time levels for tripping the output short-circuit protection. For example, type-3 compensation has high bandwidth, and may not be right for some designs. Choose the appropriate bandwidth and gain to meet the design goals.
4. Check with your local Intersil Field Applications for help in choosing compensation values for these special cases; improved tools are available to help calculate values and predict acceptable performance.

Feedback Compensation Equations

This section highlights the design consideration for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 15).

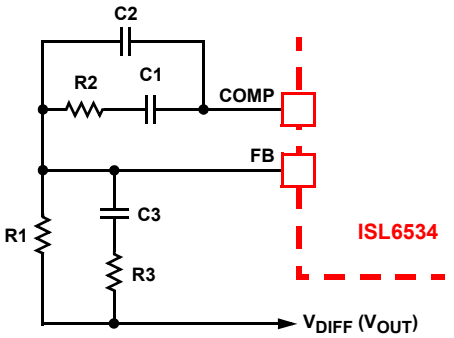


FIGURE 15. COMPENSATION CONFIGURATION FOR ISL6534 CIRCUIT

Figure 16 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable to the ISL6534 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

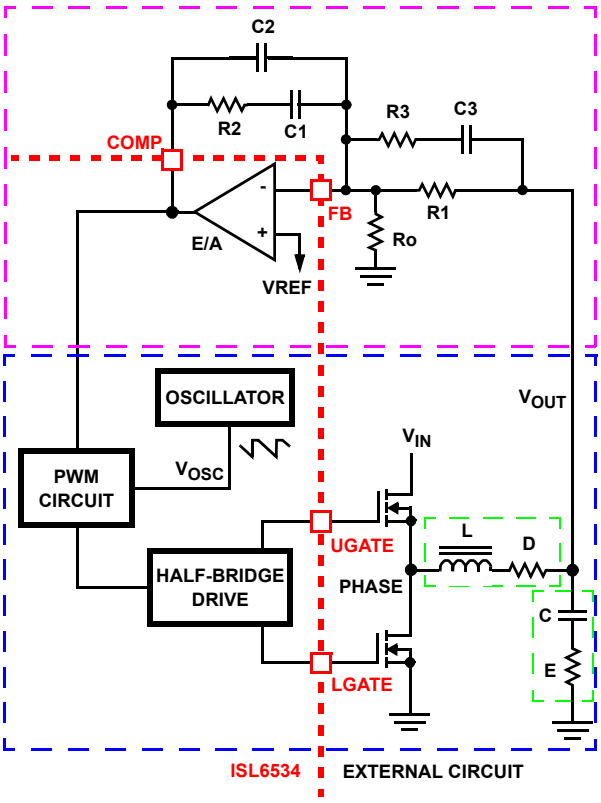


FIGURE 16. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the channel inductance and its DCR, while C and E represents the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot E}$$

The compensation network consists of the error amplifier (internal to the ISL6534) and the external R1-R3, C1-C3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45degrees). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 15. Use the following guidelines for locating the poles and zeros of the compensation network:

5. Select a value for R1 (1kΩ to 5kΩ, typically). Calculate value for R2 for desired converter bandwidth (F_0). If setting the output voltage via an offset resistor connected to the FB pin, Ro in Figure 16, the design procedure can be followed as presented.

$$R2 = \frac{V_{OSC} \cdot R1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}}$$

6. Calculate C1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C1 = \frac{1}{2\pi \cdot R2 \cdot 0.5 \cdot F_{LC}}$$

7. Calculate C2 such that F_{P1} is placed at F_{CE}.

$$C2 = \frac{C1}{2\pi \cdot R2 \cdot C1 \cdot F_{CE} - 1}$$

8. Calculate R3 such that F_{Z2} is placed at F_{LC}. Calculate C3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R3 = \frac{R1}{\frac{F_{SW}}{F_{LC}} - 1} \qquad C3 = \frac{1}{2\pi \cdot R3 \cdot 0.7 \cdot F_{SW}}$$

It is recommended a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. The following equations describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot E \cdot C}{1 + s(f) \cdot (E + D) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R2 \cdot C1}{s(f) \cdot R1 \cdot (C1 + C2)} \cdot \frac{1 + s(f) \cdot (R1 + R3) \cdot C3}{(1 + s(f) \cdot R3 \cdot C3) \cdot \left(1 + s(f) \cdot R2 \cdot \left(\frac{C1 \cdot C2}{C1 + C2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R2 \cdot C1} \qquad F_{P1} = \frac{1}{2\pi \cdot R2 \cdot \frac{C1 \cdot C2}{C1 + C2}}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R1 + R3) \cdot C3} \qquad F_{P2} = \frac{1}{2\pi \cdot R3 \cdot C3}$$

Figure 17 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 17 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

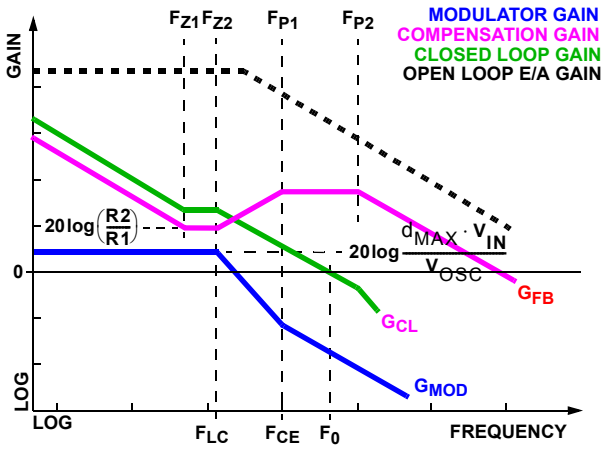


FIGURE 17. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the switching frequency, F_{SW}.

FET Selection (VOUT1, VOUT2)

The typical FET expected to be used will have a low $r_{DS(ON)}$ (5-10mΩ) and a low V_{GS} (Gate-to-source threshold voltage; 1-2V). It can be packaged in a thermally enhanced SO-8 IC package (where the drain leads are thermally connected to the leadframe under the die, or similar approaches), or even in more conventional power packages (D-PAK). If the FETs are surface mounted to the PCB, with only the area of the power planes to conduct the heat away, then the maximum load current will be limited by the thermal ratings under those conditions. Using conventional heatsinks or sufficient airflow can extend the limit of dissipation.

FETs can be paralleled for higher currents; this spreads the heat between the FETs, which helps keep the temperature lower. However, the gate driver is now driving twice the gate capacitance, so there will be more dissipation in the ISL6534 gate drivers. It is recommended that parallel FETs be the same part number; even though they may not match exactly, it is more likely than using two different parts. In particular, the $r_{DS(ON)}$ of each helps determine the relative current sharing; the gate threshold and the internal gate resistance helps determine the turn on and off characteristics.

Typical values for maximum current (based on 8-pin SOIC FETs surface-mounted on PCB, with no heatsinks or airflow) are 5A for a dual FET; 10A for single FETs for upper and lower; and 20A for two FETs in parallel for both upper and lower. These are just rough numbers; many factors affect it, such as PCB board area available for heatsinking planes, how close other dissipative devices are, etc.

In general (and especially for short UGATE duty cycles, such as converting 12V input down to 1V or 2V outputs), the upper FET should be chosen to minimize the Gate charge, since switching losses dominate. Since the lower FET is on most of the time, low $r_{DS(ON)}$ should be the main consideration for it.

Note that the LGATE driver is sourced from the VCC12 input; it is not necessary to use a very low threshold lower FET device; for example, the difference in $r_{DS(ON)}$ between a 1V and 2V threshold, with a 12V gate voltage is very small; the curve for $r_{DS(ON)}$ versus V_{GS} is already flattening out around 10V. And, in fact, a too-low threshold voltage can cause a transition problem. As LGATE goes to GND to turn off, (and UGATE starts to turn on), it only takes a couple of volts of noise or ringing or coupling in the LGATE to turn it

back on momentarily, causing large shoot-through currents, and hurting efficiency.

For extreme cases (such as high current (>20A using parallel lower FETs) and low threshold (~1V)), one possible solution is to capacitive-couple the LGATE; Figure 18 shows one implementation. The zener reverse drop on the left (~3V) and the forward drop of the zener on the right level shifts the LGATE down about to about -4V when off, which keeps Q2 off better; the downsides are the extra components, and the lowered LGATE high voltage (shifted from 12V down to ~8V).

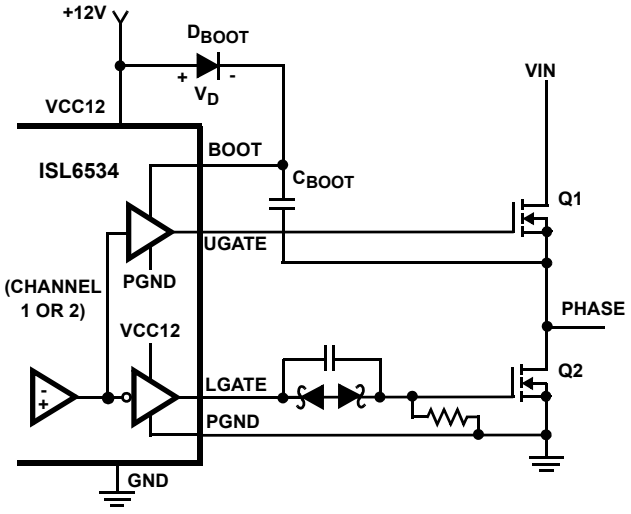


FIGURE 18. CAPACITIVE-COUPLED LGATE

The ISL6534 requires 2 N-Channel power MOSFETs for each switcher output. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements. The following are some additional guidelines.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the upper MOSFET has switching losses, since the FET body diode (or optional external Schottky rectifier) clamps the switching node before the synchronous rectifier turns on.

$$P_{UPPER} = I_O^2 \times r_{DS(ON)} \times D + \frac{1}{2} Io \times V_{IN} \times t_{SW} \times Fs$$

$$P_{LOWER} = I_O^2 \times r_{DS(ON)} \times (1 - D)$$

Where: D is the duty cycle = V_O/V_{IN},
t_{SW} is the switching interval, and
Fs is the switching frequency.

These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFETs body diode. The gate-charge losses are dissipated by the ISL6534 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

Standard-gate MOSFETs (typically 30V breakdown and 20V maximum gate voltage) are normally recommended for use with the ISL6534, especially since 12V is expected to be available to drive the gates. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFETs absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 19 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from VCC12. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the PHASE node. This supply is refreshed each cycle to a voltage of VCC12 less the boot diode drop (V_D) when the lower MOSFET, Q2 turns on. A logic-level MOSFET can only be used for Q1 if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to VIN = VCC12. A a lower voltage supply (such as 5V) can also be used for bootstrapping, which would allow for a lower gate voltage rating; but only if the lower voltage is still high enough to turn the upper FET on hard enough. For Q2, a logic-level MOSFET can be used if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to VCC12; but very low thresholds can cause problems.

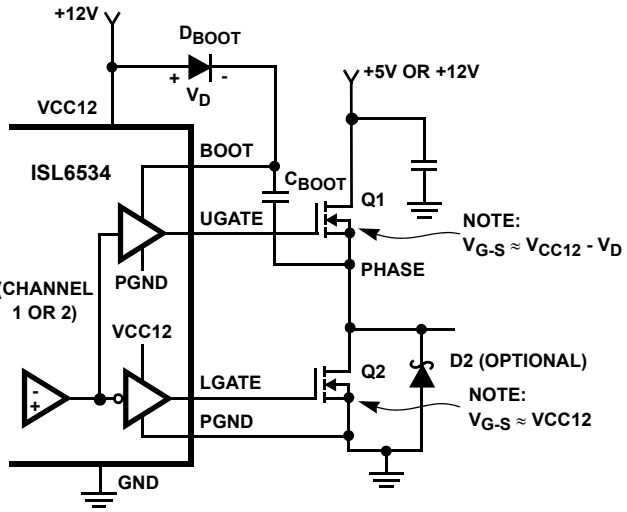


FIGURE 19. UPPER GATE DRIVE - BOOTSTRAP OPTION

Figure 20 shows the upper gate drive supplied by a direct connection to VCC12. This option should only be used in converter systems where the main input voltage is +5 VDC or less. The peak upper gate-to-source voltage is approximately VCC12 less the input supply. For +5V main power and +12 VDC for the VIN bias, the gate-to-source voltage of Q1 is 7V. A logic-level MOSFET may be a good choice for Q1 (again, check the max gate voltage ratings) and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to VCC12.

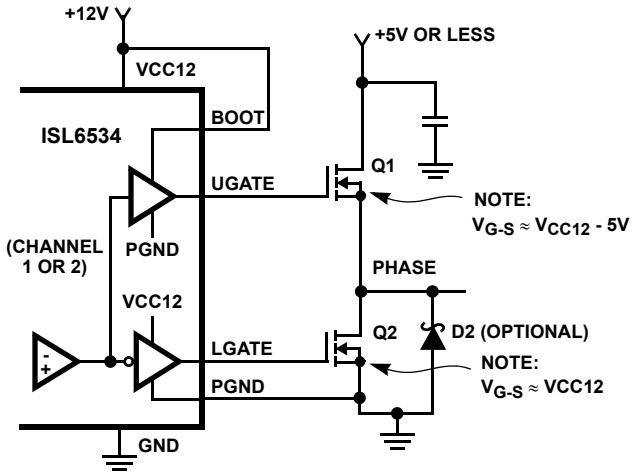


FIGURE 20. UPPER GATE DRIVE - DIRECT VCC12 DRIVE OPTION

Bootstrap Trade-offs

Bootstrapping to 12V requires that the upper FET have a maximum gate-source rating of greater than 12V. Since the LGATE output is sourced from the VCC12 supply in all cases, the lower FET must also have the high rating. So this may rule out using some 20V breakdown FETs that have gate ratings of 12V or less.

Figure 19 shows the diode D_{BOOT} and bootstrap capacitor C_{BOOT}. A small capacitor (~1µF; not shown) is sometimes used as a local decoupling cap to GND; it should be placed near the anode of the diode to GND.

The anode of the diode is shown tied to VCC12, but it can also connect to VCC (even in the shunt regulator mode in some cases) or to VIN or to another appropriate supply. If the shunt voltage is used for bootstrapping, it does increase the current used in the shunt; check that the shunt voltage is not affected; if it is, a lower value of shunt resistor may be necessary.

Figure 20 shows the direct hookup; the advantage is that two components (D_{BOOT} and C_{BOOT}) are not needed; a possible disadvantage is that the VCC12 may not be the optimum voltage for efficiency (perhaps a bootstrap diode/capacitor to 5V would be better, for example).

The PHASE node is not brought into the ISL6534, so there is no way to reference the gate voltage to it, as is often done in other regulators. The considerations for the BOOT2 pin are identical to BOOT1; but since they may have different VIN, VOUT, FETs, etc., the preferred solution for each output may be different for any given system.

The voltage required on V_{BOOT} (Bootstrap Voltage; the diode anode) depends primarily on the upper NFET $r_{DS(ON)}$ and V_{th}. A high voltage makes the $r_{DS(ON)}$ as low as possible, which should help the overall efficiency; however, the high voltage makes the switching power in the gate driver higher, which lowers the efficiency. So the net overall effect is a trade-off between the two. At the other extreme, a low voltage must be at least as high as the FET threshold voltage, plus a few volts of overdrive, in order to turn on the NFET hard enough to source the maximum load current. So the $r_{DS(ON)}$ is not as low, hurting the efficiency, but the gate driver power is lower, which helps the efficiency.

Since the gate driver power is a function of (voltage)^2, the theoretical optimum V_{BOOT} voltage is to make it only high enough to turn on the NFET to handle the maximum load. However, since there are usually only a few available power supplies to choose from, the user often must compromise. And sometimes the only supply available is the same one used for VIN, which may be good for one term, but not as good for the other.

The size of the bootstrap capacitor can be chosen by using the following equations:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V} \quad \text{and} \quad Q_{GATE} = \frac{N \bullet Q_G \bullet VIN}{V_{GS}}$$

where

N is the number of upper FETs

Q_G is the total gate charge per upper FET

VIN is the input voltage

V_{GS} is the gate-source voltage (usually VIN - diode drop)

ΔV is the change in boot voltage before and immediately after the transfer of charge; typically 0.7V to 1.0V

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V} = \frac{N \bullet Q_G \bullet VIN}{V_{GS} \bullet \Delta V} = \frac{1 \bullet 33 \bullet 12}{11 \bullet 0.7} = 0.051\mu F$$

The last equation plugs in some typical values: N = 1; Q_G is 33nC, VIN is 12V, V_{GS} is 11V, ΔV_{max} = 1V. In this example, $C_{BOOT} \geq 0.051\mu F$. This value is often rounded up to 0.1µF as a starting value. The bootstrap capacitors usually need to be rated at 16V, to handle the typical 12V boot.

In general, as the number of FETs or the size of the FETs increases (which usually makes Q_G larger) or if VIN or the bootstrap supply (if not VIN) increases (for example, from 5V to 12V), these all require that C_{BOOT} become larger.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \bullet \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient (and usually increases the DCR of the inductor, which decreases the efficiency). Increasing the switching frequency (Fs) for a given inductor also reduces the ripple current and voltage.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6534 will provide either 0% or 87.5% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the output voltage setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. And keep in mind that not all applications have the same requirements; some may need many ceramic capacitors in parallel; others may need only one.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For both through-hole and surface-mount design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

Snubbers

A snubber network is a series resistor and capacitor, usually from the phase node to GND (across the lower FET); it is used to dampen the ringing of the phase node, which can introduce noise into other parts of the circuit. In particular, jitter on the gate drivers can be caused by disturbances that trigger the programmable duty cycle edge of the internal ramp generator. If noise or ringing is a problem in your particular circuit, consider adding a snubber. Typical values are 2.2nF for the capacitor, and 2.2Ω for the resistor. Since the resistor may have large currents, use a 1/2W type resistor. The order of R and C doesn't usually matter, but one preference is putting the resistor to GND, such that the voltage across it can be easily measured on an oscilloscope to represent the current. See Figure 21.

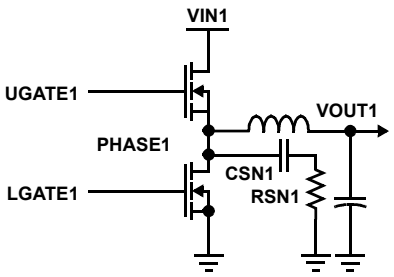


FIGURE 21. SNUBBER COMPONENT SELECTION

Optional Schottky Selection

An optional rectifier D2 (see Figure 19 or 20) is a clamp that catches the negative inductor swing during the dead time between turning off the lower MOSFET and turning on the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. If used, connect the cathode to the phase node, and the anode to PGND. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency will drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

Margining and "Fine-Tuning"

Margining can be added externally to a voltage regulator, in order to raise and/or lower the output voltage a nominal amount, such as ±10%. The purpose might be to run the processor at higher voltage for faster clock speeds, or to run at lower voltages, to save power, for example.

A straightforward method involves adding two extra resistors and two small FETs (and re-adjusting R2, depending upon the decoding used); see Figure 22. Both resistors (RM1, RM2) are high values (10-100kΩ) compared to R1 and R2 (~1kΩ). So when placed in parallel with R2, it lowers the resistance of R2; pick the values for the desired amount. Some simple logic is needed on the gates A and B to control them; pull-up or pull-down resistors might also be needed. Only 3 of the 4 possible states are shown decoded. There are other variations of this technique, but this shows the basic principle. Since the FB are sensitive nodes, care should be taken in the layout, to keep the extra resistors (and the FETs to GND) near the pin.

A variation of this technique can be used without the margining to fine tune the output voltage, when two 1% resistors (R1, R2) can't give the exact value desired. Simply use a much higher value resistor in parallel with either R1 or R2 (or both) to fine-tune the value; a 100-1 ratio in resistor values will be able to change the voltage by roughly 1%; that might be good enough.

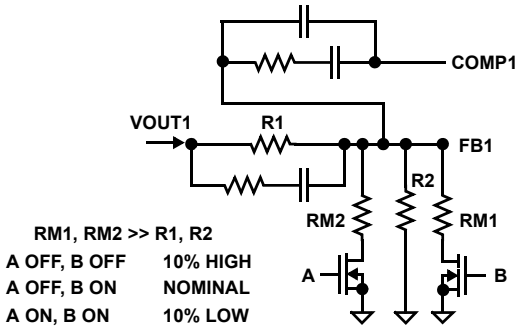


FIGURE 22. MARGINING COMPONENT SELECTION

Short-Circuit Protection

The ISL6534 does not have the typical overcurrent protection used by many of the Core Processor IC's. Instead, it has a simple and inexpensive method of protection. But it is important for the user to understand the method used, and the limitations of that method.

There are no sense pins available on the ISL6534. This means that the many standard ways of sensing output current (sense resistors, FET $r_{DS(ON)}$, Inductor DCR, etc.) are not possible, without adding a lot of external components. There are also no PHASE pins available. Monitoring undervoltage (by sensing drops on the FB pins, or on the outputs) was not done.

The only method of protection for the two switching regulators is to monitor the COMP1 and COMP2 pins for overvoltage. What happens on a short-to-GND on the output? As the output voltage is dragged down, the FB pin should start to follow, since it is usually just a resistor divider from the output. The loop detects that the FB pin is lower than the Error-Amp reference, and the COMP voltage will rise to try to equalize them; that will increase the duty-cycle of the upper FET gate driver (which allows more time to pull the output voltage higher). If the short is hard enough, the COMP pin will rise higher and the duty cycle will increase further. If the short is still too hard, at some point the COMP pin output will go out of range, the duty cycle will hit the maximum, and the loop can no longer effectively try any harder. This is the point at which an overcurrent condition is

detected. A comparator monitors the COMP pins, and if either one exceeds the trip point (nominal 3.3V), and stays above it for a filter time (1-2 clock pulses of the internal oscillator; 3-6µs at the nominal 300kHz; 2-4µs at 500kHz), then it will shut down both switchers, as well as the linear regulator, and require a POR on either (or both) of the VCC12 or VCC power pins. There is no “hiccup” or retry mode, where it keeps trying. The protection was not designed to work while powering up into a short circuit.

So that is the detection method; what are the implications of it? On the plus side, it’s built in, and the user doesn’t have to set anything to use it; no additional components are required. On the negative side, it is not easy to predict its performance, since many factors can affect how well it works. It was designed to detect a “hard” short; like a screwdriver shorting the output to GND. But defining how close to “zero ohms” the short has to be in order to work properly is not straightforward. If the resistance is too high to trip the detector, the regulator will react simply as if the load has increased, and will continue to try to regulate up until the FETs overheat. If the COMP pin doesn’t immediately rise to its trip point when the short is applied, chances are it won’t trip later as the FETs heat up. So most of the potential problems can occur if the initial trip is missed.

Following are a list of the many possible factors that affect the performance:

1. If the power supply used for the VIN of one of the regulators is shared with the VCC12 (or VCC) supply of the IC, then shorting the output could potentially momentarily drag down the supply low enough to trip the VCC12 (or VCC) falling POR, which could result in unpredictable behavior once the outputs shut off due to the POR, and then try to start up into the short after the supply recovers. This scenario can be avoided with a “stiff” power supply, or a separate one.
2. If the power supply for VIN has a built-in current shutdown or limit, then it might shut-down before the IC, or the limiting might help the IC shutdown, either of which is generally good. However, many supplies used in real systems don’t have this built in, or would require a much higher current short than this scenario would provide.
3. If the circuit survives the initial short but doesn’t shut down, the removal of the short can cause an inductive kick on the phase node, which can create an overvoltage condition on the boot pin, which can in the worst case damage the IC and/or the FETs.
4. The resistance of the short itself is probably the most critical factor affecting the overcurrent shutdown performance. If the short is not low enough resistance, then the part will NOT shutdown, and the FETs can overheat. Note that the “short” to the output also includes wiring, PCB traces, contact resistances, as well as all of the return paths.
5. The higher the output voltage, the more current you will get out of a fixed-resistance short, and the more likely you will get a clean shutdown; see also #6. In addition, the higher VOUT for a given VIN will give a higher UGATE duty cycle, and the average COMP voltage is higher, so it doesn’t have as far to go to trip.
6. In general, the faster the rise time of the output current during the short, the more current will be allowed on the initial peak, and the better chance the COMP pin will have a sharp rise as well. A low resistance short (#4) and a higher output voltage (#5) both help. However, if the current ramps too fast, then a false trip is also possible (shutting down at a current level still within the expected load range).
7. The load current at the time of the short can affect the results; the response of a short can be different at no load versus full load.
8. The compensation components are chosen to stabilize the regulation loop; however, if they unnecessarily load the COMP output, that could affect the trip point response.
9. The output capacitance and its ESR can affect how quickly the current ramps up during a short.
10. Other variables that may contribute to a lesser degree include variations in the COMP comparator and filter, the inductor L and DCR, the $r_{DS(ON)}$ of the FET, the FB resistor dividers, the error amp reference voltage, the oscillator frequency, switching noise, VCC voltage, ambient temperature and airflow, and the layout of the PCB.
11. Adding external circuitry to sense a fault may be possible, but subject to the usual limitations of those circuits. For example, sensing the output or FB voltage doesn’t always directly correlate with output current.

So the recommendations are as follows:

1. If there is a specific fault condition that needs protection, try it out first under controlled conditions, either on an EVAL board, the final circuit, or something close to it, along with the power supply that will also be used. Monitor VCC12 and VCC (to be sure they aren’t tripping POR), the output and the COMP pin. A current probe monitoring the output current is also very useful.
2. Compare the short circuit resistance to the nominal load resistance; if they are too close, the circuit may not work well. Calculate how long the FETs can sit at the higher current. Is the short more likely from zero load or full load?
3. Check the rise time of the short circuit current, and what happens if when the short is released.
4. From the waveform of the COMP pin, see if the values can be optimized for the short condition. Within the constraints of the stability criteria, smaller caps (in general) may give a quicker response.

PCB Layout Considerations

General Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

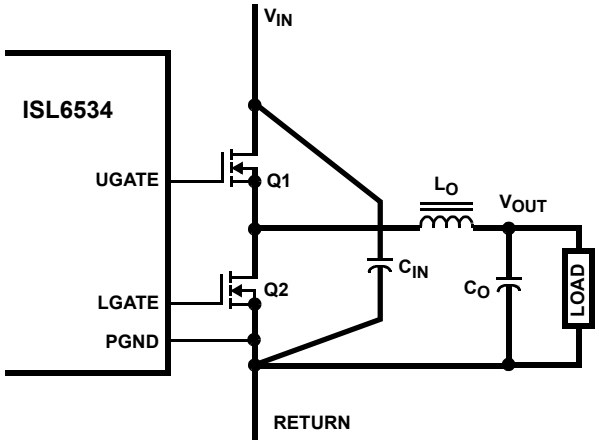


FIGURE 23. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 23 shows the critical power components of the converter, for either output channel. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 23 should be located as close together as possible. The capacitors C_{IN} and C_O can each represent numerous physical capacitors. Locate the ISL6534 within 1 inch (or even less, if possible) of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the ISL6534 must be sized to handle up to 1.5A peak current.

Figure 24 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Note that the "quiet" analog-type signals (including VCC, SS/EN, FS/SYNC shown, as well as others, such as VREF, REFOUT, and all three of the FB resistor dividers) share a local "quiet" GND. VCC12 decoupling cap can also share the same GND; on the QFN package, a separate cap for each VCC12 and PGND pin pair can help isolate some switching noise between the channels, if placed properly (short traces to both pins, before tying the GNDs into the common GND plane). On the output side, the lower FET source and C_{IN} cap should share a short connection; same with the upper FET drain, and the C_{IN} cap. The output load and C_{OUT} share another local connection; these output GNDs are considered "noisy", due to the high current switching; they should be kept away from the "quiet" GNDs near the IC. Finally, all of these GNDs tie into one common GND plane.

Minimize any leakage current paths on each of the SS pins and locate the capacitors, C_{SS} close to the SS pin because the internal current source is only 30µA. Provide local V_{CC12} decoupling between VCC12 and PGND pins, as well as the VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT pin and PHASE node (but since PHASE is one of the noisiest signals, otherwise keep it away from the IC area). The PGND pins are used only for the gate drivers and other output circuitry (including the VCC12 decoupling capacitor); the GND pins are used by the VCC pin, and the control circuitry. They should be joined at a common point; the metal pad under the IC is a good location.

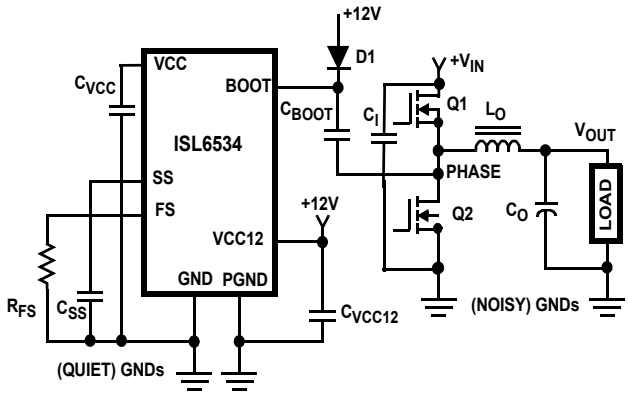


FIGURE 24. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Layout Considerations for the ISL6534

The metal plate on the bottom of either the TSSOP or QFN (MLFP) package must be soldered down to the PC board, and sufficient plane area given for heat transfer. It is recommended that the plane be connected to GND (pin 15 in TSSOP) and PGND (pin 18 in TSSOP), but if it is left floating, it should NOT be tied to any other potential. Thermal vias (at least 4) are recommended to connect to a plane on the opposite side of the PCB (which can also be used as a quiet GND for many of the IC components), and to the internal GND plane, for additional heat transfer. See Tech Brief TB379 for more details.

Decoupling capacitors should be very close to the VCC12 (to PGND) and VCC5 (to GND) pins, with vias (if needed) to the quiet GND plane. PGND and GND should be joined at the metal plate.

The traces from the gate drivers to the FETs (UG1, UG2, LG1, LG2, DRIVE3) should be short (for low resistance) and wide (to handle large currents); the pin spacing will limit the widths right near the package. But the closer the FETs are to

the IC, the more they will heat each other, so keep that thermal consideration in mind.

BOOT1/2 capacitors should be near their pins; the bottom to phase and diode can be a little further away. If a separate small capacitor is used for the bootstrap supply (if different than either VIN or VCC12), it should be located next to the bootstrap diode anode.

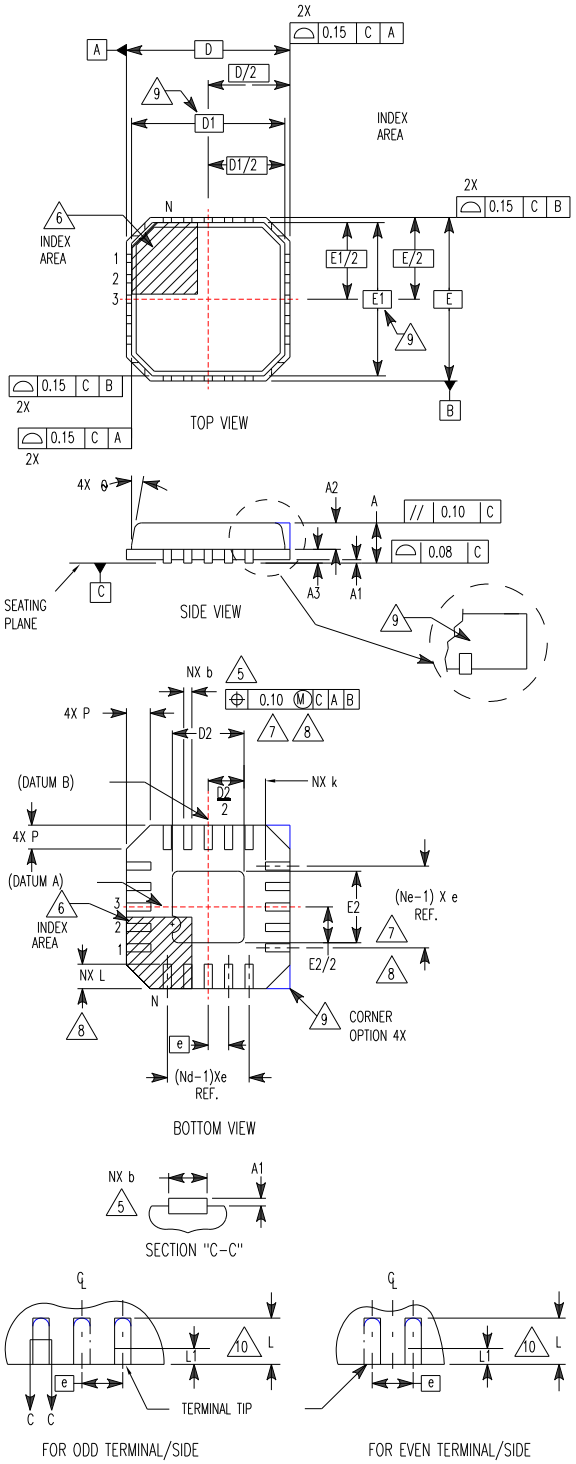
Other traces to keep short include:

- FB1/2/3: the resistor dividers should be near the IC; via (if needed) to quiet GND plane; the signal from the VOUT can travel, since it is low impedance. The VOUT should be taken as close as possible to the load for best regulation, and the trace to the feedback resistor divider should be isolated from any load current.
- Resistor dividers used for references (from VREF or VOUT or to REFIN) should be near the REFIN input; the bottom resistor tied to quiet GND.
- COMP1/2: **ALL** of the compensation components should be close to these pins (as well as FB1/2 pins), with vias (if needed) to the quiet GND plane. The FB divider should **NOT** be near the output, with FB routed back to the IC; the FB trace can act as an antenna and pick up noise that will adversely affect performance. Route the VOUT signal instead, and connect it to the components near the IC.
- SS/EN capacitors should be near pin, with vias (if needed) to quiet GND plane.
- FS_SYNC resistor (if needed) should be near pin, with a via (if needed) to quiet GND. Do not leave the pin open; connect to GND (through a zero ohm resistor or a short trace) for default 300 kHz operation. The GND connection (for either the resistor or default) should be kept away from the Power GND of the output FETs; this is especially important because the FS_SYNC pin location is near the channel 2 switcher. Noise picked up can cause jitter in both switcher outputs.
- Output capacitors should be close to the loads, where the filtering will help most; small ceramic capacitors (~1µF) in parallel help for high frequency transients. Input capacitors should be near the VIN pins of the FETs; the input capacitor GNDs should be close to the lower FET GND as well.
- The VIN plane should be large to heatsink the upper FET effectively, since the drain pin is usually the thermal node. By the same reasoning then, the phase node plane should also be large, since the lower FET drain is connected there. However, the phase node plane couples high frequency switching noise to other levels nearby, so it should be minimized for that reason. And don't route any sensitive or high impedance signals over the phase planes.
- GND: All of the "quiet" analog functions (mostly the top, left and bottom of Figure 2 or 3) should share a common IC GND, tied to the metal pad, and the GND and PGND pins. These include components associated with the following pins: VCC, VCC12, FB1, FB2, FB3, REFIN, REFOUT, VREF, FS_SYNC, SS1/EN1, SS2/EN2, SS3/EN3, GND, PGND. The metal pad under the IC can be extended as a local top (or bottom) layer GND plane; if thermal vias are used to a plane on the opposite layer, that too can be used as a local GND plane. Vias to the GND plane only are still acceptable, as long as they are local to the IC area. Each output section should have its own local power GND area, away from the IC GND. Finally, all of the GND's can be connected together.

Several placement approaches are possible:

- IC and output FETs, caps, and inductors on top level (tallest heights); most of the miscellaneous resistors and capacitors (all small heights) on the bottom level; this allows most of the analog components to be grouped near the pins, with vias to the pins. The IC can also be placed on the bottom.
- All components on top level, with output components facing pins 13-24 side of IC, and input components facing pins 1-12. This has less flexibility for close placement of the analog components, but it is still easy to accomplish, as long as there aren't too many other board size or shape constraints.
- In either case, it is recommended that the IC and its associated components have a local GND, separated from the output stage GNDs, but connected through the GND plane.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

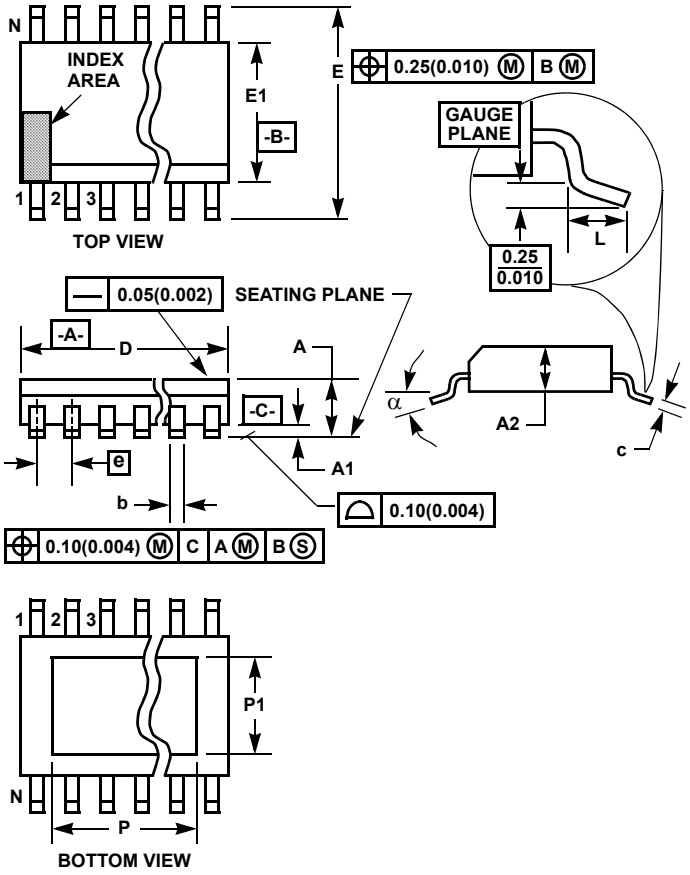
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Thin Shrink Small Outline Exposed Pad Plastic Packages (EPTSSOP)



M24.173B

24 LEAD THIN SHRINK SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.000	0.006	0.00	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.303	0.311	7.70	7.90	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-
P	-	0.197	-	5.00	11
P1	-	0.126	-	3.20	11

NOTES: Rev. 1 11/03

1. These package dimensions are within allowable dimensions of JEDEC MO-153-ADT, Issue F.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

ISL6534CRZ ISL6534CRZ-T ISL6534CVZ ISL6534CVZ-T