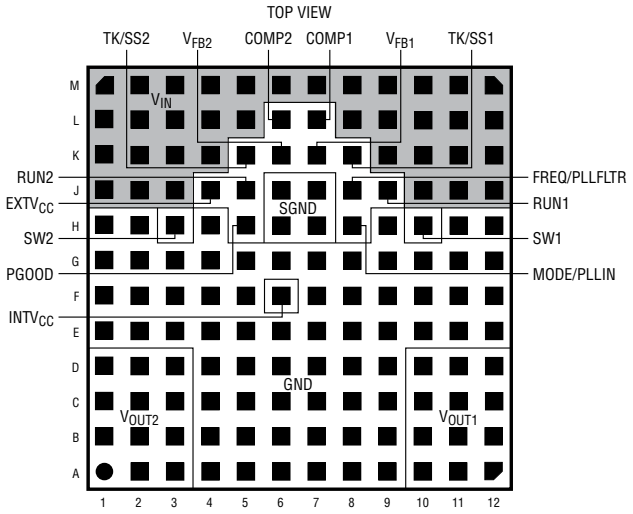
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 28V
$INTV_{CC}$, PGOOD, RUN1, RUN2, $EXTV_{CC}$..... –0.3V to 6V
V_{FB1}, V_{FB2} ..... –0.3V to 2.7V
COMP1, COMP2 (Note 4)..... –0.3V to 2.7V
MODE/PLLIN, TK/SS1, TK/SS2,
FREQ/PLLFLTR .....–0.3V to $INTV_{CC}$
V_{OUT1}, V_{OUT2}..... 0.8V to 5V
Internal Operating Temperature Range
(Note 2).....–40°C to 125°C
Maximum Reflow Body Temperature..... 245°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
144-LEAD (15mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 13.4°C/W, $\theta_{JCbottom}$ = 6°C/W, θ_{JCtop} = 16°C/W, $\theta_{JB} \approx \theta_{JCbottom}$, $\theta_{JB} + \theta_{BA}$ = 13.4° C/W, θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS WEIGHT = 1.7g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4619EV#PBF	Au (RoHS)	LTM4619V	e4	LGA	3	–40°C to 125°C
LTM4619IV#PBF	Au (RoHS)	LTM4619V	e4	LGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Markings:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  http://www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application in Figure 19. Specified as each channel. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage	V_{IN} ≤ 5.5V, Connect V_{IN} and $INTV_{CC}$ Together	●	4.5		26.5	V
$V_{OUT1, 2(RANGE)}$	Output Voltage Range	V_{IN} = 5.5V to 26.5V	●	0.8		5.0	V
$V_{OUT1, 2(DC)}$	Output Voltage	C_{IN} = 10µF ×1, C_{OUT} = 100µF Ceramic, 100µF POSCAP, R_{SET} = 28.0kΩ					
		V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 0A		2.483	2.52	2.557	V
		V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 4A	●	2.470	2.52	2.570	V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Thresholds	V_{INTVCC} Rising		2.00	2.2	2.35	V
		V_{INTVCC} Falling		1.85	2.0	2.15	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application in Figure 19. Specified as each channel. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 10µF, C_{OUT} = 100µF, V_{OUT} = 2.5V V_{IN} = 12V			0.25		A
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT1} = 2.5V, Switching Continuous V_{IN} = 12V, V_{OUT2} = 2.5V, Switching Continuous V_{IN} = 26.5V, V_{OUT1} = 2.5V, Switching Continuous V_{IN} = 26.5V, V_{OUT2} = 2.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 20V			30 30 40 40 40		mA mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 4A V_{IN} = 26.5V, V_{OUT} = 2.5V, I_{OUT} = 4A			0.97 0.480		A A
$INTV_{CC}$	Internal V_{CC} Voltage	V_{IN} = 12V, V_{RUN} > 2V, No Load		4.8	5	5.2	V
$EXTV_{CC}$	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
Output Specifications							
$I_{OUT1, 2(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 2.5V (Note 5)		0		4	A
$\frac{\Delta V_{OUT1(LINE)}}{V_{OUT(NOM)}}$	Line Regulation Accuracy	V_{OUT} = 2.5V, V_{IN} from 6V to 26.5V I_{OUT} = 0A For Each Output	 ●		0.15 0.25	0.3 0.5	% %
$\frac{\Delta V_{OUT2(LINE)}}{V_{OUT(NOM)}}$	Line Regulation Accuracy	V_{OUT} = 2.5V, V_{IN} from 6V to 26.5V I_{OUT} = 0A For Each Output	 ●		0.15 0.25	0.3 0.5	% %
$\frac{\Delta V_{OUT1(LOAD)}}{V_{OUT1(NOM)}}$	Load Regulation Accuracy	For Each Output, V_{OUT} = 2.5V, 0A to 4A (Note 5) V_{IN} = 12V	●		0.6	0.8	±%
$\frac{\Delta V_{OUT2(LOAD)}}{V_{OUT2(NOM)}}$	Load Regulation Accuracy	For Each Output, V_{OUT} = 2.5V, 0A to 4A (Note 5) V_{IN} = 12V	●		0.6	0.8	±%
$V_{OUT1, 2(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF X5R Ceramic V_{IN} = 12V, V_{OUT} = 2.5V V_{IN} = 26.5V, V_{OUT} = 2.5V			 20 25		 mV mV
f_S	Output Ripple Voltage Frequency	I_{OUT} = 2A, V_{IN} = 12V, V_{OUT} = 2.5V FREQ/PLLFLTR = $INTV_{CC}$			780		kHz
$\Delta V_{OUTSTART}$	Turn-On Overshoot	C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, I_{OUT} = 0A V_{IN} = 12V V_{IN} = 26.5V			 10 10		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, I_{OUT} = 0A Resistive Load, V_{IN} = 12V V_{IN} = 26.5V			 0.250 0.130		 ms ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, V_{IN} = 12V			 15		 mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF X5R Ceramic, V_{OUT} = 2.5V, V_{IN} = 12V			 10		 µs
I_{OUTPK}	Output Current Limit	C_{OUT} = 100µF X5R Ceramic, V_{IN} = 6V, V_{OUT} = 2.5V V_{IN} = 26.5V, V_{OUT} = 2.5V			 12 11		 A A
Control Section							
V_{FB1}, V_{FB2}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 2.5V	 ●	0.792 0.788	0.8 0.8	0.808 0.810	V
$I_{TK/SS1, 2}$	Soft-Start Charge Current	$V_{TK/SS}$ = 0V, V_{OUT} = 2.5V		0.9	1.3	1.7	µA
DF_{MAX}	Maximum Duty Factor	In Dropout (Note 4)			97		%
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application in Figure 19. Specified as each channel. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0V		210	250	290	kHz
f_{HIGH}	Highest Frequency	V_{FREQ} ≥ 2.4V		700	780	860	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
I_{FREQ}	Frequency Setting Sinking Current Sourcing Current	 $f_{MODE} > f_{OSC}$ $f_{MODE} < f_{OSC}$			 –13 13		 µA µA
$V_{RUN1, 2}$	RUN Pin ON/OFF Threshold	RUN Rising RUN Falling		1.1 1.02	1.22 1.14	1.35 1.27	V V
R_{FB1}, R_{FB2}	Resistor Between V_{OUT} and V_{FB} Pins for Each Channel			60.1	60.4	60.7	kΩ
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±2	µA
ΔV_{PGOOD}	PGOOD Range	V_{FB} Ramping Negative V_{FB} Ramping Positive		–5 5	–7.5 7.5	–10 10	% %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4619E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4619I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The two outputs are tested separately and the same testing condition is applied to each output.

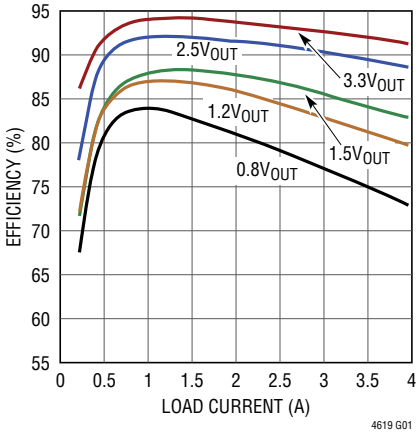
Note 4: 100% tested at wafer level only.

Note 5: See Output Current Derating curves for different V_{IN}, V_{OUT} and T_A.

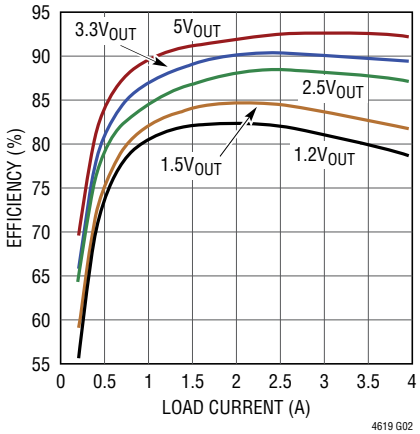
TYPICAL PERFORMANCE CHARACTERISTICS

(Refer to Figures 19 and 20)

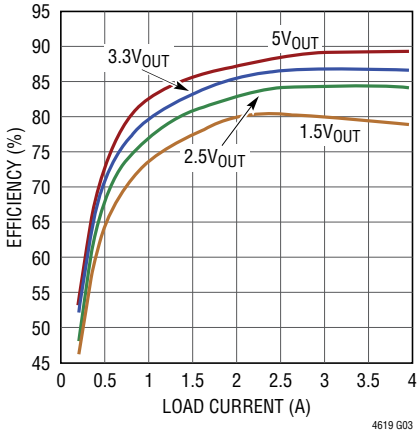
Efficiency vs Load Current with $5V_{IN}$ (f = 500kHz for $0.8V_{OUT}$, $1.2V_{OUT}$ and $1.5V_{OUT}$)



Efficiency vs Load Current with $12V_{IN}$ (f = 500kHz for $1.2V_{OUT}$ and $1.5V_{OUT}$)

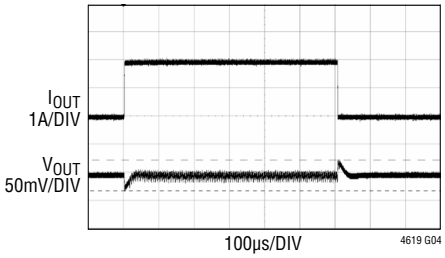


Efficiency vs Load Current with $24V_{IN}$ (f = 500kHz for $1.5V_{OUT}$)



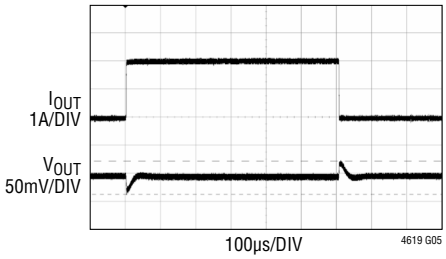
TYPICAL PERFORMANCE CHARACTERISTICS (Refer to Figures 19 and 20)

1.2V Output Transient Response



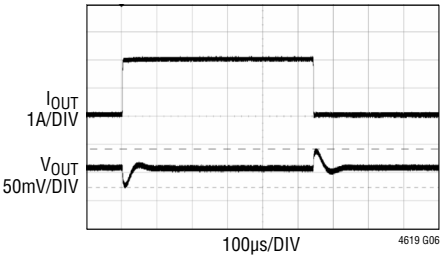
$6V_{IN}$ $1.2V_{OUT}$ AT 2A/µs LOAD STEP
f = 780kHz
C_{OUT} 2× 22µF, 6.3V X5R CERAMIC
C_{OUT} 1× 330µF, 6.3V SANYO POSCAP

1.5V Output Transient Response



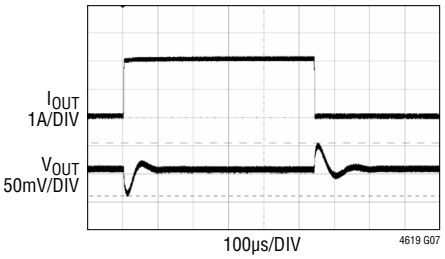
$6V_{IN}$ $1.5V_{OUT}$ AT 2A/µs LOAD STEP
f = 780kHz
C_{OUT} 2× 22µF, 6.3V X5R CERAMIC
C_{OUT} 1× 330µF, 6.3V SANYO POSCAP

2.5V Output Transient Response



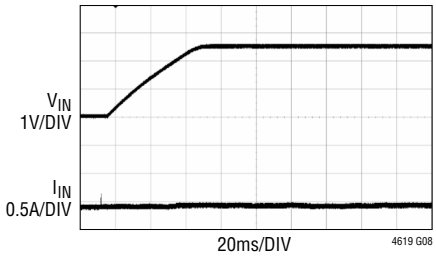
$6V_{IN}$ $2.5V_{OUT}$ AT 2A/µs LOAD STEP
f = 780kHz
C_{OUT} 2× 22µF, 6.3V X5R CERAMIC
C_{OUT} 1× 330µF, 6.3V SANYO POSCAP

3.3V Output Transient Response



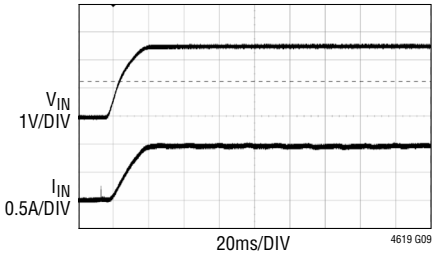
$6V_{IN}$ $3.3V_{OUT}$ AT 2A/µs LOAD STEP
f = 780kHz
C_{OUT} 2× 22µF, 6.3V X5R CERAMIC
C_{OUT} 1× 330µF, 6.3V SANYO POSCAP

Start-Up, I_{OUT} = 0A



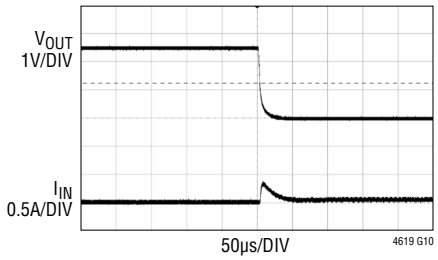
V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 0A
C_{OUT} = 2× 22µF 10V
AND 1× 100µF 6.3V CERAMIC CAPs
$C_{SOFTSTART}$ = 0.1µF
USE RUN PIN TO CONTROL START-UP

Start-Up, I_{OUT} = 4A



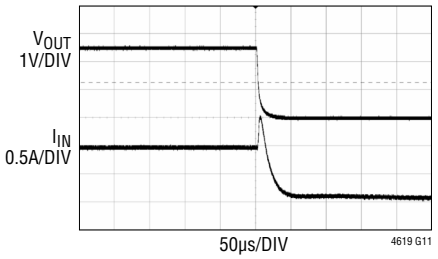
V_{IN} = 12V, V_{OUT} = 2.5V,
I_{OUT} = 4A RESISTIVE LOAD
C_{OUT} = 2× 22µF 10V,
AND 1× 100µF 6.3V CERAMIC CAPs
$C_{SOFTSTART}$ = 0.1µF
USE RUN PIN TO CONTROL START-UP

Short Circuit, I_{OUT} = 0A



V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 0A
C_{OUT} = 2× 22µF 10V,
AND 1× 100µF 6.3V CERAMIC CAPs

Short Circuit, I_{OUT} = 4A



V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 4A
C_{OUT} = 2× 22µF 10V,
AND 1× 100µF 6.3V CERAMIC CAPs

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (J1 to J3, J10 to J12, K1 to K4, K9 to K12, L1 to L5, L8 to L12, M1 to M12): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins. For V_{IN} < 5.5, tie V_{IN} and $INTV_{CC}$ together.

V_{OUT1}, V_{OUT2} (A10 to D10, A11 to D11, A12 to D12, A1 to D1, A2 to D2, A3 to D3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins.

PGND (H1, H2, H4, H9, H11, H12, G1 to G12, F1 to F5, F7 to F12, E1 to E12, D4 to D9, C4 to C9, B4 to B9, A4 to A9): Power ground pins for both input and output returns.

$INTV_{CC}$ (F6): Internal 5V Regulator Output. This pin is for additional decoupling of the 5V internal regulator.

$EXTV_{CC}$ (J4): External Power Input to Controller. When $EXTV_{CC}$ is higher than 4.7V, the internal 5V regulator is disabled and external power supplies current to reduce the power dissipation in the module. This will improve the efficiency more at high input voltages.

SGND (J6, J7, H6, H7): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to PGND in the application.

MODE/PLLIN (H8): Mode selection or external synchronization pin. Tying this pin high enables pulse-skipping mode. Tying this pin low enables force continuous operation. Floating this pin enables Burst Mode operation. A clock on the pin will force the controller into the continuous mode of operation and synchronize the internal oscillator. The suitable synchronizable frequency range is 250kHz to 780kHz subject to inductor ripple current limits described in the FREQ/PLLFLTR pin section. The external clock input high threshold is 1.6V, while the input low threshold is 1V.

FREQ/PLLFLTR (J8): Frequency Selection Pin. An internal lowpass filter is tied to this pin. The frequency can be selected from 250kHz to 780kHz by varying the DC voltage on this pin from 0V to 2.4V. The nominal frequency setting is 500kHz. Frequency selection can be modified as long as the inductor ripple current is less ≈40% to 50% at the output current

$$I_{RIPPLE} = \frac{\frac{1}{FREQ}\left(1-\frac{V_{OUT}}{V_{IN}}\right)V_{OUT}}{L}$$

Where FREQ is selected operating frequency and L is the inductor value. Leave this pin floating when external synchronization is used.

TK/SS1, TK/SS2 (K8, K5): Output Voltage Tracking and Soft-Start Pins. Internal soft-start currents of 1.3µA charge the soft-start capacitors. See the Applications Information section to use the tracking function.

V_{FB1}, V_{FB2} (K7, K6): The negative input of the error amplifier. Internally, this pin is connected to V_{OUT} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND pins. See the Applications Information section for details.

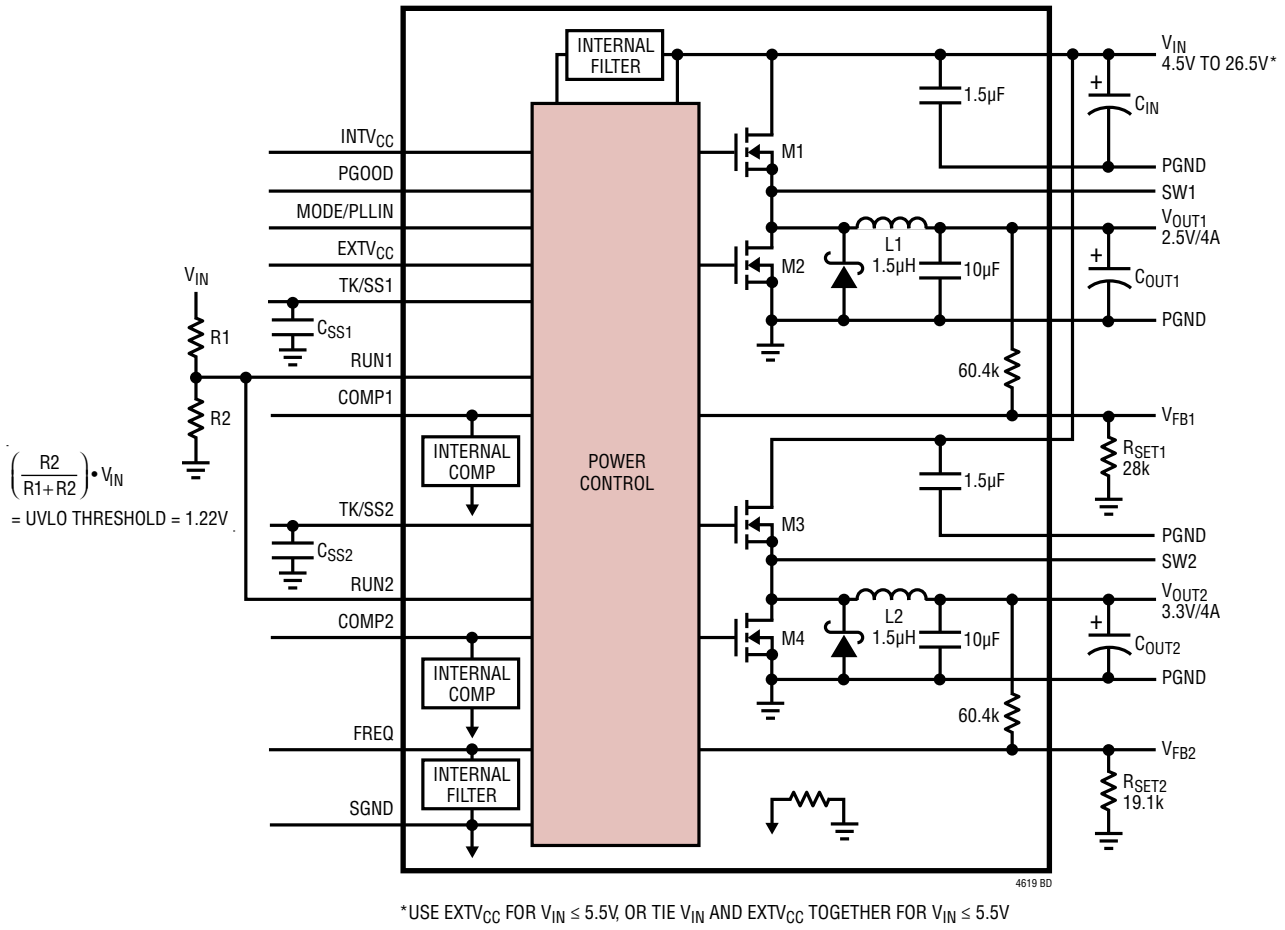
COMP1, COMP2 (L7, L6): Current Control Threshold and Error Amplifier Compensation Point. The module has been internally compensated for most I/O ranges.

PGOOD (H5): Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

RUN1, RUN2 (J9, J5): Run Control Pins. 0.5µA pull-up currents on these pins turn on the module if these pins are floating. Forcing either of these pins below 1.2V will shut down the corresponding outputs. An additional 4.5µA pull-up current is added to this pin, once the RUN pin rises above 1.2V. Also, active control or pull-up resistors can be used to enable the RUN pin. The maximum voltage is 6V on these pins.

SW1, SW2 (H10, H3): Switching Test Pins. These pins are provided externally to check the operation frequency.

SIMPLIFIED BLOCK DIAGRAM



*USE $EXTV_{CC}$ FOR $V_{IN} \leq 5.5V$, OR TIE V_{IN} AND $EXTV_{CC}$ TOGETHER FOR $V_{IN} \leq 5.5V$

Figure 1. Simplified LTM4619 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 26.5V, V_{OUT1} = 2.5V, V_{OUT2} = 3.3V)	I_{OUT1} = 4A, I_{OUT2} = 4A		10			µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement (V_{IN} = 4.5V to 26.5V, V_{OUT1} = 2.5V, V_{OUT2} = 3.3V)	I_{OUT1} = 4A I_{OUT2} = 4A			200 200		µF µF

OPERATION

The LTM4619 is a dual-output standalone non-isolated switching mode DC/DC power supply. It can deliver up to 4A (DC current) for each output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.8VDC to 5.0VDC over 4.5V to 26.5V input voltages. The typical application schematic is shown in Figure 19.

The LTM4619 has integrated constant frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 780kHz. To reduce switching noise, the two outputs are interleaved with 180° phase internally and can be synchronized externally using the MODE/PLLIN pin.

With current mode control and internal feedback loop compensation, the LTM4619 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and current foldback in a short-circuit condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±7.5% window around the regulation point. The power good pin is disabled during start-up.

Pulling the RUN pin below 1.2V forces the controller into its shutdown state, by turning off both MOSFETs. The TK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

The LTM4619 is internally compensated to be stable over all operating conditions. LTpowerCAD™ is available for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground. Multiphase operation can be easily employed with the synchronization.

High efficiency at light loads can be accomplished with selectable Burst Mode operation or pulse-skipping mode using the MODE/PLLIN pin. Efficiency graphs are provided for light load operations in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The typical LTM4619 application circuit is shown in Figure 19. External component selection is primarily determined by the maximum load current and output voltage.

Output Voltage Programming

The PWM controller has an internal 0.8V reference voltage. As shown in the block diagram, a 60.4k internal feedback resistor R_{FB} connects V_{OUT} to V_{FB} pin. The output voltage will default to 0.8V with no feedback resistor. Adding a resistor R_{SET} from V_{FB} pin to SGND programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{60.4k + R_{SET}}{R_{SET}}$$

or equivalently

$$R_{SET} = \frac{60.4k}{\left(\frac{V_{OUT}}{0.8V} - 1\right)}$$

Table 1. R_{SET} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.8	1.2	1.5	1.8	2.5	3.3	5
R_{SET} (kΩ)	Open	121	68.1	48.7	28.0	19.1	11.5

Input Capacitors

The LTM4619 module should be connected to a low AC-impedance DC source. Two 1.5µF input ceramic capacitors are included inside the module. Additional input capacitors are needed if a large load is required up to the 4A level. A 47µF to 100µF surface mount aluminum electrolytic capacitor can be used for more input bulk capacitance. This bulk capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or a polymer capacitor. One 10µF ceramic input capacitor is typically rated for 2A of RMS ripple current, so the RMS input current at the worst case for each output at 4A maximum current is about 2A. If a low inductance plane is used to power the device, then two 10µF ceramic capacitors are enough for both outputs at 4A load and no external input bulk capacitor is required.

Output Capacitors

The LTM4619 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 47µF to 220µF. Additional output filtering may be required by the system designer. If further reduction of output ripple or dynamic transient spikes is required, LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD calculates the output ripple reduction as the number of implemented phases increased by N times.

APPLICATIONS INFORMATION

Mode Selections and Phase-Locked Loop

The LTM4619 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode. To select the forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.8V. To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin.

Frequency Synchronization

A phase-lock loop is available on the LTM4619 to synchronize the internal clock to an external clock source connected on the MODE/PLLIN pin. The clock high level needs to be higher than 1.6V and the clock low level needs to be lower than 1V. The frequency programming voltage and or the programming voltage divider must be removed from the FREQ/PLLFLTR pin when synchronizing to an external clock. The FREQ/PLLFLTR pin has the required onboard PLL filter components for clock synchronization. The LTM4619 will default to forced continuous mode while being clock synchronized. Channel 1 is synchronized to the rising edge on the external clock, and channel 2 is 180 degrees out-of-phase with the external clock.

Frequency Selection

The switching frequency of the LTM4619's controllers can be selected using the FREQ/PLLFLTR pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ/PLLFLTR pin can be set from 0V to 2.4V to program the controller's operating frequency from 250kHz to 780kHz using a voltage divider to $INTV_{CC}$ (see Figure 20). The typical frequency is 780kHz. If the output is too low or the minimum on-time is reached, the frequency needs to decrease to enlarge the turn-on time. Otherwise, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

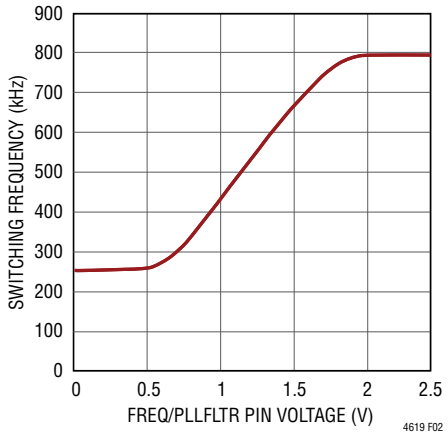


Figure 2. Switching Frequency vs FREQ/PLLFLTR Pin Voltage

APPLICATIONS INFORMATION

Soft-Start and Tracking

The LTM4619 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When one particular channel is configured to soft-start by itself, a capacitor should be connected to its TK/SS pin. This channel is in the shutdown state if its RUN pin voltage is below 1.2V. Its TK/SS pin is actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.2V, the channel powers up. A soft-start current of 1.3µA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.8V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = \frac{0.8V \bullet C_{SS}}{1.3\mu A}$$

Output voltage tracking can be programmed externally using the TK/SS pin. The master channel is divided down with an external resistor divider that is the same as the slave channel's feedback divider to implement coincident tracking. The LTM4619 uses an accurate 60.4k resistor internally for the top feedback resistor. Figure 3 shows an example of coincident tracking. Figure 4 shows the output voltages with coincident tracking.

$$V_{SLAVE} = \left(1 + \frac{R1}{R2}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's TK/SS2 pin. V_{TRACK} has a control range of 0V to 0.8V. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point.

Ratiometric modes of tracking can be achieved by selecting different divider resistors values to change the output tracking ratio. The master output must be greater than the slave output for the tracking to work. Master and slave data inputs can be used to implement the correct resistors values for coincident or ratiometric tracking.

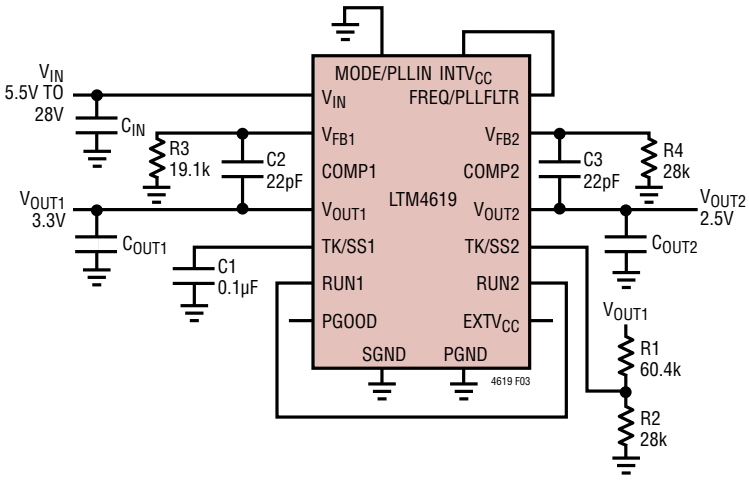


Figure 3. Example of Coincident Tracking

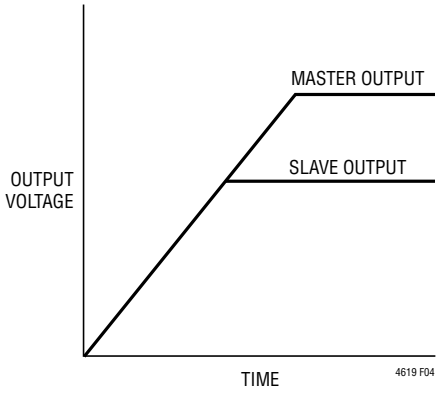


Figure 4. Coincident Tracking

APPLICATIONS INFORMATION

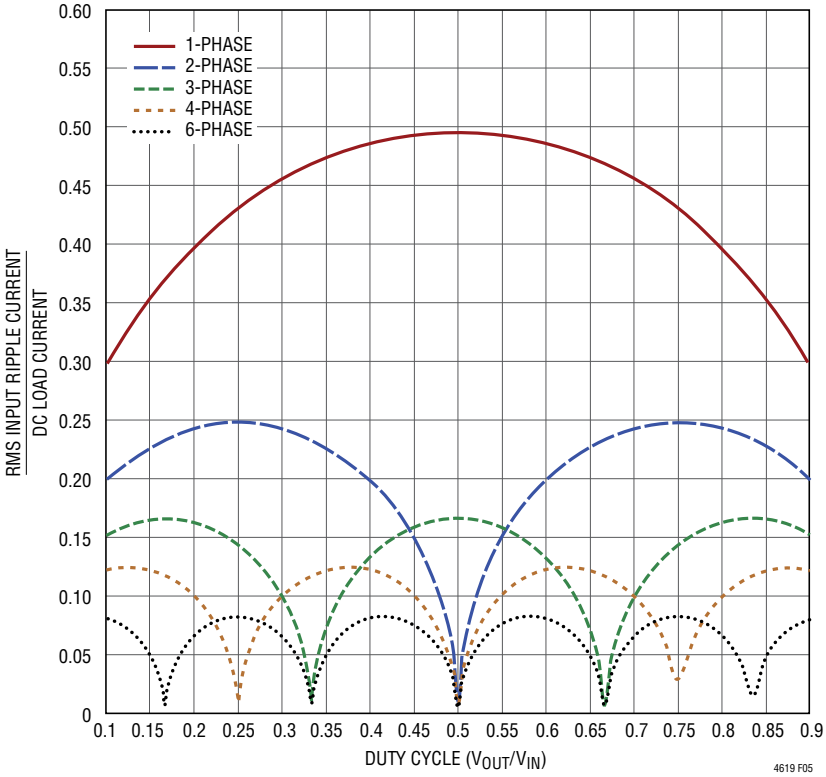


Figure 5. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six Phases

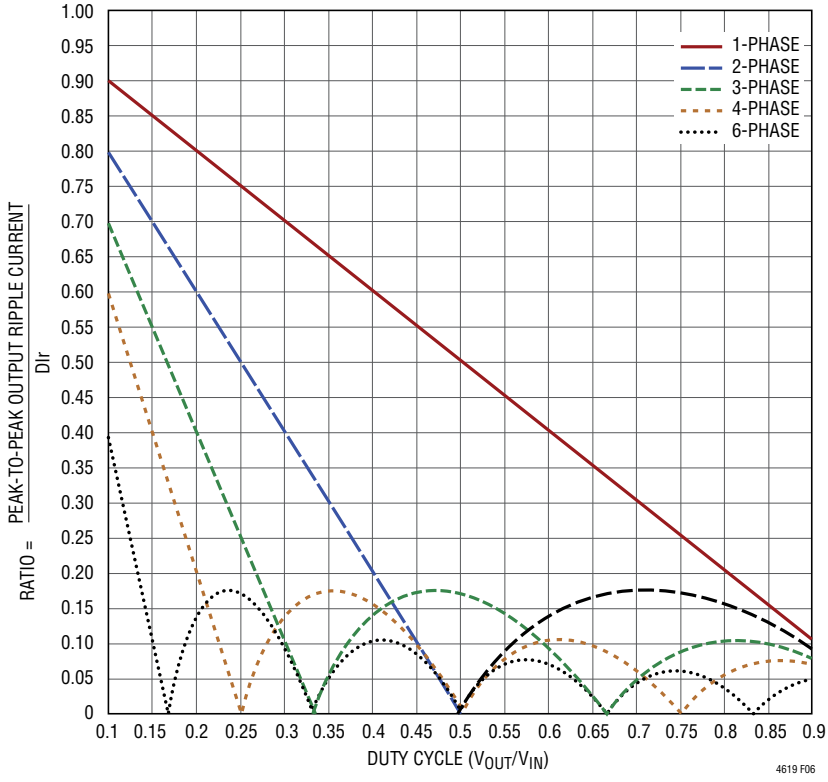


Figure 6. Normalized Output Ripple Current vs Duty Cycle, DIr = V_{OUT} T/L

APPLICATIONS INFORMATION

Multiphase Operation

Multiphase operation with multiple LTM4619 devices in parallel will lower the effective input RMS ripple current as well as the output ripple current due to the interleaving operation of the regulators. Figure 5 provides a ratio of input RMS ripple current to DC load current as a function of duty cycle and the number of paralleled phases. Choose the corresponding duty cycle and the number of phases to get the correct ripple current value. For example, the 2-phase parallel for one LTM4619 design provides 8A at 2.5V output from a 12V input. The duty cycle is DC = 2.5V/12V = 0.21. The 2-phase curve has a ratio of ~0.25 for a duty cycle of 0.21. This 0.25 ratio of RMS ripple current to a DC load current of 8A equals ~2A of input RMS ripple current for the external input capacitors.

The effective output ripple current is lowered with multiphase operations as well. Figure 6 provides a ratio of peak-to-peak output ripple current to the normalized output ripple current as a function of duty cycle and the number of paralleled phases. Choose the corresponding duty cycle and the number of phases to get the correct output ripple current ratio value. If a 2-phase operation is chosen at $12V_{IN}$ to $2.5V_{OUT}$ with a duty cycle of 21%, then 0.6 is the ratio of the normalized output ripple current to inductor ripple DIr at zero duty cycle. This leads to ~1.3A of the effective output ripple current ΔI_L if the DIr is at 2.2A. Refer to Application Note 77 for a detailed explanation of the output ripple current reduction as a function of paralleled phases.

The output ripple voltage has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. Therefore, the output ripple voltage can be calculated with the known effective output ripple current. The equation:

$$\Delta V_{OUT(P-P)} \approx \Delta I_L/(8 \bullet f \bullet N \bullet C_{OUT}) + ESR \bullet \Delta I_L$$

where f is frequency and N is the number of parallel phases.

RUN Pin

The RUN pins can be used to enable or sequence the particular regulator channel. The RUN pins have their own internal 0.5µA current source to pull up the pin to 1.2V, and then the current increases to 4.5µA above 1.2V. Careful consideration is needed to assure that board contamination or residue does not load down the 0.5µA pull-up current. Otherwise active control to these pins can be used to enable the regulators. A voltage divider can be used from V_{IN} to set an enable point that can also be used as a UVLO feature for the regulator. The resistor divider needs to be low enough resistance to swamp out the pull-up current sources to prevent unintended activation of the device. See the Simplified Block Diagram.

Power Good

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when either V_{FB} pin voltage is not within ±7.5% of the 0.8V reference voltage. The PGOOD pin is also pulled low when either RUN pin is below 1.2V or when the LTM4619 is in the soft-start or tracking phase. When the V_{FB} pin voltage is within the ±7.5% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when both V_{FB} pins are within the ±7.5% window. However, there is an internal 17µs power bad mask when either V_{FB} goes out of the ±7.5% window.

APPLICATIONS INFORMATION

$INTV_{CC}$ and $EXTV_{CC}$

The $INTV_{CC}$ is the internal 5V regulator that powers the LTM4619 internal circuitry and drives the power MOSFETs. The input voltage of the LTM4619 must be 6V or above for the $INTV_{CC}$ to regulate to the proper 5V level due to the internal LDO dropout from the input voltage. For applications that need to operate below 6V input, then the input voltage can be connected directly to the $EXTV_{CC}$ pin to bypass the LDO dropout concern, or an external 5V supply can be used to power the $EXTV_{CC}$ pin when the input voltage is at high end of the supply range to reduce power dissipation in the module. For example the dropout voltage for 24V input would be 24V – 5V = 19V. This 19V headroom then multiplied by the power MOSFET drive current of ~15mA would equal ~0.3W additional power dissipation. So utilizing an external 5V supply on the $EXTV_{CC}$ would improve design efficiency and reduce device temperature rise.

Slope Compensation

The module has already been internally compensated for all output voltages. LTpowerCAD is available for control loop optimization.

Burst Mode Operation and Pulse-Skipping Mode

The LTM4619 regulator can be placed into high efficiency power saving modes at light load condition to conserve power. The Burst Mode operation can be selected by floating the MODE/PLLIN pin, and pulse-skipping mode can be selected by pulling the MODE/PLLIN pin to $INTV_{CC}$. Burst Mode operation offers the best efficiency at light load, but output ripple will be higher and lower frequency ranges are capable which can interfere with some systems. Pulse-skipping mode efficiency is not as good as Burst Mode operation, but this mode only skips pulses to save efficiency and maintains a lower output ripple and a higher switching frequency. Burst Mode operation and pulse-skipping mode efficiencies can be reviewed in graph supplied in the Typical Performance Characteristics section.

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4619 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4619 provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to one-third of its full current limit value. Foldback current limiting is disabled during soft-start and tracking up.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased in the following:

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1 θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.

2 $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3 θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4 θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 7; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4619, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4619 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4619 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

APPLICATIONS INFORMATION

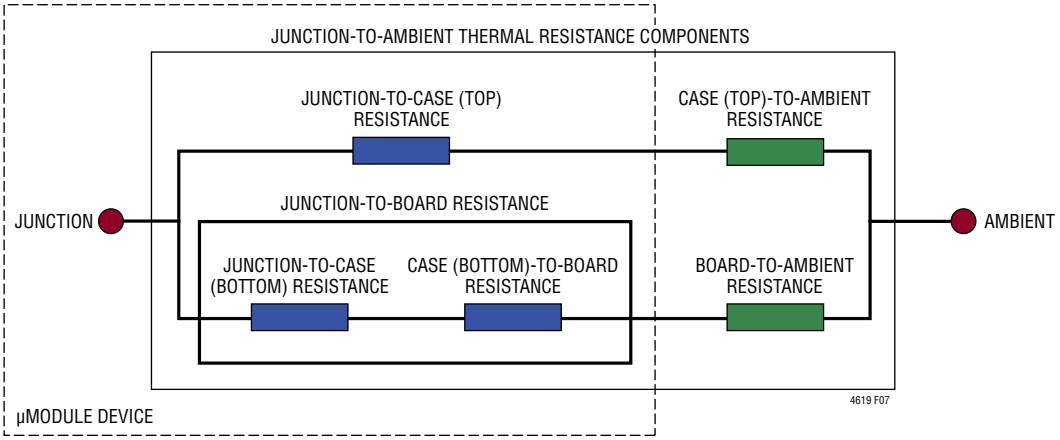


Figure 7. Graphical Representation of JESD51-12 Thermal Coefficients

The 1.5V and 3.3V power loss curves in Figures 8 and 9 can be used in coordination with the load current derating curves in Figures 10 to 17 for calculating an approximate Θ_{JA} thermal resistance for the LTM4619 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.35 multiplicative factor at 120°C. The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at 8A of load with low ambient temperature. The output voltages are 1.5V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 12, the load current is derated to 5A at ~95°C with no air or heat sink and the power loss for the 12V to 1.5V at 5A output is about 1.83W. The 1.83W loss is calculated with the 1.35W room temperature loss from the 12V to 1.5V power loss curve at 5A, and the 1.35 multiplying factor at 120°C ambient. If the 95°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 25°C divided by 1.83W equals a 13.6°C/W Θ_{JA} thermal resistance. Table 2 specifies a 13.4°C/W value which is pretty close. The airflow graphs are more accurate due to the fact that the ambient temperature environment is controlled better with airflow. As an example in Figure 14, the load current is derated to 5A at ~95°C with 400LFM of airflow and the power loss for the 12V to 3.3V at 5A output is ~2.5W. The 2.5W loss is calculated with the ~1.85W room temperature loss from the 12V to 3.3V power loss curve at 5A, and the 1.35 multiplying factor at 120°C ambient. If the 95°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 25°C divided by 2.5W equals a 10°C/W Θ_{JA} thermal resistance. Table 2 specifies a 9.7°C/W value which is pretty close. Tables 2 and 3 provide equivalent thermal resistances for 1.5V and 3.3V outputs with and without airflow and heat sinking.

The derived thermal resistances in Tables 2 and 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed in Table 3.

APPLICATIONS INFORMATION

Table 2. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEATSINK	Θ_{JA} (°C/W)
Figures 10, 12	6, 12	Figure 8	0	none	13.4
Figures 10, 12	6, 12	Figure 8	200	none	11.2
Figures 10, 12	6, 12	Figure 8	400	none	9.7
Figures 11, 13	6, 12	Figure 8	0	BGA Heatsink	12.6
Figures 11, 13	6, 12	Figure 8	200	BGA Heatsink	10.0
Figures 11, 13	6, 12	Figure 8	400	BGA Heatsink	9.6

Table 3. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEATSINK	Θ_{JA} (°C/W)
Figures 14, 16	12, 24	Figure 9	0	none	13.4
Figures 14, 16	12, 24	Figure 9	200	none	11.2
Figures 14, 16	12, 24	Figure 9	400	none	9.7
Figures 15, 17	12, 24	Figure 9	0	BGA Heatsink	12.6
Figures 15, 17	12, 24	Figure 9	200	BGA Heatsink	10.0
Figures 15, 17	12, 24	Figure 9	400	BGA Heatsink	9.6

HEATSINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424B00034G	www.aavidthermalloy.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

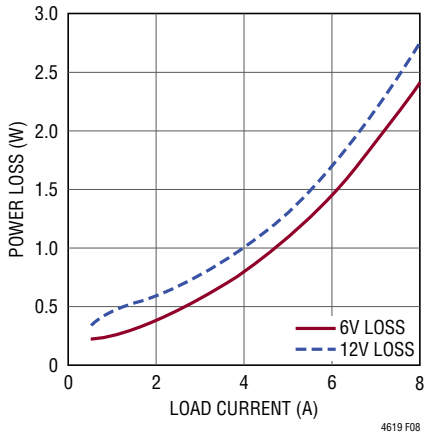


Figure 8. Power Loss at 1.5V Output

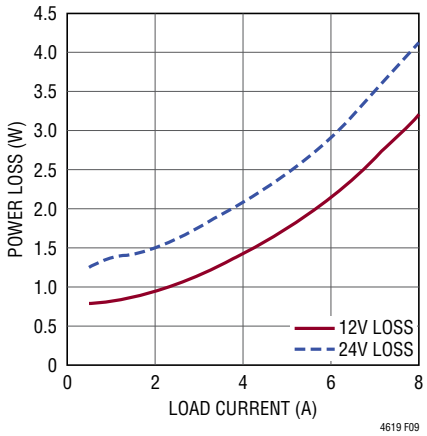


Figure 9. Power Loss at 3.3V Output

APPLICATIONS INFORMATION

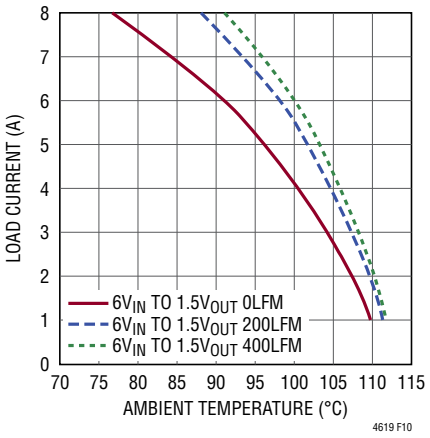


Figure 10. $6V_{IN}$ to $1.5V_{OUT}$ without Heat Sink

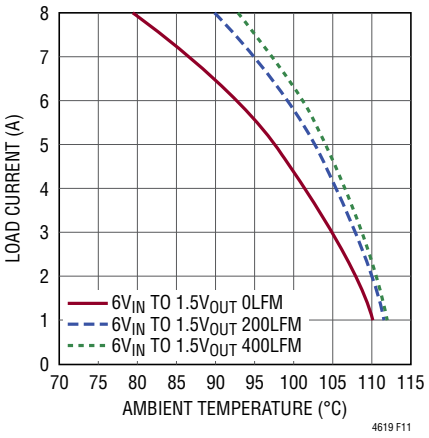


Figure 11. $6V_{IN}$ to $1.5V_{OUT}$ with Heat Sink

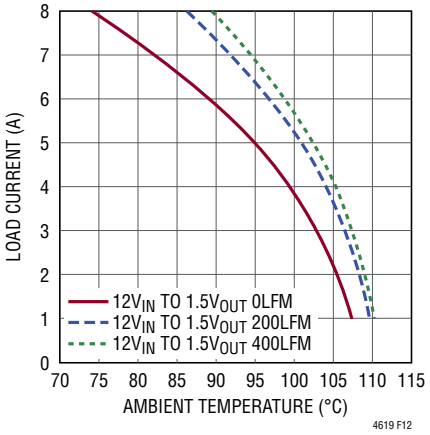


Figure 12. $12V_{IN}$ to $1.5V_{OUT}$ without Heat Sink

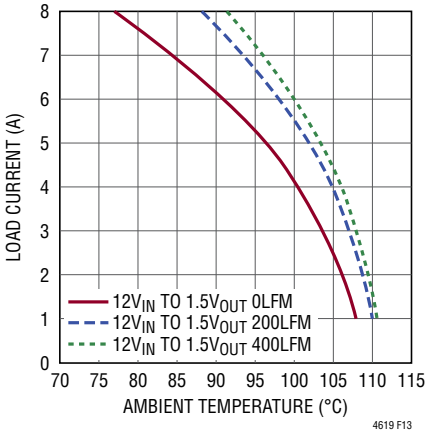


Figure 13. $12V_{IN}$ to $1.5V_{OUT}$ with Heat Sink

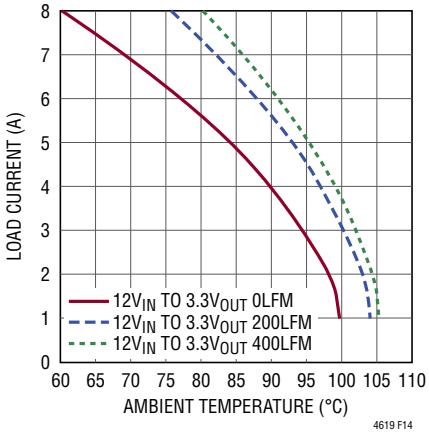


Figure 14. $12V_{IN}$ to $3.3V_{OUT}$ without Heat Sink

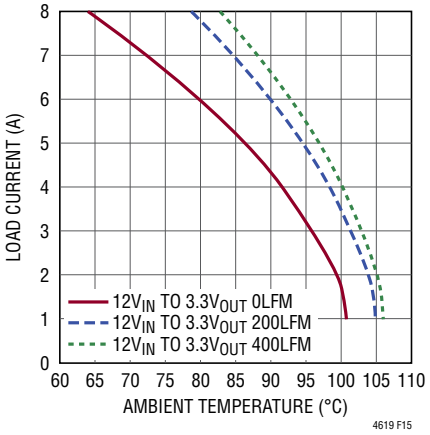


Figure 15. $12V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

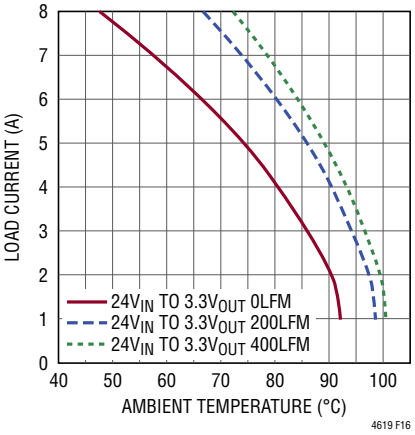


Figure 16. $24V_{IN}$ to $3.3V_{OUT}$ without Heat Sink

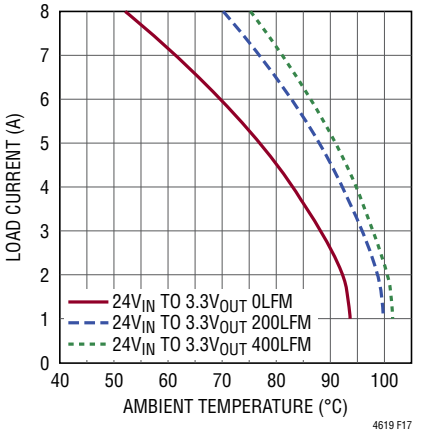


Figure 17. $24V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

APPLICATIONS INFORMATION

Safety Considerations

The LTM4619 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4619 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnections between top layer and other power layers.
- Do not put vias directly on the pads.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.
- Decouple the input and output grounds to lower the output ripple noise.

Figure 18 gives a good example of the recommended layout.

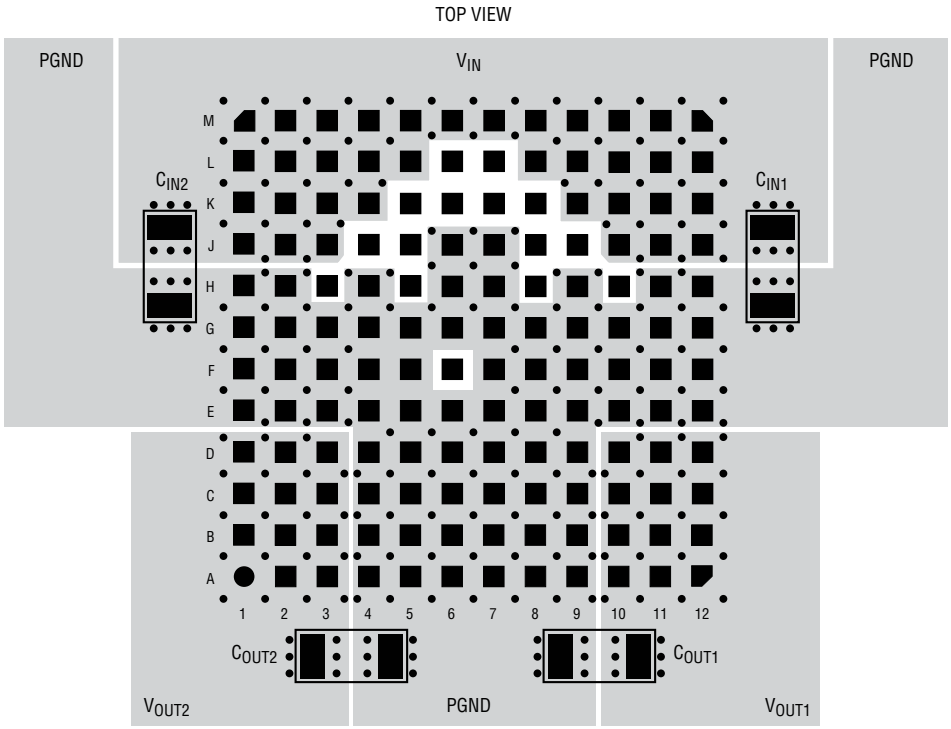


Figure 18. Recommended PCB Layout

TYPICAL APPLICATIONS

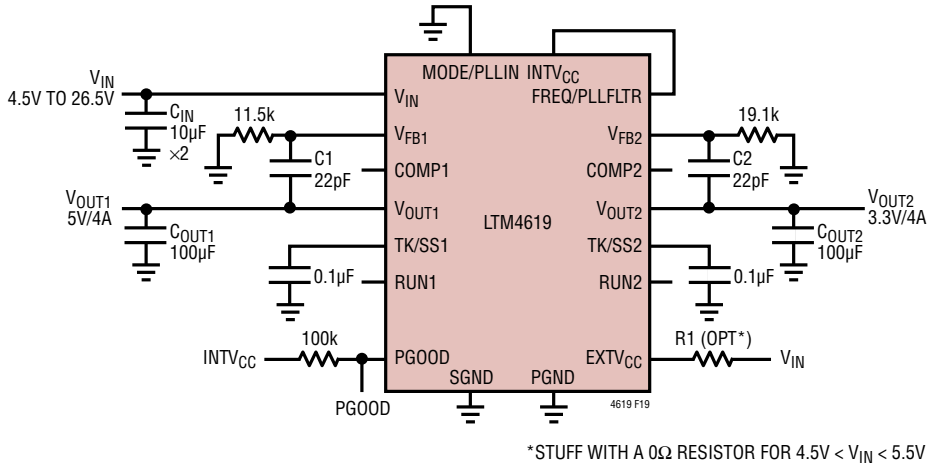


Figure 19. Typical 4.5V to 26.5V Input, 5V and 3.3V Outputs at 4A Design

TYPICAL APPLICATIONS

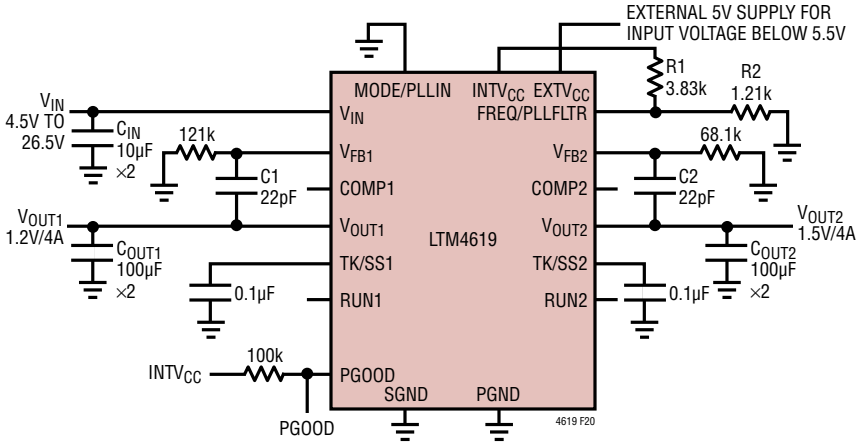


Figure 20. Typical 4.5V to 26.5V Input, 1.2V and 1.5V Outputs at 4A Design with Adjusted Frequency at 500kHz

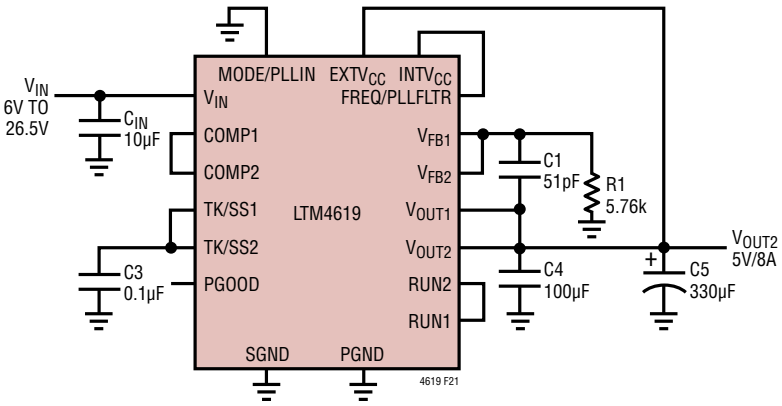


Figure 21. Output Paralleled LTM4619 Module for 5V Output at 8A Design

TYPICAL APPLICATIONS

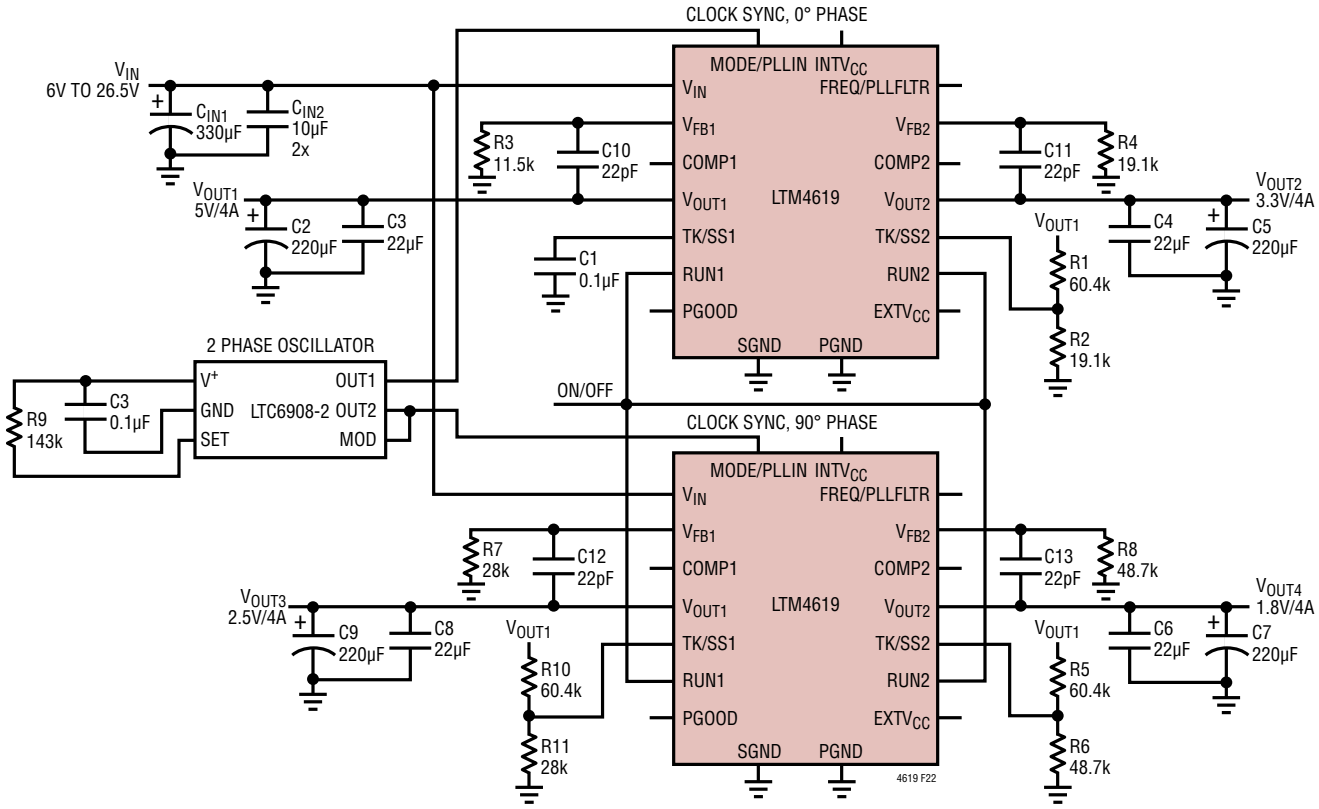


Figure 22. 4-Phase, Four Outputs (5V, 3.3V, 2.5V and 1.8V) with Tracking

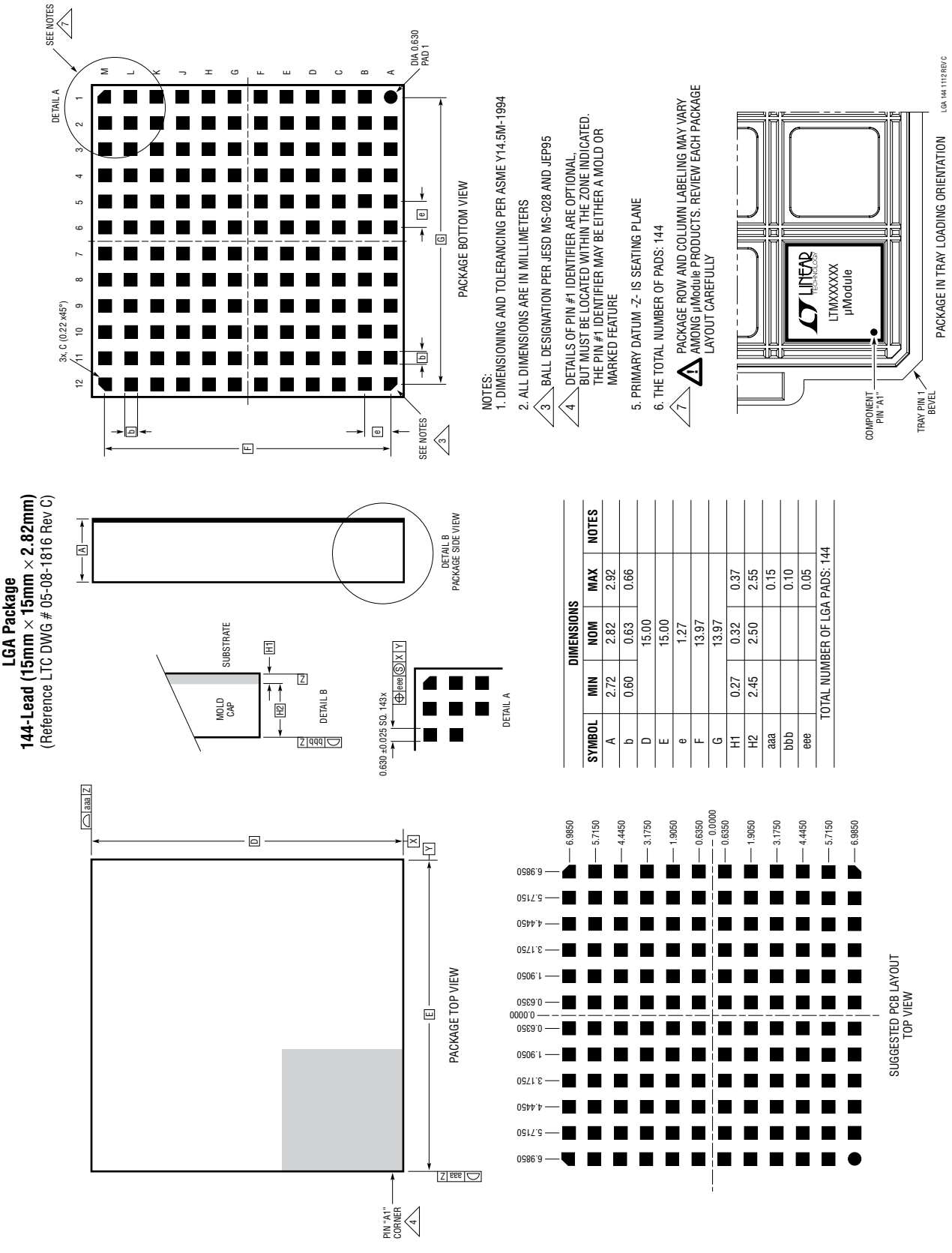
PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Assignment Table 4
(Arranged by Pin Function)

PIN NAME		PIN NAME		PIN NAME		PIN NAME	
A1	V_{OUT2}	D1	V_{OUT2}	G1	PGND	K1	V_{IN}
A2	V_{OUT2}	D2	V_{OUT2}	G2	PGND	K2	V_{IN}
A3	V_{OUT2}	D3	V_{OUT2}	G3	PGND	K3	V_{IN}
A4	PGND	D4	PGND	G4	PGND	K4	V_{IN}
A5	PGND	D5	PGND	G5	PGND	K5	TK/SS2
A6	PGND	D6	PGND	G6	PGND	K6	V_{FB2}
A7	PGND	D7	PGND	G7	PGND	K7	V_{FB1}
A8	PGND	D8	PGND	G8	PGND	K8	TK/SS1
A9	PGND	D9	PGND	G9	PGND	K9	V_{IN}
A10	V_{OUT1}	D10	V_{OUT1}	G10	PGND	K10	V_{IN}
A11	V_{OUT1}	D11	V_{OUT1}	G11	PGND	K11	V_{IN}
A12	V_{OUT1}	D12	V_{OUT1}	G12	PGND	K12	V_{IN}
B1	V_{OUT2}	E1	PGND	H1	PGND	L1	V_{IN}
B2	V_{OUT2}	E2	PGND	H2	PGND	L2	V_{IN}
B3	V_{OUT2}	E3	PGND	H3	SW2	L3	V_{IN}
B4	PGND	E4	PGND	H4	PGND	L4	V_{IN}
B5	PGND	E5	PGND	H5	PGOOD	L5	V_{IN}
B6	PGND	E6	PGND	H6	SGND	L6	COMP2
B7	PGND	E7	PGND	H7	SGND	L7	COMP1
B8	PGND	E8	PGND	H8	MODE/PLLIN	L8	V_{IN}
B9	PGND	E9	PGND	H9	PGND	L9	V_{IN}
B10	V_{OUT1}	E10	PGND	H10	SW1	L10	V_{IN}
B11	V_{OUT1}	E11	PGND	H11	PGND	L11	V_{IN}
B12	V_{OUT1}	E12	PGND	H12	PGND	L12	V_{IN}
C1	V_{OUT2}	F1	PGND	J1	V_{IN}	M1	V_{IN}
C2	V_{OUT2}	F2	PGND	J2	V_{IN}	M2	V_{IN}
C3	V_{OUT2}	F3	PGND	J3	V_{IN}	M3	V_{IN}
C4	PGND	F4	PGND	J4	$EXTV_{CC}$	M4	V_{IN}
C5	PGND	F5	PGND	J5	RUN2	M5	V_{IN}
C6	PGND	F6	$INTV_{CC}$	J6	SGND	M6	V_{IN}
C7	PGND	F7	PGND	J7	SGND	M7	V_{IN}
C8	PGND	F8	PGND	J8	FREQ/PLLFLTR	M8	V_{IN}
C9	PGND	F9	PGND	J9	RUN1	M9	V_{IN}
C10	V_{OUT1}	F10	PGND	J10	V_{IN}	M10	V_{IN}
C11	V_{OUT1}	F11	PGND	J11	V_{IN}	M11	V_{IN}
C12	V_{OUT1}	F12	PGND	J12	V_{IN}	M12	V_{IN}

PACKAGE DESCRIPTION

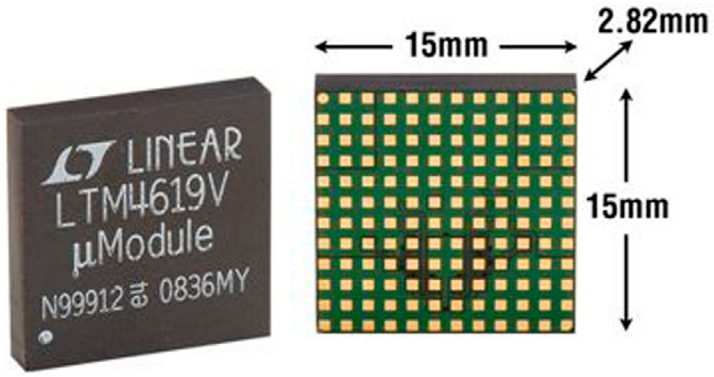


DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.72	2.82	2.92	
b	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 144				

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	08/13	Added “or single 8A” to Description	1
		Changed MODE to MODE/PLLIN	8
		Changed GND to PGND	22
		Added Design Resources	24
C	05/14	Update Order Information Table	2
		Update thermal resistance figures	2, 17
		Update Thermal Considerations Section	14, 15, 16

PACKAGE PHOTOGRAPH



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4614	Dual, 4A, Low V_{IN}, DC/DC µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.82mm LGA
LTM4615	Triple, Low V_{IN}, DC/DC µModule Regulator	Two 4A Outputs and One 1.5A, 15mm × 15mm × 2.82mm LGA
LTM4616	Dual, 8A, Low V_{IN}, DC/DC µModule Regulator	$2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.82mm LGA
LTM4628	Dual, 8A, 26V, DC/DC µModule Regulator	$4.5V \le V_{IN} \le 28.5V$, $0.6V \le V_{OUT} \le 5.5V$, Remote Sense Amplifier, Internal Temperature Sensing Diode Output, 15mm × 15mm × 4.32mm LGA
LTM4620A	Dual, 16V, 13A, 26A, Step-Down µModule Regulator	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 5.3V$, 15mm × 15mm × 4.41mm LGA

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

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