Dual-Voltage µP Supervisory Circuits with Sequenced Reset Outputs

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
$\overline{RESET1}$ (MAX6392), RESET IN2, CSRT, $\overline{MR}$ to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{RESET1}$ (MAX6391), $\overline{RESET2}$, R1, R2 to GND.....-0.3V to +6.0V
Input Current (V_{CC}, GND, CSRT, R1, R2, $\overline{MR}$) .....±20mA
Output Current ($\overline{RESET1}$, $\overline{RESET2}$) .....±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 5.26mW/°C above +70°C).....421mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.2V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Range		T_A = 0°C to +85°C	1.0		5.5	V
		T_A = -40°C to +85°C	1.2		5.5	
Supply Current	I_{CC}	No load		15	25	µA
V_{CC} Reset Threshold	V_{TH1}	MAX639_UA46	4.50	4.63	4.75	V
		MAX639_UA44	4.25	4.38	4.50	
		MAX639_UA31	3.00	3.08	3.15	
		MAX639_UA29	2.85	2.93	3.00	
		MAX639_UA26	2.55	2.63	2.70	
		MAX639_UA23	2.25	2.32	2.38	
		MAX639_UA22	2.12	2.19	2.25	
		MAX639_UA17	1.62	1.67	1.71	
		MAX639_UA16	1.54	1.58	1.61	
RESET IN2 Threshold	V_{TH2}	V_{CC} = 5V	610	625	640	mV
RESET IN2 Input Current					50	nA
V_{CC} to $\overline{RESET1}$ Delay	t_{RD1}	V_{CC} falling at 1mV/µs (Note 2)		20		µs
V_{CC} or RESET IN2 to $\overline{RESET2}$ Delay	t_{RD2}			10		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.2V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RESET1}$ Timeout Period	t_{RP1}			140	200	280	ms
$\overline{RESET2}$ Timeout Period (Note 3)	t_{RP2}	C_{CSRT} = 1500pF		2.2	3.1	4.0	ms
		C_{CSRT} = V_{CC}		140	200	280	
$\overline{RESET}$_ Output Voltage Low	V_{OL}	I_{SINK} = 50µA, reset asserted	V_{CC} ≥ 1.0V, T_A = 0°C to +85°C			0.3	V
			V_{CC} ≥ 1.2V, T_A = -40°C to +85°C			0.3	
		I_{SINK} = 1.2mA, reset asserted, V_{CC} ≥ 2.5V				0.3	
		I_{SINK} = 3.2mA, reset asserted, V_{CC} ≥ 4.25V				0.4	
Open-Drain $\overline{RESET}$ Output Leakage Current	I_{LKG}	V_{CC} ≥ V_{TH1}, $V_{RESET\ IN2}$ ≥ V_{TH2}, reset not asserted				1.0	µA
Push-Pull $\overline{RESET1}$ Output Voltage High (MAX6392 only)	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 500µA, reset not asserted				0.8 x V_{CC}	V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA, reset not asserted					
$\overline{MR}$ Input	V_{IL}	V_{CC} > 4.0V				0.8	V
	V_{IH}			2.4			
	V_{IL}	V_{CC} < 4.0V				0.3 x V_{CC}	
	V_{IH}			0.7 x V_{CC}			
$\overline{MR}$ Minimum Pulse Width				50			µs
$\overline{MR}$ Glitch Rejection					100		ns
$\overline{MR}$ to $\overline{RESET1}$ Delay	t_{MR1}				10		µs
$\overline{MR}$ to $\overline{RESET2}$ Delay	t_{MR2}				100		ns
t_{MR} Skew		t_{MR1} - t_{MR2}			10		µs
$\overline{MR}$ Pullup Resistance		Pullup to V_{CC}		35	47	60	kΩ
Reset Pullup Resistance		$\overline{RESET1}$ to R1 or $\overline{RESET2}$ to R2		35	47	60	kΩ

Note 1: Overtemperature limits are guaranteed by design and not production tested. Devices tested at +25°C only.

Note 2: $\overline{RESET2}$ asserts before $\overline{RESET1}$ when V_{CC} goes below the threshold for all supply voltage and temperature ranges.

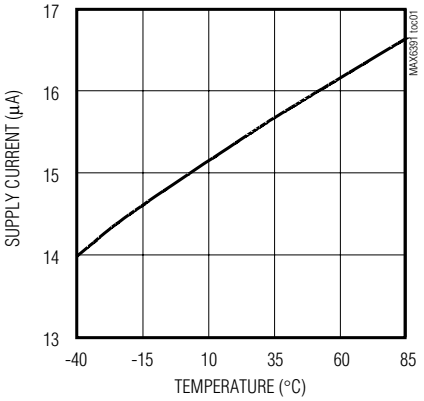
Note 3: CSRT must be connected to either V_{CC} (for fixed $\overline{RESET2}$ timeout period) or an external capacitor (for user-adjustable $\overline{RESET2}$ timeout period).

Dual-Voltage µP Supervisory Circuits with Sequenced Reset Outputs

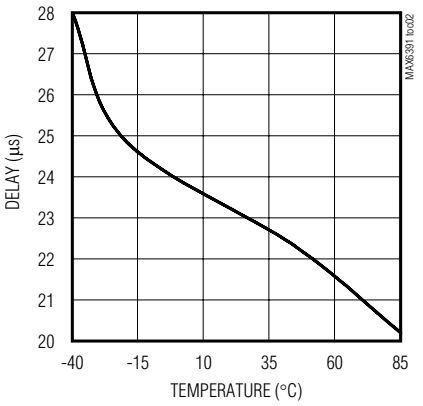
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

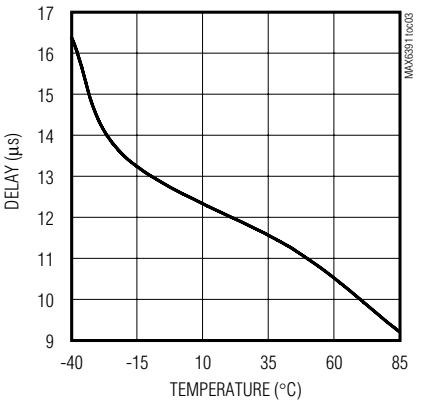
SUPPLY CURRENT vs. TEMPERATURE



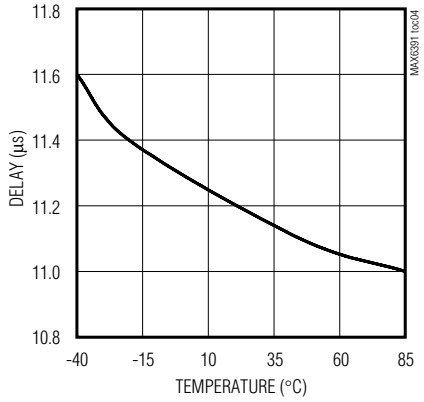
V_{CC} FALLING TO $\overline{RESET1}$ DELAY vs. TEMPERATURE



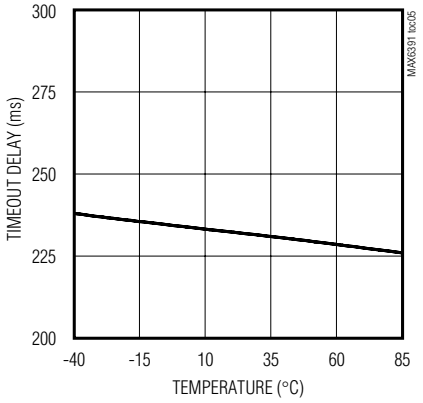
V_{CC} FALLING TO $\overline{RESET2}$ DELAY vs. TEMPERATURE



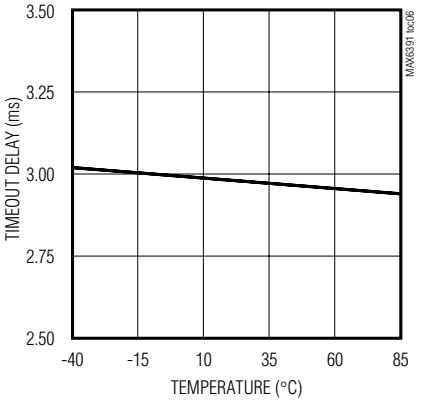
$\overline{RESET2}$ TO $\overline{RESET1}$ DELAY vs. TEMPERATURE



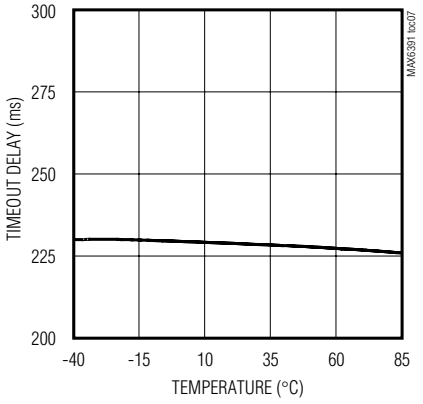
$\overline{RESET1}$ TIMEOUT PERIOD vs. TEMPERATURE



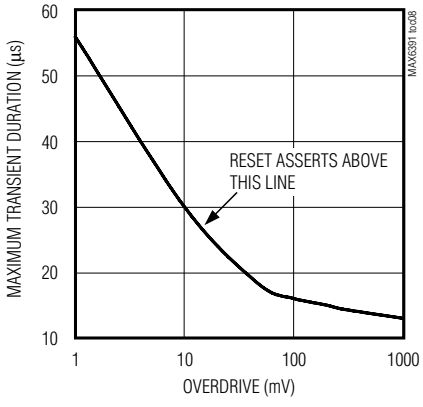
$\overline{RESET1}$ TO $\overline{RESET2}$ TIMEOUT PERIOD vs. TEMPERATURE (CSRT = 1500pF)



$\overline{RESET1}$ TO $\overline{RESET2}$ TIMEOUT PERIOD vs. TEMPERATURE (CSRT TIED TO V_{CC})



MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



Pin Description

PIN		NAME	FUNCTION
MAX6391	MAX6392		
1	1	RESET IN2	Input Voltage for $\overline{RESET2}$ Monitor. High-impedance input for internal reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage.
2	2	V_{CC}	Supply Voltage and Input Voltage for Primary Supply Monitor
3	3	CSRT	$\overline{RESET2}$ Delay Set Capacitor. Connect to V_{CC} for a fixed 140ms (min) timeout period or to an external capacitor for a user-adjustable timeout period after V_{CC} exceeds its minimum threshold.
4	4	GND	Ground
5	5	$\overline{RESET2}$	Secondary Reset Output, Open-Drain, Active-Low. $\overline{RESET2}$ changes from high to low when either V_{CC} or RESET IN2 drop below their thresholds. $\overline{RESET2}$ remains low for a user-adjustable timeout period (see CSRT) or a fixed 140ms (min) after V_{CC} and RESET IN2 meet their minimum thresholds.
6	6	R2	47kΩ Internal Pullup Resistor for $\overline{RESET2}$. Connect to external voltage for $\overline{RESET2}$ high pullup.
7	7	$\overline{RESET1}$	Primary Reset Output, Open-Drain (MAX6391) or Push-Pull (MAX6392), Active-Low. $\overline{RESET1}$ changes from HIGH to LOW when the V_{CC} input drops below the selected reset threshold. $\overline{RESET1}$ remains LOW for the reset timeout period after V_{CC} exceeds the minimum threshold.
8	—	R1	47kΩ Internal Pullup Resistor for $\overline{RESET1}$. Connect to external voltage for $\overline{RESET1}$ high pullup.
—	8	$\overline{MR}$	Manual Reset, Active-Low, Internal 47kΩ Pullup to V_{CC}. Pull LOW to force a reset. $\overline{RESET1}$ and $\overline{RESET2}$ remain asserted as long as $\overline{MR}$ is LOW and for the $\overline{RESET1}$ and $\overline{RESET2}$ timeout periods after $\overline{MR}$ goes HIGH. Leave unconnected or connect to V_{CC} if unused.

Detailed Description

Each device includes a pair of voltage monitors with sequenced reset outputs. The first block monitors V_{CC} only ($\overline{RESET1}$ output is independent of the RESET IN2 monitor). It asserts a reset signal (LOW) whenever V_{CC} is below the preset voltage threshold. $\overline{RESET1}$ remains asserted for at least 140ms after V_{CC} rises above the reset threshold. $\overline{RESET1}$ timing is internally set in each device. V_{CC} voltage thresholds are available from 1.57V to 4.63V. In all cases V_{CC} acts as the master supply (all resets are asserted when V_{CC} goes below its selected threshold). The V_{CC} input also acts as the device power supply.

The second block monitors both RESET IN2 and V_{CC}. It asserts a reset signal (LOW) whenever RESET IN2 is below the 625mV threshold or V_{CC} is below its reset threshold. $\overline{RESET2}$ remains asserted for a fixed 140ms (min) or a user-adjustable time period after RESET IN2 rises above the 625mV reset threshold and $\overline{RESET1}$ is deasserted. Resets are guaranteed valid for V_{CC} down to 1V.

The timing diagram in Figure 2 shows the reset timing characteristics of the MAX6391/MAX6392. As shown in Figure 2, $\overline{RESET1}$ deasserts 140ms (min) (t_{RP1}) after V_{CC} exceeds the reset threshold. $\overline{RESET2}$ deasserts t_{RP2} (140ms minimum or a user-adjustable timeout period) after RESET IN2 exceeds 625mV and $\overline{RESET1}$ is deasserted. When RESET IN2 drops below 625mV while V_{CC} is above the reset threshold, $\overline{RESET2}$ asserts within 10µs typ. $\overline{RESET1}$ is unaffected when this happens. When V_{CC} falls below V_{TH1}, $\overline{RESET2}$ always asserts before $\overline{RESET1}$ ($t_{RD2} < t_{RD1}$).

Dual-Voltage µP Supervisory Circuits with Sequenced Reset Outputs

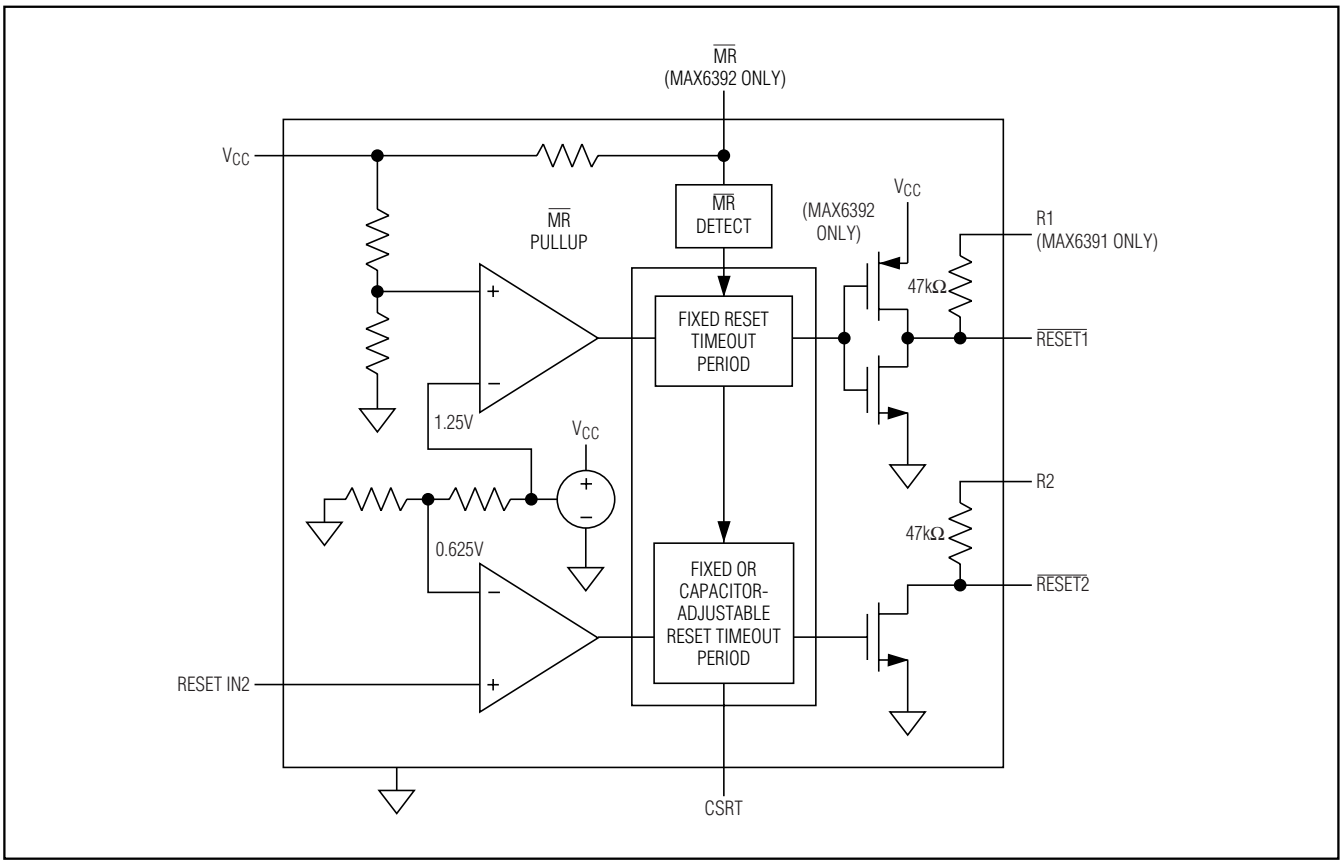


Figure 1. Functional Diagram

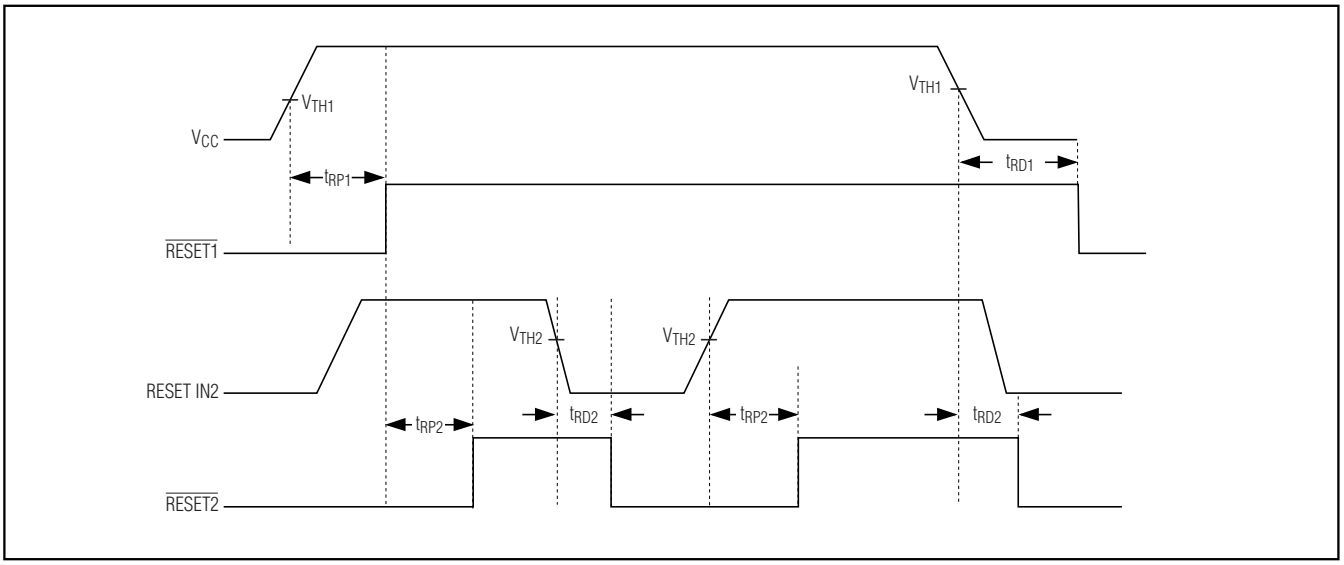


Figure 2. Timing Diagram

Dual-Voltage µP Supervisory Circuits with Sequenced Reset Outputs

Selector Guide

PART NUMBER	NOMINAL THRESHOLD (V)	TOP MARK
MAX6391KA**46**	4.63	AAHJ
MAX6391KA44	4.38	AAHK
MAX6391KA31	3.08	AAHL
MAX6391KA**29**	2.93	AAHM
MAX6391KA26	2.63	AAHN
MAX6391KA**23**	2.32	AAHO
MAX6391KA22	2.19	AAHP
MAX6391KA17	1.67	AAHQ
MAX6391KA**16**	1.58	AAHR
MAX6392KA**46**	4.63	AAHS
MAX6392KA44	4.38	AAHT
MAX6392KA31	3.08	AAHU
MAX6392KA**29**	2.93	AAHV
MAX6392KA26	2.63	AAHW
MAX6392KA**23**	2.32	AAHX
MAX6392KA22	2.19	AAHY
MAX6392KA17	1.67	AAHZ
MAX6392KA**16**	1.58	AAIA

Standard versions in bold face. Samples are typically available for standard versions. Contact factory for availability.

Applications Information

Selecting the Reset Timeout Capacitor

The $\overline{RESET2}$ delay may be adjusted by the user with an external capacitor connected from the CSRT pin to ground. The MAX6391 includes a 600nA current source that is switched to C_{CSRT} to create a voltage ramp. The voltage ramp is compared to the internal 1.25V reference to set the $\overline{RESET2}$ delay period. The period is calculated by:

$$\Delta t = C \times \Delta V / I$$

where ΔV = 1.25V, I = 600nA, and C is the external capacitor.

Simplifying,

$$t_{RP} = 2.08 \times 10^6 \text{ s} / F \times C_{CSRT}$$

$$\text{For } C_{CSRT} = 1500pF,\ t_{RP} = 3.1ms$$

A fixed internal 140ms (min) reset delay time for $\overline{RESET2}$ may be chosen by connecting the CSRT pin to V_{CC}. The V_{CC} to CSRT connection disables the voltage ramp and enables a separate fixed delay counter chain. The MAX6391 internally determines the CSRT connection and provides the proper timing setup.

In all cases, RESET IN2 acts as the slave supply. V_{CC} can assert the $\overline{RESET2}$ output but RESET IN2 will have no effect on the $\overline{RESET1}$ output.

Monitoring Voltages Other Than V_{CC}

An external resistive-divider network is required at RESET IN2 for most applications. The divider resistors, R3 and R4, may be calculated by the following formula:

$$V_{RST} = V_{TH2} \times (R3 + R4)/R4$$

where V_{TH2} = 625mV (internal reference voltage) and V_{RST} is the desired reset threshold voltage. R4 may be set to a conveniently high value (500kΩ for example, to minimize current consumption) and the equation may be solved for R3 by:

$$R3 = R4 \times (V_{RST}/V_{TH2} - 1)$$

For single-supply operations requiring two reset outputs ($\overline{RESET1}$ before $\overline{RESET2}$), connect RESET IN2 directly to V_{CC} and adjust $\overline{RESET2}$ timeout delay with C_{CRST} as desired.

Pullup Resistors

The MAX6391 includes open-drain outputs for both $\overline{RESET1}$ and $\overline{RESET2}$. Two internal resistors, R1 and R2, of 47kΩ each are provided with internal connections to $\overline{RESET1}$ and $\overline{RESET2}$. These resistors may be connected to the appropriate external voltage for independent V_{OH} drive with no additional component requirements.

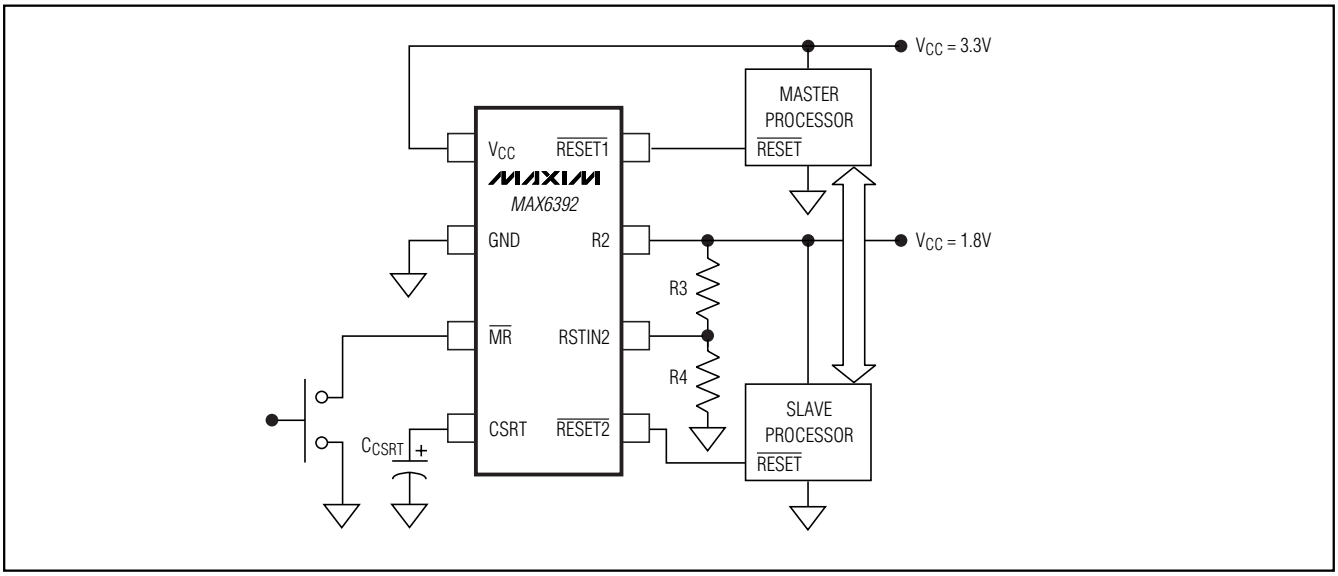
The MAX6392 includes a manual reset option, $\overline{MR}$, that replaces the R1 pullup resistor. The active-low manual reset input forces both $\overline{RESET1}$ and $\overline{RESET2}$ low. $\overline{RESET2}$ is driven active before $\overline{RESET1}$ in all cases (10µs typ). The resets follow standard reset timing specifications after the manual reset is released. The manual reset is internally pulled up to V_{CC} through a 47kΩ resistor.

Negative-Going V_{CC} Transients

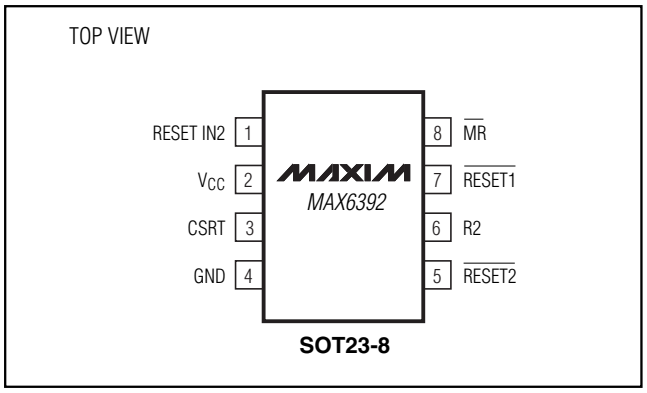
In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these devices are relatively immune to short-duration, negative-going V_{CC} or RESET IN2 transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Comparator Overdrive graph. The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without issuing a reset signal. As the amplitude of the transient increases, the maximum allowable pulse width decreases.

Dual-Voltage µP Supervisory Circuits with Sequenced Reset Outputs

Typical Operating Circuit



Pin Configurations (continued)



Chip Information

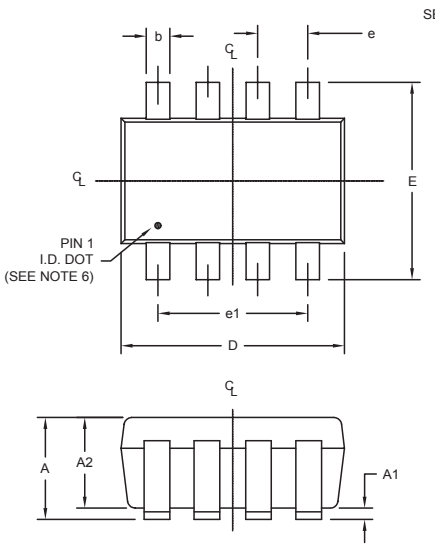
TRANSISTOR COUNT: 810

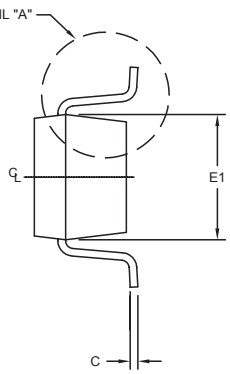
PROCESS: BiCMOS

Package Information

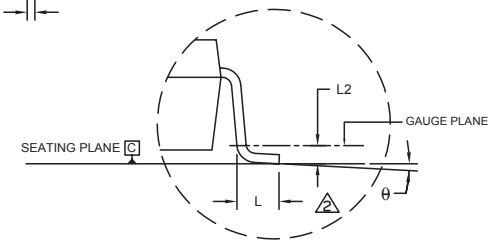
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0∞	8∞



DETAIL "A"

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ÿ MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	D	1/1

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX6392KA46+T MAX6391KA16+T MAX6391KA17+T MAX6391KA22+T MAX6391KA23+T MAX6391KA26+T MAX6391KA29+T MAX6391KA31+T MAX6391KA44+T MAX6391KA46+T MAX6392KA16+T MAX6392KA17+T MAX6392KA22+T MAX6392KA23+T MAX6392KA26+T MAX6392KA29+T MAX6392KA31+T MAX6392KA44+T