Absolute Maximum Ratings

V_{CC} ..... -0.3V to +6.0V
Open-Drain $\overline{RESET}$, $\overline{WDO}$, $\overline{PFO}$ ..... -0.3V to +6.0V
Push-Pull RESET, $\overline{RESET}$, $\overline{WDO}$, $\overline{PFO}$ ... -0.3V to (V_{CC} + 0.3V)
$\overline{MR}$, WDI, PFI, RST_IN1, RST_IN2 ..... -0.3V to (V_{CC} + 0.3V)
Input Current (V_{CC}) 20mA
Output Current ($\overline{O}$, $\overline{WDO}$) 20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C) 714mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +4.25V to +5.5V for L/M versions, V_{CC} = +2.55V to +3.6V for the T/S/R versions, V_{CC} = +2.1V to +2.75V for the Z/Y versions. T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	T_A = 0°C to +125°C		1.0		5.5	V
		T_A = -40°C to +125°C		1.2		5.5	
Supply Current $\overline{MR}$ Unconnected	I_{CC}	V_{CC} < 5.5V, no load			12	25	µA
		V_{CC} < 3.6V, no load			9	20	
		V_{CC} < 3.6V, no load (MAX6708 only)			6	20	
V_{CC} Reset Threshold (V_{CC} falling)	V_{TH}	MAX670_L/MAX670_AL	T_A = -40°C to +85°C	4.50	4.63	4.75	V
			T_A = -40°C to +125°C	4.47		4.78	
		MAX670_M/MAX670_AM	T_A = -40°C to +85°C	4.25	4.38	4.50	
			T_A = -40°C to +125°C	4.22		4.53	
		MAX670_T/MAX670_AT	T_A = -40°C to +85°C	3.00	3.08	3.15	
			T_A = -40°C to +125°C	2.97		3.17	
		MAX670_S/MAX670_AS	T_A = -40°C to +85°C	2.85	2.93	3.00	
			T_A = -40°C to +125°C	2.83		3.02	
		MAX670_R/MAX670_AR	T_A = -40°C to +85°C	2.55	2.63	2.70	
			T_A = -40°C to +125°C	2.53		2.72	
		MAX670_Z/MAX670_AZ	T_A = -40°C to +85°C	2.25	2.32	2.38	
			T_A = -40°C to +125°C	2.24		2.40	
		MAX670_Y/MAX670_AY	T_A = -40°C to +85°C	2.12	2.19	2.25	
			T_A = -40°C to +125°C	2.11		2.27	
Reset Threshold Temperature Coefficient	ΔV_{TH}				60		ppm/°C
V_{CC} to Reset Output Delay		V_{CC} falling at 10mV/µs			12		µs
Reset Timeout Period	t_{RP}		T_A = -40°C to +85°C	140	200	280	ms
			T_A = -40°C to +125°C	120		300	
V_{CC} Falling to $\overline{WDO}$ Delay		MAX6701(A)/MAX6702(A)/MAX6703(A)/MAX6705(A)/ MAX6706(A)/MAX6707(A)			5		µs
PFI, RST_IN1, RST_IN2 Threshold		V_{CC} = 1.8V to 5.5V	T_A = -40°C to +85°C	602	618	634	mV
			T_A = -40°C to +125°C	593		642	
PFI Hysteresis					6		mV

Electrical Characteristics (continued)

(V_{CC} = +4.25V to +5.5V for L/M versions, V_{CC} = +2.55V to +3.6V for the T/S/R versions, V_{CC} = +2.1V to +2.75V for the Z/Y versions. T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

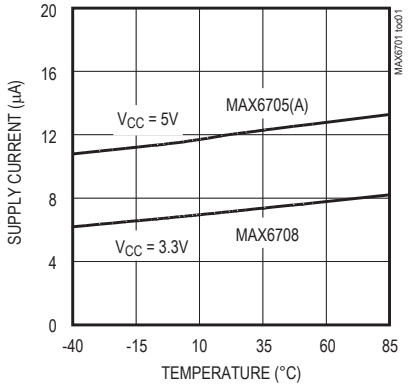
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PFI, RST_IN1, RST_IN2 Leakage Current		(Note 2)	T_A = -40°C to +85°C	-50		+50	nA
			T_A = -40°C to +125°C	-200		+200	
PFI to $\overline{PFO}$ Delay	t_{PF}				1		µs
$\overline{MR}$ Input Voltage	V_{IL}					0.3 x V_{CC}	V
	V_{IH}			0.7 x V_{CC}			
$\overline{MR}$ Minimum Input Pulse				1			µs
$\overline{MR}$ Glitch Rejection					100		ns
$\overline{MR}$ to Reset Delay	t_{MD}				200		ns
V_{CC} Rising to $\overline{WDO}$ Delay		MAX6701(A)/MAX6702(A)/MAX6703(A)/ MAX6705(A)/MAX6706(A)/MAX6707(A)			100		ns
$\overline{MR}$ Pullup Resistance				25	50	75	kΩ
Watchdog Timeout Period	t_{WD}	T_A = -40°C to +85°C		1.12	1.6	2.4	s
		T_A = -40°C to +125°C		0.96		2.52	
WDI Pulse Width	t_{WDI}	(Note 2)		50			ns
WDI Input Voltage	V_{IL}					0.3 x V_{CC}	V
	V_{IH}			0.7 x V_{CC}			
WDI Input Current	I_{WDI}	V_{WDI} = 0V or V_{CC}		-1		+1	µA
RESET, WDO Output Low (Push-Pull or Open Drain)	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50µA, output asserted (T_A = 0°C to +125°C)				0.3	V
		V_{CC} ≥ 1.2V, I_{SINK} = 100µA, output asserted				0.3	
		V_{CC} ≥ 2.55V, I_{SINK} = 1.2mA, output asserted				0.3	
		V_{CC} ≥ 4.25V, I_{SINK} = 3.2mA, output asserted				0.4	
PFO Output Low (Push-Pull or Open Drain)	V_{OL}	V_{CC} ≥ 1.80V, I_{SINK} = 200µA, output asserted				0.3	V
		V_{CC} ≥ 2.55V, I_{SINK} = 1.2mA, output asserted				0.3	
		V_{CC} ≥ 4.25V, I_{SINK} = 3.2mA, output asserted				0.4	
$\overline{RESET}$, $\overline{WDO}$, $\overline{PFO}$ Output High (Push-Pull Only)	V_{OH}	V_{CC} ≥ 2.7V, I_{SOURCE} = 500µA, output not asserted		0.8 x V_{CC}			V
		V_{CC} ≥ 4.75V, I_{SOURCE} = 800µA, output not asserted		0.8 x V_{CC}			
$\overline{RESET}$, $\overline{WDO}$, $\overline{PFO}$ Output Open-Drain Leakage Current	I_{LKG}	V_{CC} > V_{TH}, output not asserted				1.0	µA
RESET Output High (Push-Pull Only)	V_{OH}	V_{CC} ≥ 1.0V, I_{SOURCE} = 1µA, reset asserted (T_A = 0°C to +125°C)		0.8 x V_{CC}			V
		V_{CC} ≥ 1.2V, I_{SOURCE} = 50µA, reset asserted		0.8 x V_{CC}			
		V_{CC} ≥ 2.55V, I_{SOURCE} = 500µA, reset asserted		0.8 x V_{CC}			
		V_{CC} ≥ 4.25V, I_{SOURCE} = 800µA, reset asserted		0.8 x V_{CC}			
RESET Output Low (Push-Pull Only)	V_{OL}	V_{CC} ≥ 2.7V, I_{SINK} = 1.2mA, reset not asserted				0.3	V
		V_{CC} ≥ 4.75V, I_{SINK} = 3.2mA, reset not asserted				0.4	

Note 1: Over-temperature limits are guaranteed by design and not production tested. Devices are tested at T_A = +25°C.
Note 2: Guaranteed by design. Not production tested.

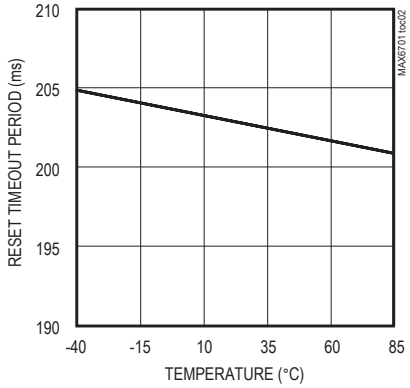
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

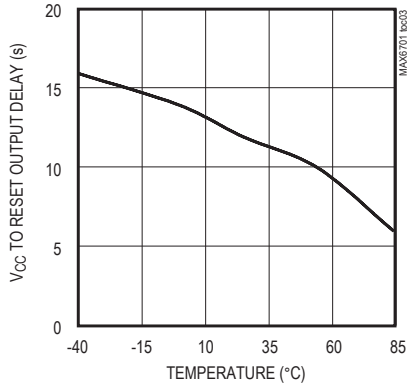
SUPPLY CURRENT vs. TEMPERATURE



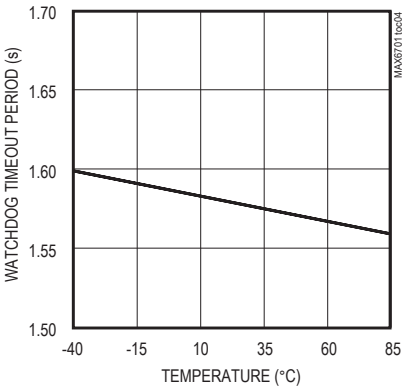
RESET TIMEOUT PERIOD vs. TEMPERATURE



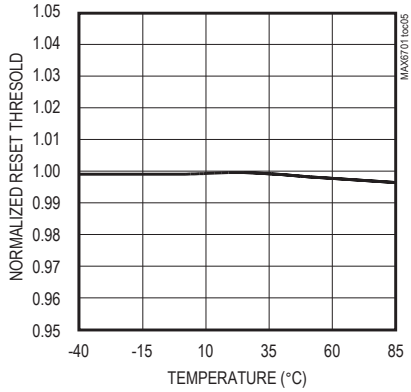
VCC TO RESET OUTPUT DELAY vs. TEMPERATURE



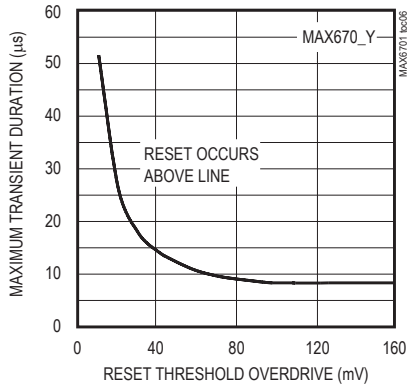
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



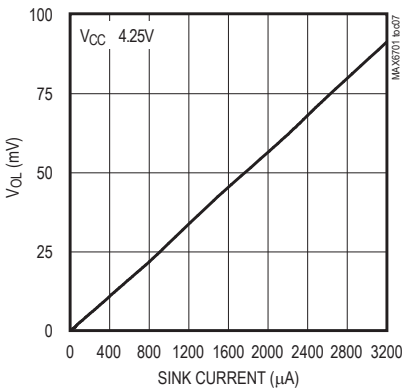
NORMALIZED RESET THRESHOLD vs. TEMPERATURE



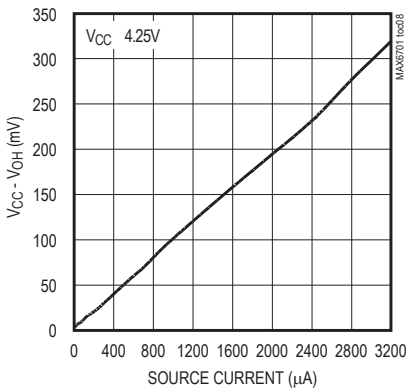
MAXIMUM VCC TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



OUTPUT-VOLTAGE LOW vs. SINK CURRENT



VCC - VOH vs. SOURCE CURRENT



Pin Description

PIN				NAME	FUNCTION
MAX6701(A) MAX6702(A) MAX6703(A)	MAX6704	MAX6705(A) MAX6706(A) MAX6707(A)	MAX6708		
1	1	1	1	$\overline{MR}$	Active-Low, Manual Reset Input, Internal 50kΩ Pullup to V_{CC}. Pull low to force a reset. Reset remains active as long as $\overline{MR}$ is low and the reset timeout period after $\overline{MR}$ goes high. Leave unconnected or connect to V_{CC} if unused. $\overline{WDO}$ deasserts when $\overline{MR}$ is low (MAX6701(A)/ MAX6702(A)/MAX6703(A)/ MAX6705(A)/ MAX6706(A)/ MAX6707(A) only)
2	2	2	2	V_{CC}	Supply Voltage for MAX6701–MAX6708 and Input for Primary Reset Threshold Monitor. Push-pull outputs are powered by V_{CC}.
3	3	3	3	GND	Ground
—	4	4	4	PFI	Power-Fail Voltage Monitor Input. High-impedance input for internal power-fail comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; 0.62V (typ) threshold. Connect to GND or V_{CC} when not used.
—	5	5	5	$\overline{PFO}$	Power-Fail Monitor Output. Open drain or push-pull active low. $\overline{PFO}$ goes low when PFI is less than 0.62V.
6	6	6	—	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and $\overline{WDO}$ is asserted. $\overline{WDO}$ is asserted low after each watchdog overflow and remains low until the watchdog timer is cleared (the reset output is not affected). The internal watchdog timer clears whenever a V_{CC}/RST_IN1/RST_IN2 reset is asserted, the manual reset is asserted, or WDI sees a rising or falling edge. The watchdog timer remains cleared until the reset output is deasserted. On the MAX6704, $\overline{RESET}$ pulse asserts for the reset timeout period after each watchdog timeout overflow. The watchdog timer cannot be disabled.
—	—	—	6	N.C.	No Connection. Not internally connected.
7	7	7	7	$\overline{RESET}$	Active-Low Reset Output (Open Drain or Push-Pull). $\overline{RESET}$ changes from high to low when the V_{CC} input drops below the selected reset threshold (or RST_IN1/ RST_IN2 for the MAX6701(A)/MAX6702(A)/MAX6703(A), $\overline{MR}$ is pulled low, or the watchdog triggers a reset (MAX6704 only). $\overline{RESET}$ remains low for the reset timeout period after the reset conditions are terminated.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX6701(A) MAX6702(A) MAX6703(A)	MAX6704	MAX6705(A) MAX6706(A) MAX6707(A)	MAX6708		
8	—	8	—	$\overline{WDO}$	Active-Low Watchdog Output (Open Drain or Push-Pull). $\overline{WDO}$ is asserted whenever the watchdog times out and V_{CC} or the reset inputs are below their respective thresholds. $\overline{WDO}$ deasserts after a valid WDI transition without a reset timeout period. In the A versions, $\overline{WDO}$ deasserts without a timeout delay when V_{CC}, RST_IN1, and RST_IN2 rises above its threshold. Pull $\overline{MR}$ low to assert $\overline{WDO}$ (MAX6701/MAX6702/MAX6703/MAX6705/MAX6706/MAX6707 only). Pull $\overline{MR}$ low to deassert $\overline{WDO}$ (MAX6701(A)/MAX6702(A) / MAX6703(A)/ MAX6705(A)/MAX6706(A)MAX6707(A) only)
7*	8	7*	8	RESET	Active-High Reset Output (Push-Pull). RESET changes from low to high when the V_{CC} input drops below the selected reset threshold (or RST_IN1/RST_IN2 for MAX6701(A)/MAX6702(A)/ MAX6703(A), $\overline{MR}$ is pulled low, or the watchdog triggers a reset (MAX6704 only). RESET remains high for the reset timeout period after the reset conditions are terminated.
4	—	—	—	RST_IN1	Input for User-Adjustable V_{CC2} Monitor. High-impedance input for second internal reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; 0.62V (typ) threshold. Connect to V_{CC} when not used. Reset is asserted when either V_{CC}, RST_IN1, or RST_IN2 are below threshold.
5	—	—	—	RST_IN2	Input for User-Adjustable V_{CC3} Monitor. High-impedance input for third internal reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; 0.62V (typ) threshold. Connect to V_{CC} when not used. Reset is asserted when either V_{CC}, RST_IN1, or RST_IN2 are below threshold.

**RESET active-high for the MAX6702(A)/MAX6706(A).*

Detailed Description

Figures 1, 2, and 3 are functional diagrams for the MAX6705(A)/MAX6706(A)/MAX6707(A), MAX6704/MAX6708, and MAX6701(A)/MAX6702(A)/MAX6703(A), respectively.

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. The MAX6701–MAX6708 assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic-low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. After V_{CC}, RST_IN1, or RST_IN2 rise above the reset threshold, an internal timer holds $\overline{RESET}$ low for about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} dips below the reset threshold, including brownout conditions. If a brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less, until V_{CC} drops below 1V.

The MAX6702(A)/MAX6704/MAX6706(A)/MAX6708 active-high RESET output is the complement of the $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1V.

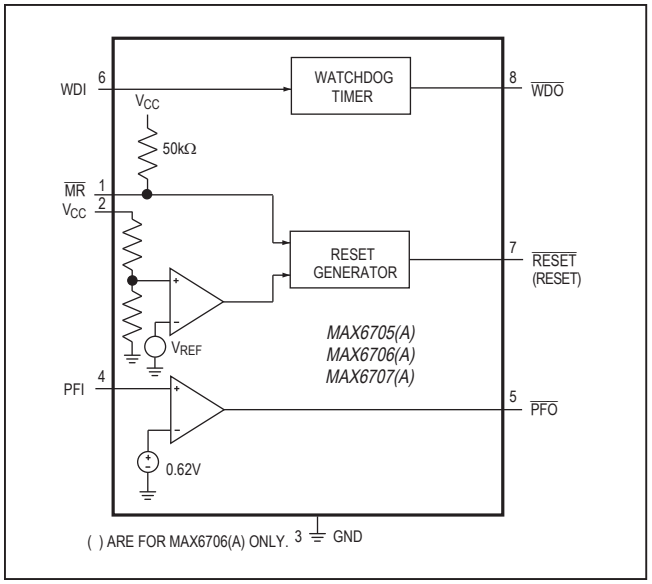


Figure 1. MAX6705(A)/MAX6706(A)/MAX6707(A) Functional Diagram

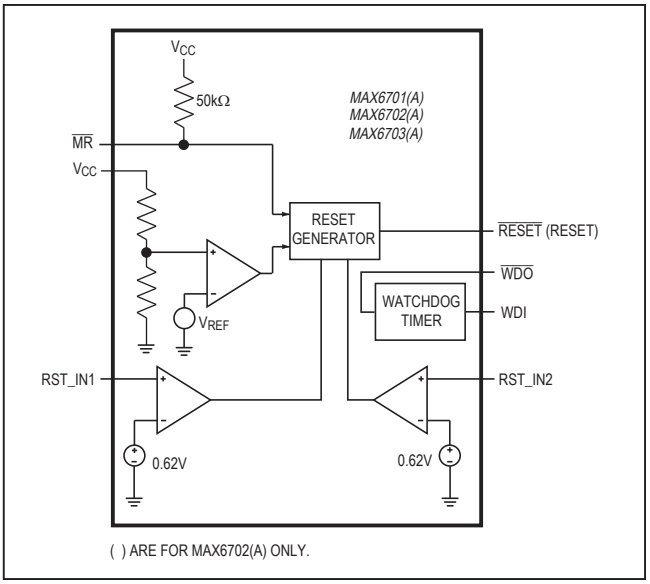


Figure 3. MAX6701(A)/MAX6702(A)/MAX6703(A) Functional Diagram

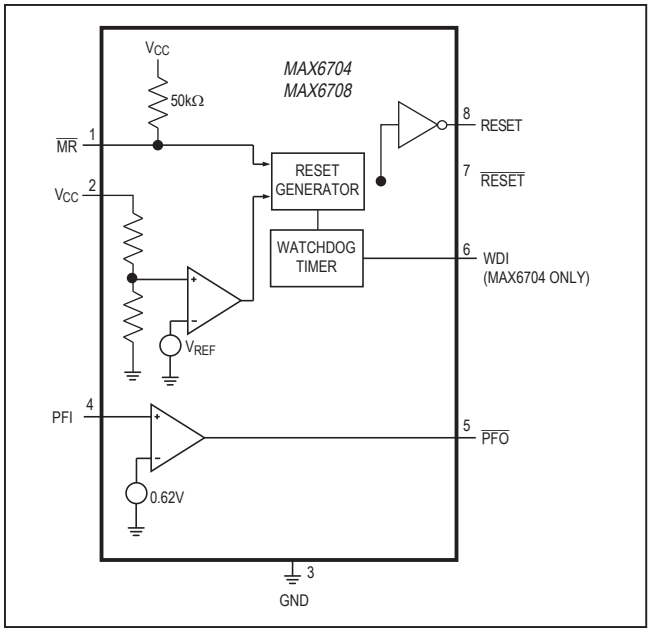


Figure 2. MAX6704/MAX6708 Functional Diagram

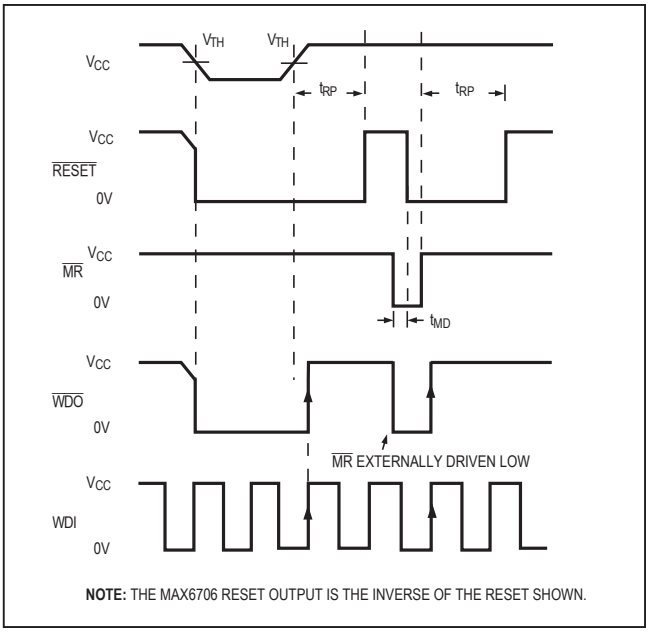


Figure 4. MAX6705/MAX6706/MAX6707 RESET, MR, WDO, and WDI Timing

Standard- vs. A-Version Comparison

The MAX6701/MAX6702/MAX6703/MAX6705/MAX6706/MAX6707s' $\overline{WDO}$ latches low when one of the following events occurs:

- The watchdog timer times out (1.6s, typ).
- V_{CC}, RST_IN1, or RST_IN2 is below its reset threshold.
- $\overline{MR}$ is pulled low.
- $\overline{WDO}$ only deasserts with a valid WDI transition.

The MAX6701(A)/MAX6702(A)/MAX6703(A)/MAX6705(A)/MAX6706(A)/ MAX6707(A)s' $\overline{WDO}$ asserts when either V_{CC}, RST_IN1, or RST_IN2 is below its reset threshold. $\overline{WDO}$ deasserts without a timeout delay when the undervoltage situation has expired. $\overline{WDO}$ is latched low when the watchdog timer elapses without seeing a WDI transition. $\overline{WDO}$ deasserts with a valid WDI transition OR by pulling $\overline{MR}$ low.

See Figures 4 and 5 for standard-version timing. See Figures 6 and 7 for A-version timing.

Watchdog Timer

The MAX6701–MAX6707 watchdog circuit monitors the µP's activity. If the µP does not toggle the WDI within 1.6s, $\overline{WDO}$ goes low. When $\overline{RESET}$ is asserted, the watchdog timer stays cleared and does not count. As soon as reset is released, the timer starts counting. $\overline{WDO}$ deasserts after a valid transition is detected at WDI. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ is connected to the NMI input of a µP. When V_{CC}, RST_IN1, or RST_IN2 drop below the reset threshold, $\overline{WDO}$ goes low whether or not the watchdog timer has timed out. Normally this would trigger an NMI, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI.

The MAX6704 watchdog circuit does not have an independent watchdog output ($\overline{WDO}$). If the µP does not toggle the watchdog input within 1.6s, the MAX6704 asserts a reset output pulse for the reset timeout period.

Manual Reset

The manual reset input ($\overline{MR}$) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the reset pulse width. $\overline{MR}$ is CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in the MAX6701(A)/MAX6702(A)/MAX6703(A)/MAX6705(A)/MAX6706(A)/MAX6707(A) by connecting $\overline{WDO}$ to $\overline{MR}$.

Power-Fail Comparator

The uncommitted power-fail comparator can be used for various purposes because its noninverting input and output are externally available. The inverting input is internally connected to a 0.62V reference. To build an early warning circuit for power failure, connect the PFI pin to a voltage-divider (see the *Typical Operating Circuit*). Choose the voltage-divider ratio so that the voltage at PFI falls below 0.62V just before the regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down. The low-input current at this pin allows for large resistor values in the divider.

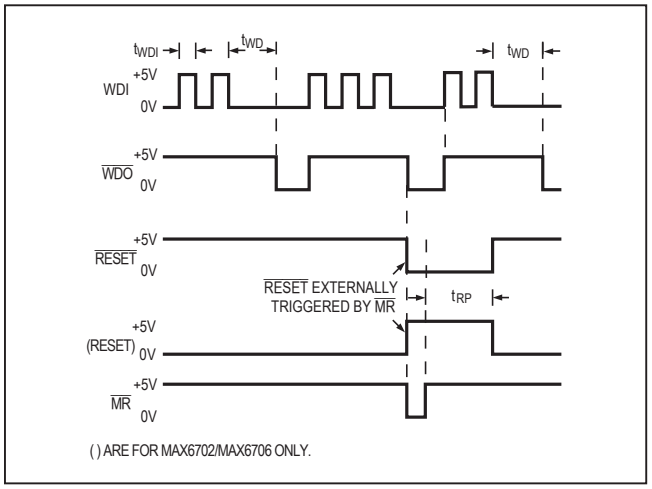


Figure 5. MAX6701/MAX6702/MAX6703/MAX6705/MAX6706/MAX6707 Watchdog

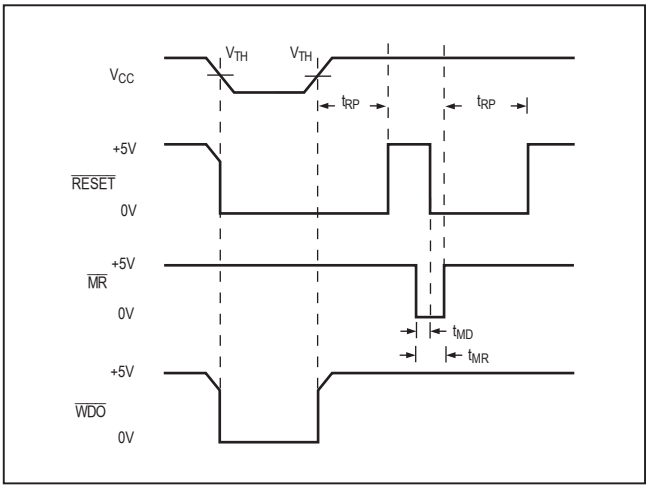


Figure 6. MAX6701(A)/MAX6702(A)/MAX6703(A)/MAX6705(A)/ MAX6706(A)/MAX6707(A) RESET, MR, and WDO Timing with WDI Three-Stated

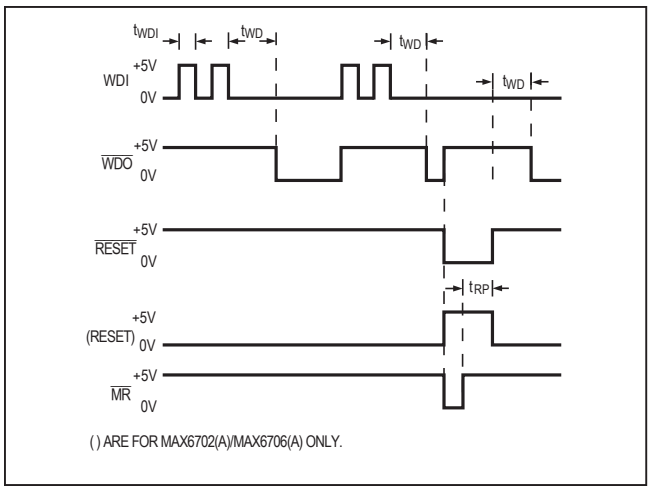


Figure 7. MAX6701(A)/MAX6702(A)/MAX6703(A)/ MAX6705(A)/ MAX6706(A)/MAX6707(A) Watchdog Timing

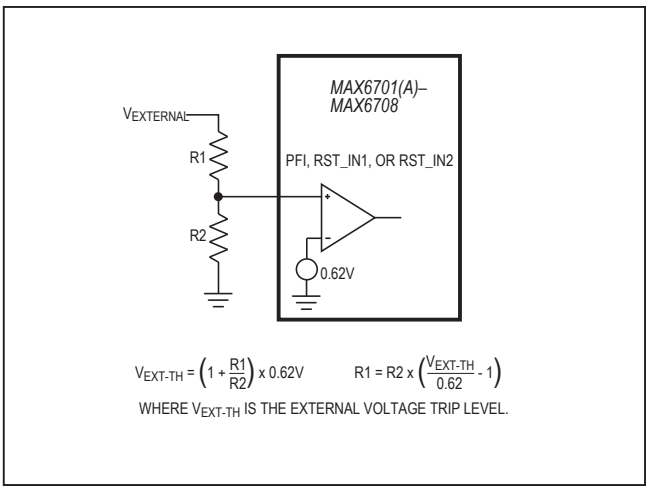


Figure 8. Calculating Adjustable Voltage Thresholds

Reset Input

The MAX6701(A)/MAX6702(A)/MAX6703(A) include two adjustable reset inputs for monitoring up to a total of three system voltages (including V_{CC}). The thresholds for the monitored RST_IN supplies are externally set with resistor-divider networks (Figure 8). The reset output is asserted if any of the monitored supplies (V_{CC}, RST_IN1, or RST_IN2) go below its specified threshold and remains asserted for the reset timeout period after all supplies are above their thresholds.

Applications Information

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC} = 0

When V_{CC} falls below 1V, the MAX6701–MAX6708 $\overline{\text{RESET}}$ output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{\text{RESET}}$ pin, as shown in Figure 9, any stray charge or leakage currents are drained to ground, holding $\overline{\text{RESET}}$ low. A resistor value (R1) is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground. This application works for push-pull output only (not for open-drain resets).

Monitoring Other System Voltages

Other systems can be monitored by connecting a voltage-divider to PFI and adjusting the ratio appropriately. In noisy systems, a capacitor between PFI and GND reduces the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. Reset can be asserted on other voltages in addition to the V_{CC} supply line. Connect $\overline{\text{PFO}}$ to $\overline{\text{MR}}$ to initiate a reset output pulse when PFI drops below 0.62V. Figure 10 shows the MAX6704–MAX6708 configured to assert a reset output when the secondary supply falls below the reset threshold.

Generating a Reset from Watchdog Overflow

Connect $\overline{\text{WDO}}$ to $\overline{\text{MR}}$ to force a watchdog timeout to generate a reset pulse for only the reset timeout period on the MAX6701(A)/MAX6702(A)/MAX6703(A)/MAX6705(A)/ MAX6706(A)/MAX6707(A). When the MAX6704 watchdog times out, reset outputs are automatically asserted (no external connections required). For the MAX6701/ MAX6702/MAX6703/MAX6705/MAX6706/MAX6707 non-A versions, do not connect $\overline{\text{WDO}}$ to $\overline{\text{MR}}$; this creates a locked condition.

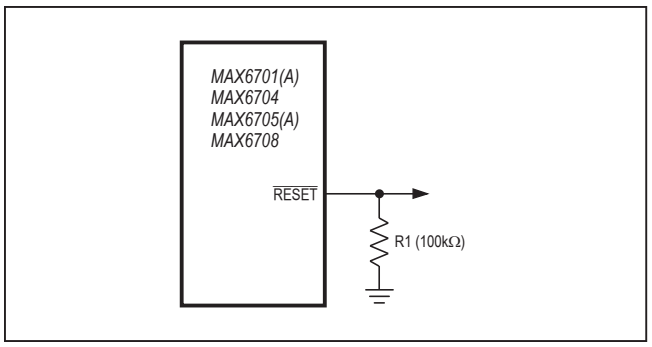


Figure 9. $\overline{RESET}$ Valid to Ground Circuit

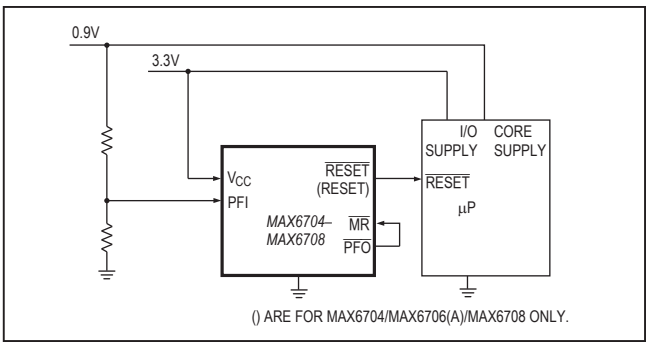


Figure 10. Monitoring Other System Voltages

Selector Guide

PART	$\overline{RESET}$ PP LOW	RESET PP HIGH	$\overline{RESET}$ OD-LOW	WDI	$\overline{WDO}$	PFI, $\overline{PFO}$	RST_IN1, RST_IN2
MAX6701	✔	—	—	✔	✔ PP	—	✔
MAX6701A*	✔	—	—	✔	✔ PP	—	✔
MAX6702	—	✔	—	✔	✔ PP	—	✔
MAX6702A*	—	✔	—	✔	✔ PP	—	✔
MAX6703	—	—	✔	✔	✔ OD	—	✔
MAX6703A*	—	—	✔	✔	✔ OD	—	✔
MAX6704	✔	✔	—	✔	—	✔ PP	—
MAX6705	✔	—	—	✔	✔ PP	✔ PP	—
MAX6705A*	✔	—	—	✔	✔ PP	✔ PP	—
MAX6706	—	✔	—	✔	✔ PP	✔ PP	—
MAX6706A*	—	✔	—	✔	✔ PP	✔ PP	—
MAX6707	—	—	✔	✔	✔ OD	✔ OD	—
MAX6707A*	—	—	✔	✔	✔ OD	✔ OD	—
MAX6708	✔	✔	—	—	—	✔ PP	—

PP = push-pull, OD = open drain.

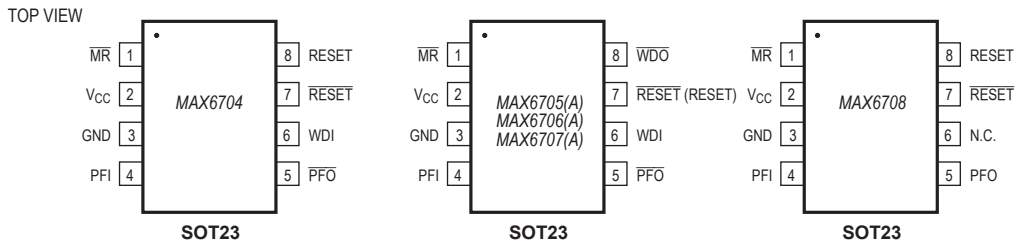
**WDO deasserts when MR is pulled low. See the Standard- vs. A-Version Comparison section for the differences on WDO.*

Threshold Suffix Guide

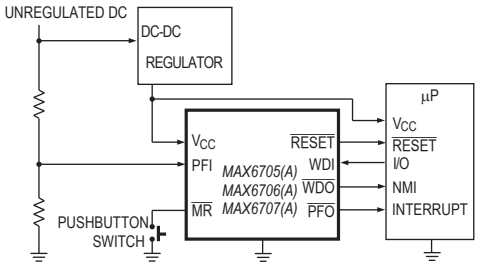
SUFFIX	RESET THRESHOLD (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63
Z	2.32
Y	2.19

Bold indicates standard version.

Pin Configurations (continued)



Typical Operating Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOT23	K8+2	21-0078	90-0176

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX6702_ KA-T	-40°C to +125°C	8 SOT23
MAX6702A_ KA-T	-40°C to +125°C	8 SOT23
MAX6703_ KA-T	-40°C to +125°C	8 SOT23
MAX6703A_ KA-T	-40°C to +125°C	8 SOT23
MAX6704_KA-T	-40°C to +125°C	8 SOT23
MAX6705_KA-T	-40°C to +125°C	8 SOT23
MAX6705A_KA-T	-40°C to +125°C	8 SOT23
MAX6706_KA-T	-40°C to +125°C	8 SOT23
MAX6706A_KA-T	-40°C to +125°C	8 SOT23
MAX6707_KA-T	-40°C to +125°C	8 SOT23
MAX6707A_KA-T	-40°C to +125°C	8 SOT23
MAX6708_KA-T	-40°C to +125°C	8 SOT23

Insert the desired suffix letter (from the Threshold Suffix Guide table) into the blank to complete the part number. All devices must be ordered in increments of 2500 pieces. Sample stock is typically held on standard versions only. Contact factory for availability.

Devices are available in both leaded and lead(Pb)-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

T = Tape and reel.

Chip Information

TRANSISTOR COUNT: 716

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	5/14	No /V OPNs; removed Automotive reference from *Applications* section	1

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX6702ALKA+T MAX6702AMKA+T MAX6702ARKA+T MAX6702ASKA+T MAX6702ATKA+T MAX6702AYKA+T MAX6702AZKA+T MAX6702LKA+T MAX6702MKA+T MAX6702RKA+T MAX6702SKA+T MAX6702TKA+T MAX6702YKA+T MAX6702ZKA+T MAX6703ARKA+T MAX6703AYKA+T MAX6704LKA+T MAX6704MKA+T MAX6704RKA+T MAX6704SKA+T MAX6704TKA+T MAX6704YKA+T MAX6704ZKA+T MAX6706ALKA+T MAX6706AMKA+T MAX6706ARKA+T MAX6706ASKA+T MAX6706ATKA+T MAX6706AYKA+T MAX6706AZKA+T MAX6703ASKA-T