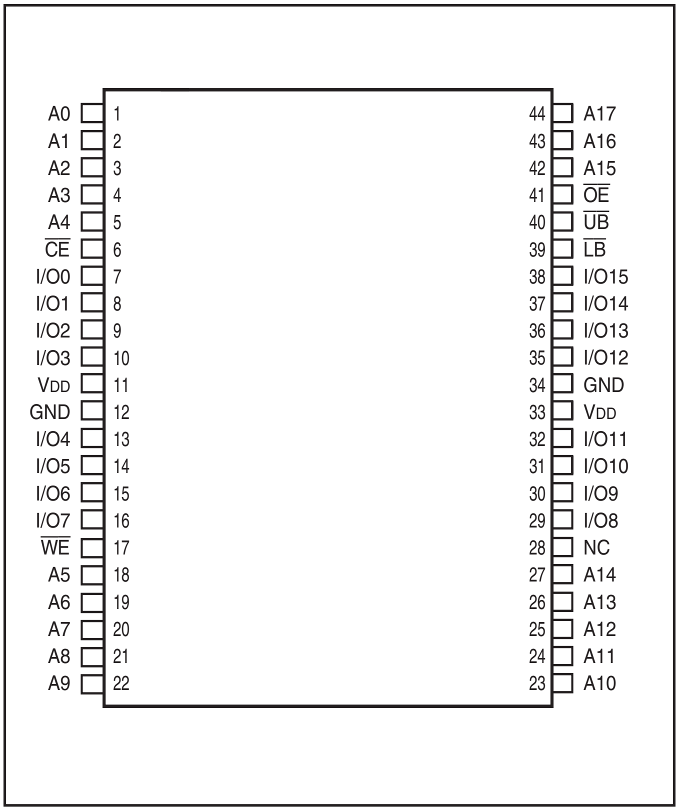
TRUTH TABLE

						I/O PIN		
Mode	$\overline{\text{WE}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	**I/O0-I/O7**	**I/O8-I/O15**	**VDD Current**
Not Selected	X	H	X	X	X	High-Z	High-Z	ISB1, ISB2
Output Disabled	H	L	H	X	X	High-Z	High-Z	ICC
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	DOUT	High-Z	ICC
	H	L	L	H	L	High-Z	DOUT	
	H	L	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	ICC
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

PIN CONFIGURATIONS

44-Pin TSOP (Type II)

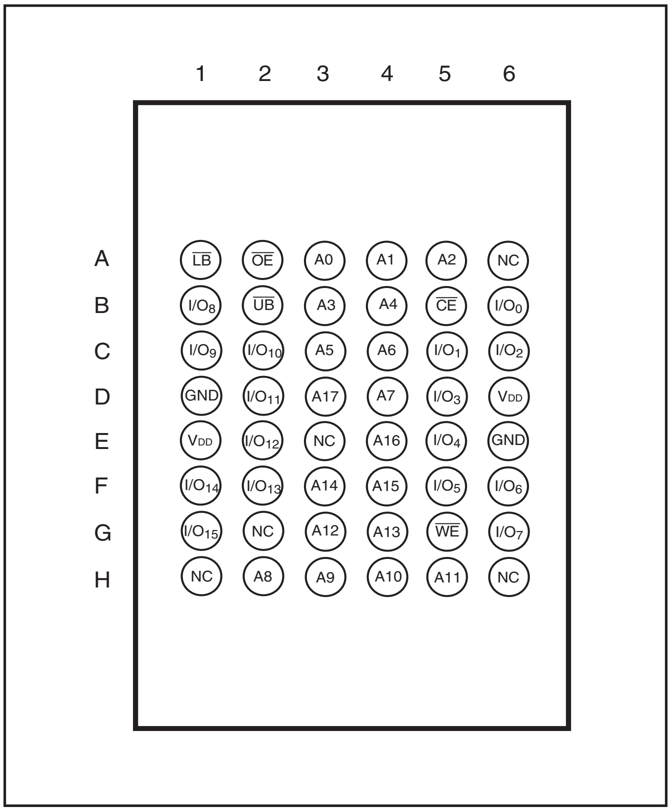


PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{LB}}$	Lower-byte Control (I/O0-I/O7)
$\overline{\text{UB}}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

PIN CONFIGURATIONS

48-Pin mini BGA



	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A0	A1	A2	NC
B	I/O$_8$	$\overline{\text{UB}}$	A3	A4	$\overline{\text{CE}}$	I/O$_0$
C	I/O$_9$	I/O$_{10}$	A5	A6	I/O$_1$	I/O$_2$
D	GND	I/O$_{11}$	A17	A7	I/O$_3$	V$_{DD}$
E	V$_{DD}$	I/O$_{12}$	NC	A16	I/O$_4$	GND
F	I/O$_{14}$	I/O$_{13}$	A14	A15	I/O$_5$	I/O$_6$
G	I/O$_{15}$	NC	A12	A13	$\overline{\text{WE}}$	I/O$_7$
H	NC	A8	A9	A10	A11	NC

PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{LB}}$	Lower-byte Control (I/O0-I/O7)
$\overline{\text{UB}}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V$_{DD}$	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD}+0.5	V
V_{DD}	V_{DD} Related to GND	–0.3 to +4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Options	Ambient Temperature	V_{DD}
A1	–40°C to +85°C	3.3V +10%, -5%
A2	–40°C to +105°C	3.3V +10%, -5%
A3	–40°C to +125°C	3.3V +10%, -5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Options	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage(1)			-0.3	0.8	V
I_{LI}	Input Leakage	GND $\leq V_{IN} \leq V_{DD}$	A1 A2 A3	-2 -5 -10	2 5 10	µA
I_{LO}	Output Leakage	GND $\leq V_{OUT} \leq V_{DD}$, Outputs Disabled	A1 A2 A3	-2 -5 -10	2 5 10	µA

Notes:
1. V_{IL} (min.) = –2.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

				-10		-12		
Symbol	**Parameter**	**Test Conditions**	**Options**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	A1	—	100	—	—	mA
			A2	—	—	—	110	
			A3	—	—	—	120	
I_{SB}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., $V_{IN} = V_{IH}$ or V_{IL} $\overline{CE} \geq V_{IH}$, f = f_{MAX}.	A1	—	50	—	—	mA
			A2	—	—	—	55	
			A3	—	—	—	60	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., $V_{IN} = V_{IH}$ or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	A1	—	20	—	—	mA
			A2	—	—	—	30	
			A3	—	—	—	40	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	A1	—	15	—	—	mA
			A2	—	—	—	25	
			A3	—	—	—	35	
			typ(2)	—	5	—	5	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change. Shaded area product in development
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE(1)

Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	ns
t_{HZOE}(2)	$\overline{OE}$ to High-Z Output	—	4	—	5	ns
t_{LZOE}(2)	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}(2	$\overline{CE}$ to High-Z Output	0	4	0	6	ns
t_{LZCE}(2)	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	4	—	5	ns
t_{HZB}(2)	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	3	0	4	ns
t_{LZB}(2)	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns
t_{PU}	Power Up Time	0	—	0	—	ns
t_{PD}	Power Down Time	—	10	—	12	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

AC TEST LOADS

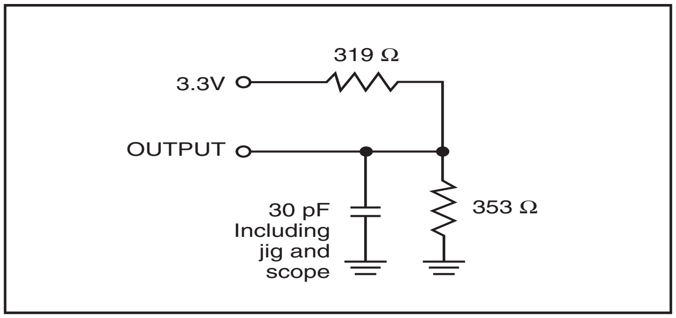


Figure 1

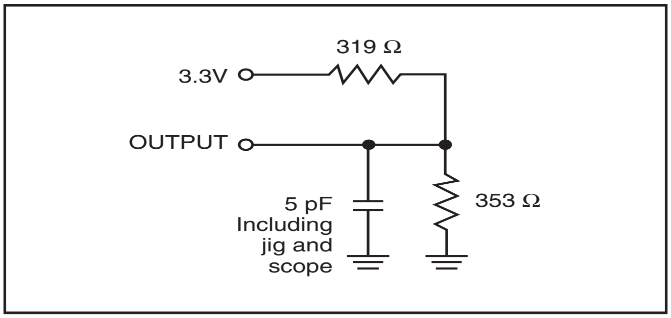


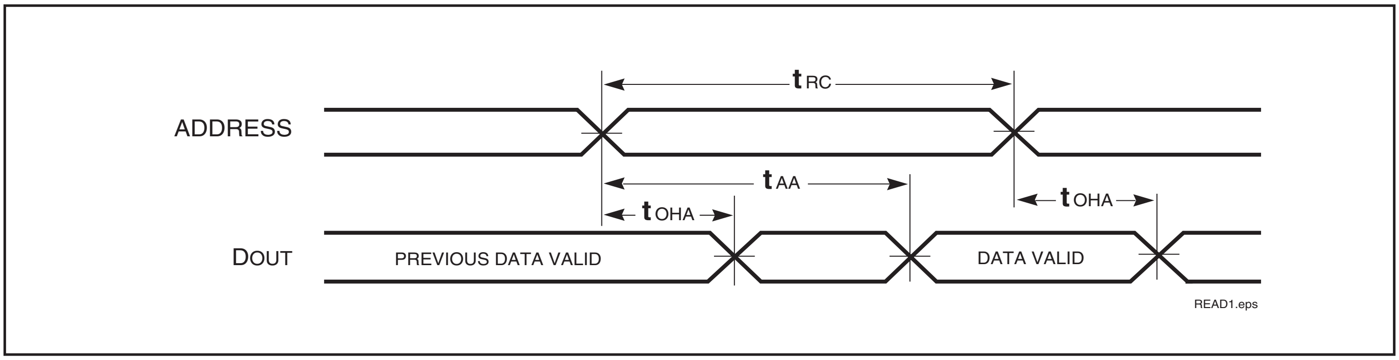
Figure 2

AC TEST CONDITIONS

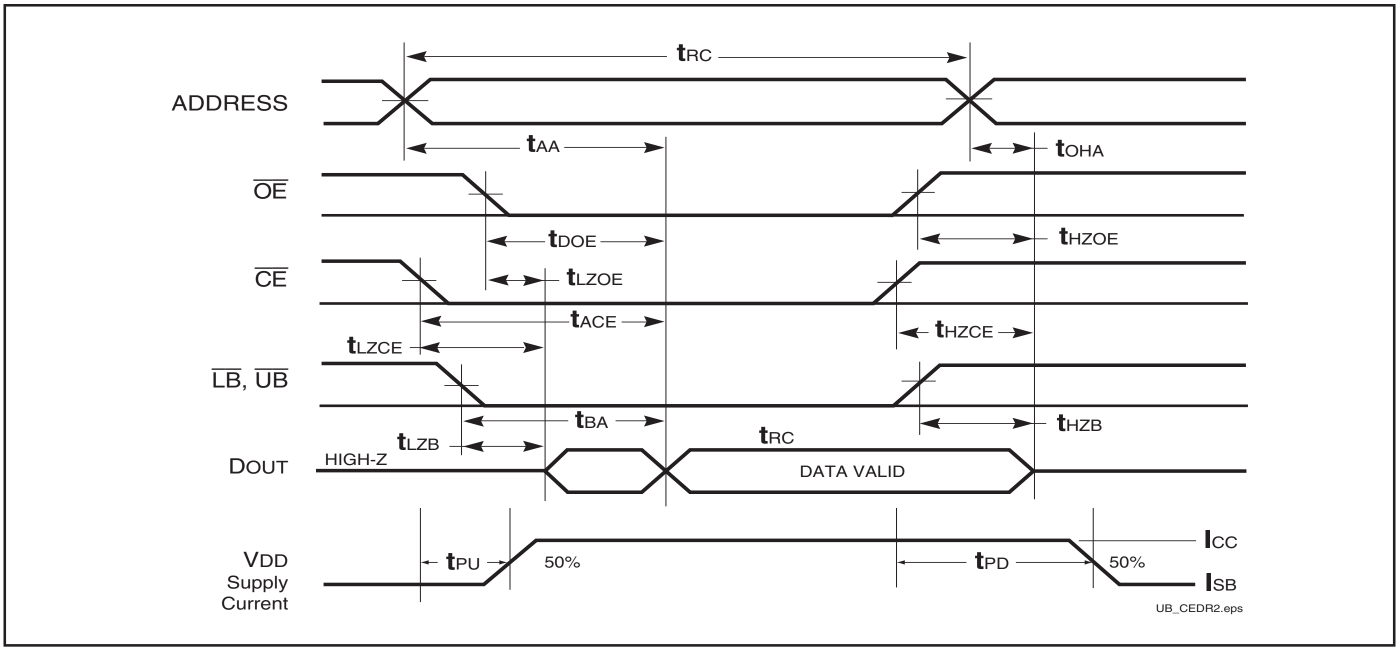
Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

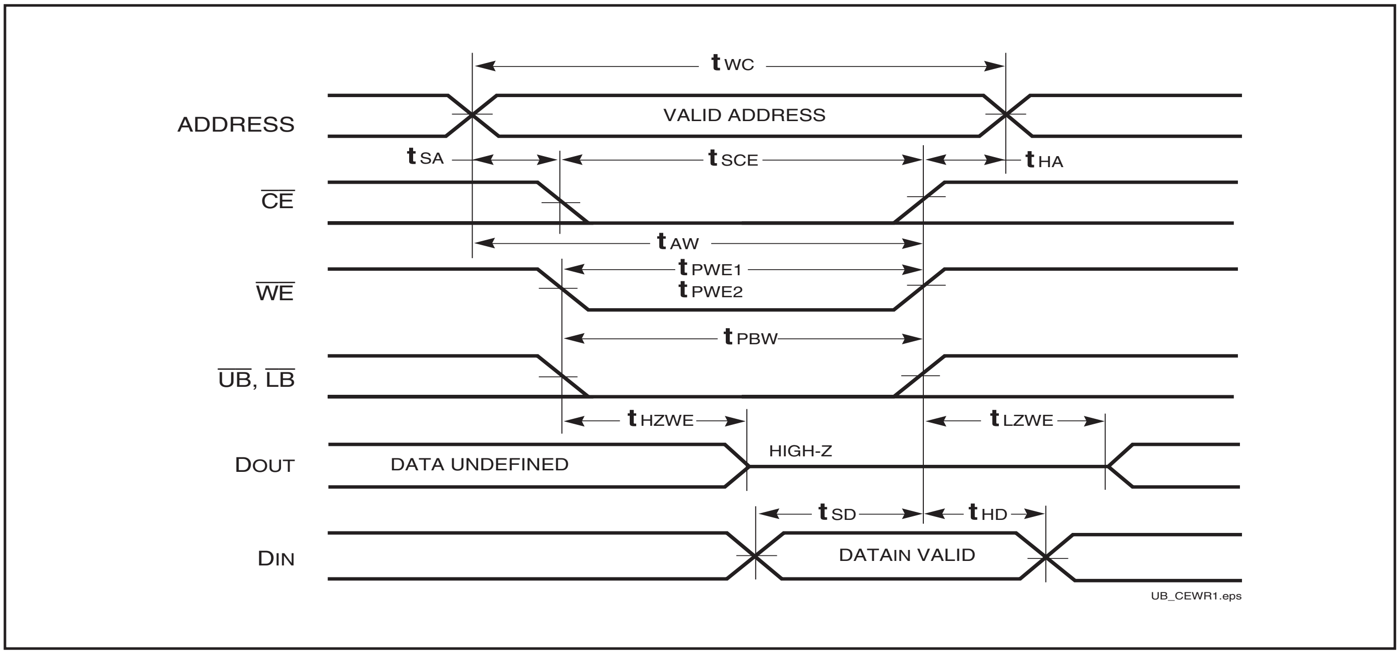
Symbol	Parameter	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PBW}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	8	—	8	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	8	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	10	—	10	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}(2)	$\overline{WE}$ LOW to High-Z Output	—	5	—	6	ns
t_{LZWE}(2)	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$ and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

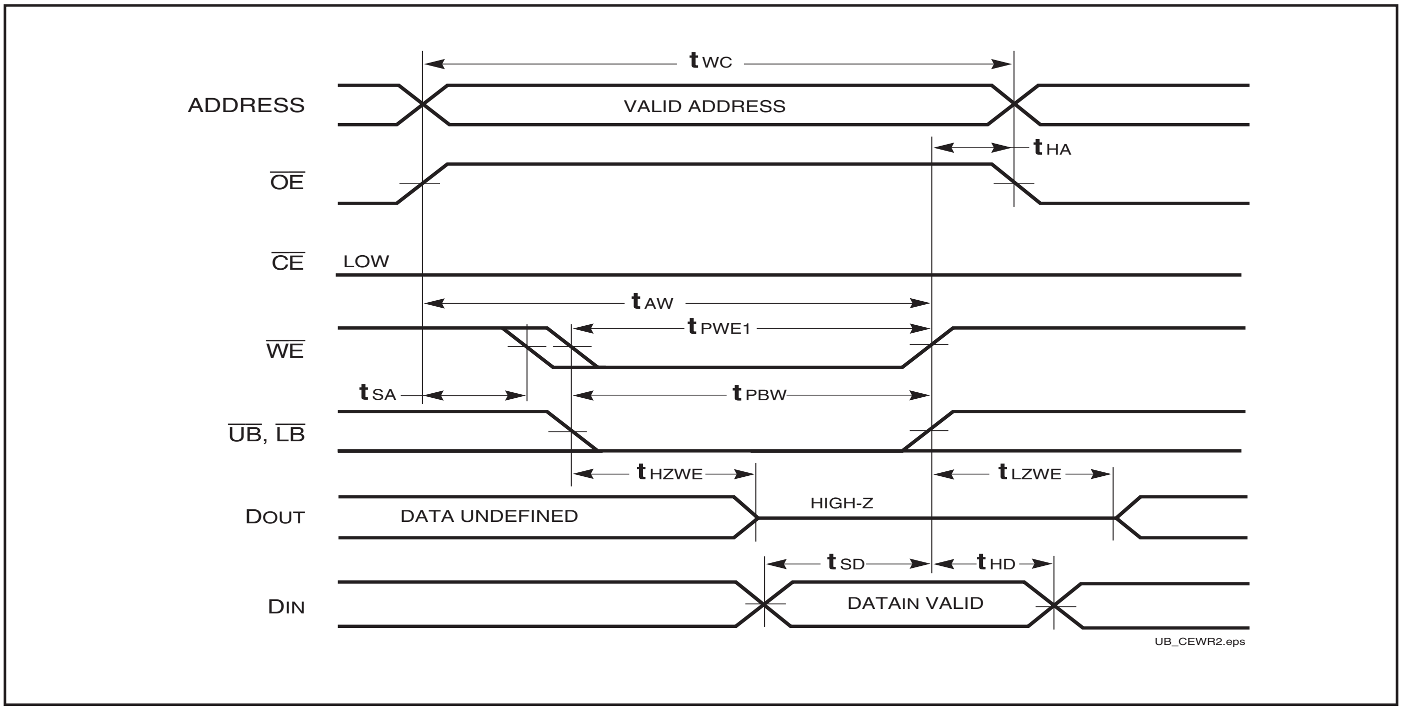
WRITE CYCLE NO. 1 ($\overline{\text{CE}}$ Controlled, $\overline{\text{OE}}$ is HIGH or LOW) (1)



Notes:

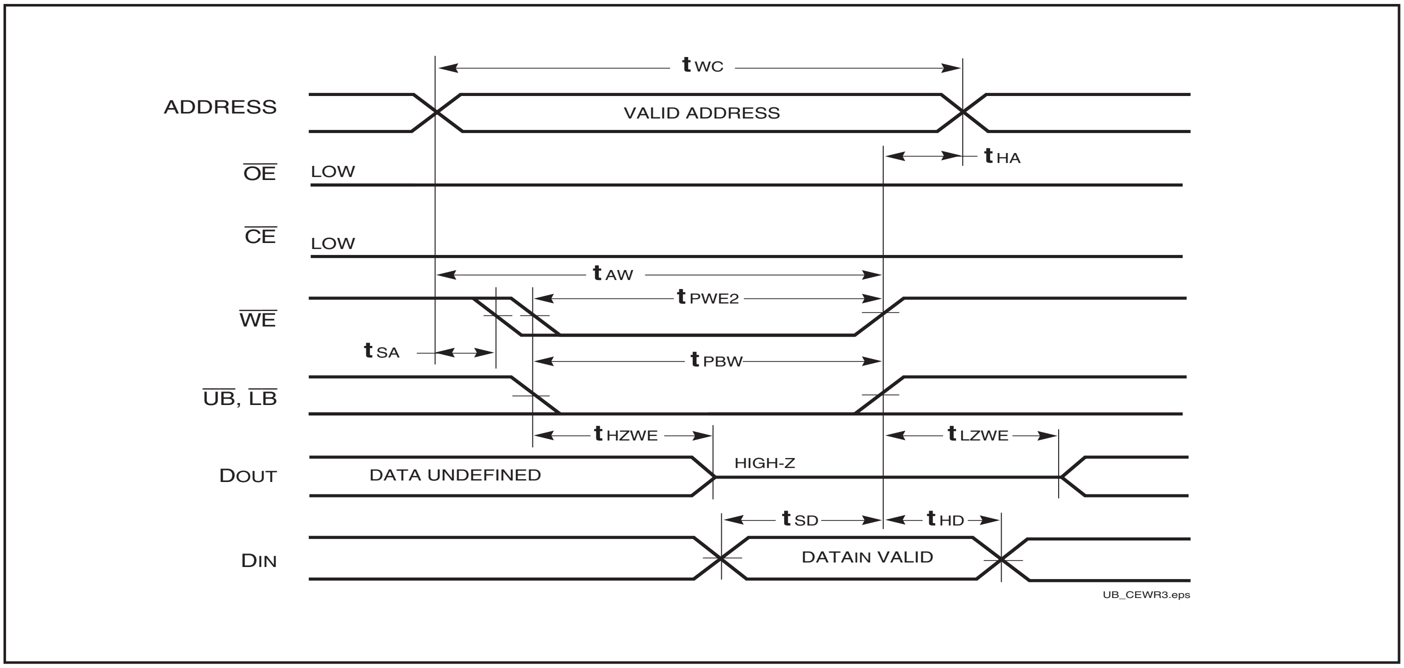
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ inputs and at least one of the $\overline{\text{LB}}$ and $\overline{\text{UB}}$ inputs being in the LOW state.
2. WRITE = ($\overline{\text{CE}}$) [($\overline{\text{LB}}$) = ($\overline{\text{UB}}$)] ($\overline{\text{WE}}$).

WRITE CYCLE NO. 2 ($\overline{\text{WE}}$ Controlled. $\overline{\text{OE}}$ is HIGH During Write Cycle) (1,2)

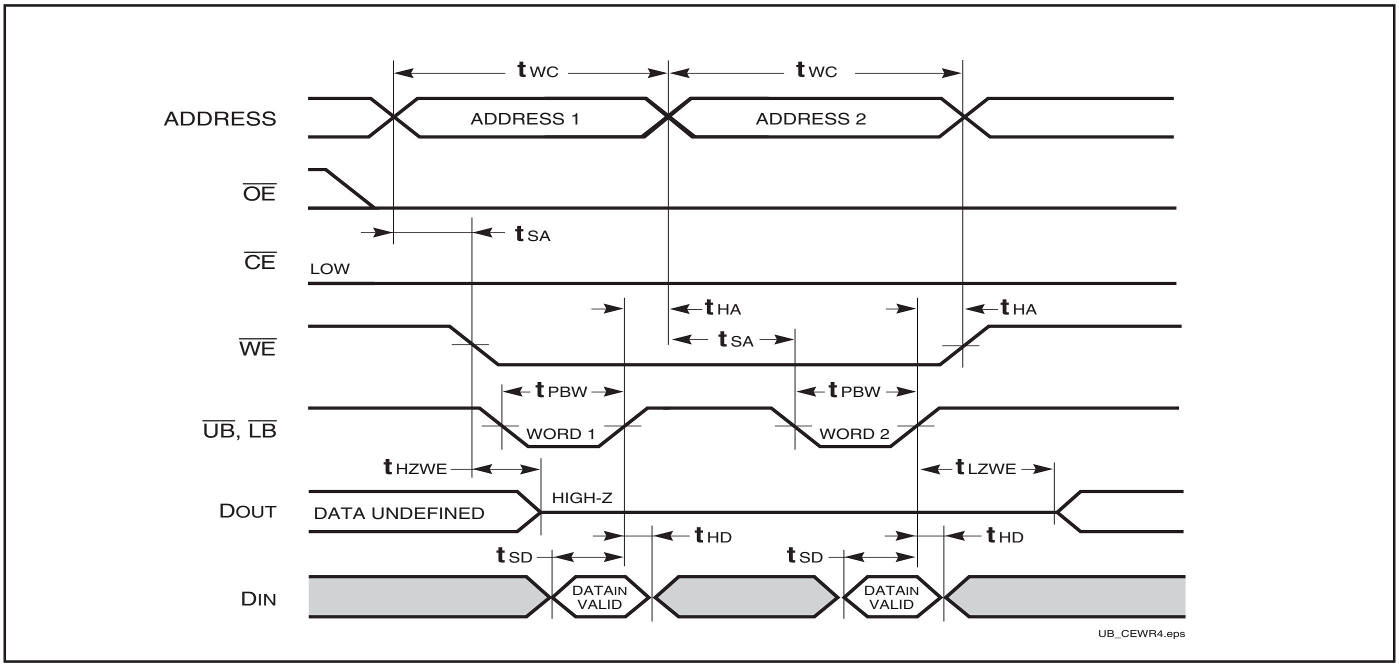


AC WAVEFORMS

WRITE CYCLE NO. 3 (WE Controlled. OE is LOW During Write Cycle) (1)



WRITE CYCLE NO. 4 (LB, UB Controlled, Back-to-Back Write) (1,3)



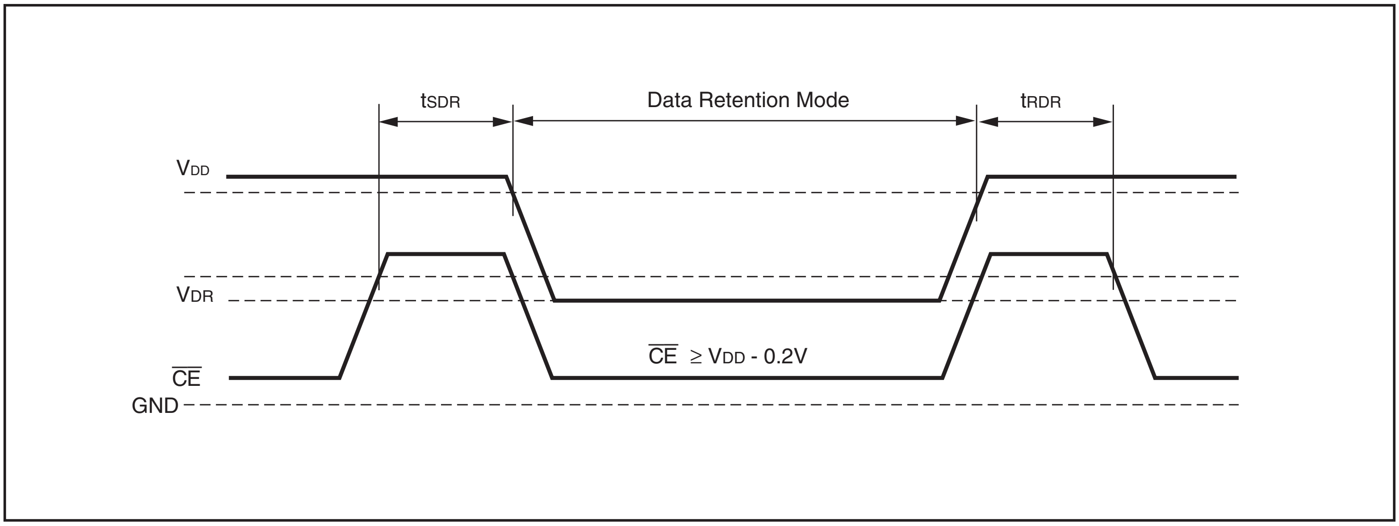
Notes:
1. The internal Write time is defined by the overlap of CE = LOW, UB and/or LB = LOW, and WE = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The tSA, tHA, tSD, and tHD timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with OE HIGH for a minimum of 4 ns before WE = LOW to place the I/O in a HIGH-Z state.
3. WE may be held LOW across many address cycles and the LB, UB pins can be used to control the Write function.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Options	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	A1	—	5	10	mA
			A2	—	—	15	
			A3	—	—	20	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS64LV25616AL-10TA1	TSOP (Type II)

Temperature Range (A2): –40°C to +105°C

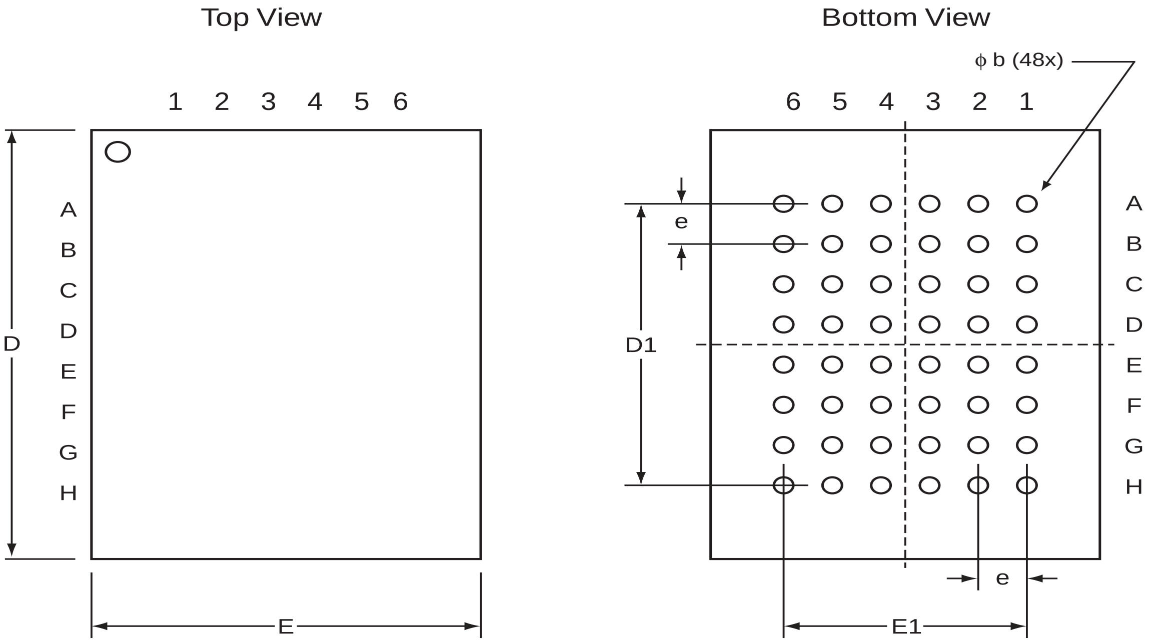
Speed (ns)	Order Part No.	Package
12	IS64LV25616AL-12TA2	TSOP (Type II)
	IS64LV25616AL-12TLA2	TSOP (Type II), Lead-free
	IS64LV25616AL-12BA2	Mini BGA (8mm x 10mm)

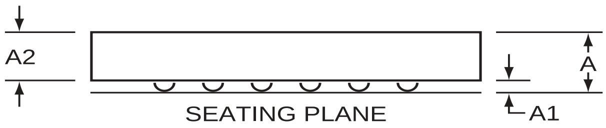
Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
12	IS64LV25616AL-12TA3	TSOP (Type II)
	IS64LV25616AL-12TLA3	TSOP (Type II), Lead-free
	IS64LV25616AL-12BA3	Mini BGA (8mm x 10mm)
	IS64LV25616AL-12BLA3	Mini BGA (8mm x 10mm), Lead-free

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: B (48-pin)





Notes:
1. Controlling dimensions are in millimeters.

mBGA - 6mm x 8mm

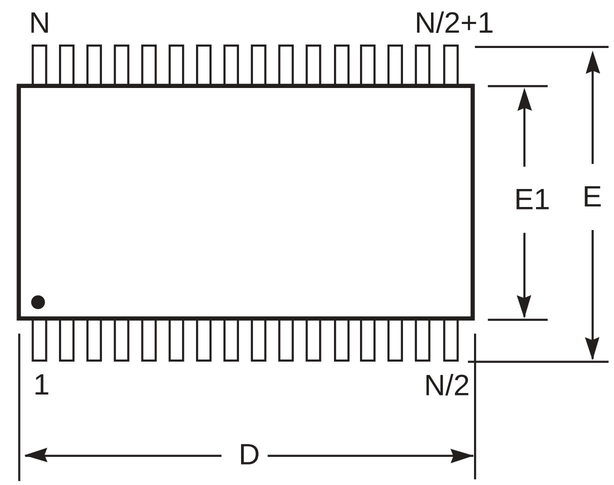
	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	7.90	—	8.10	0.311	—	0.319
D1		5.25 BSC			0.207 BSC	
E	5.90	—	6.10	0.232	—	0.240
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC			0.030 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

mBGA - 8mm x 10mm

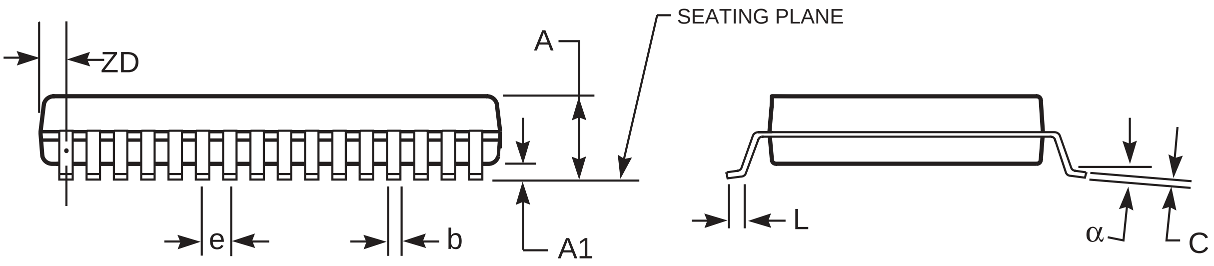
	MILLIMETER			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	9.90	—	10.10	0.390	—	0.398
D1		5.25 BSC			0.207 BSC	
E	7.90	—	8.10	0.311	—	0.319
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC			0.030 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

PACKAGING INFORMATION

Plastic TSOP
Package Code: T (Type II)



Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	**32**				**44**				**50**			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

Rev. F
06/18/03